

STRATEGY FOR TIMING ADJUSTMENT OF ATLAS END-CAP/FORWARD MUON TRIGGER SYSTEM

Kazumi Hasuko¹, Satoshi Matsuura¹ and Osamu Sasaki²

¹*International Center for Elementary Particle Physics (ICEPP), University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-0033 JAPAN,*

²*High Energy Accelerator Research Organization (KEK)
1-1 Oho Tsukuba Ibaraki, 305-0801 JAPAN*

ABSTRACT

We present a strategy for timing adjustment of ATLAS end-cap/forward muon level-1 trigger system. A basic timing setup utilizing variable delays is described. The delays with sub-nanosecond precision are introduced for the timing setup in bunch-crossing identification. For all the downstream logic, the timing is set up using test pulses and course delays in the step of 25/2 ns. The delay adjustments can be obtained using measurable delay elements, such as TOFs, cable delays, etc., and the BC clock offset obtained when beams are available. All the delay elements will be arranged into a database to achieve adequate timing setup.

1 INTRODUCTION

In the LHC, where the trigger rate is very high and the number of detector channels is very large, it is an important issue to make sure that all the signals generated at the same bunch crossing are read out optimally. Hence some procedures must be defined to set up and maintain the timing over the whole experiment.

In this paper, we present a strategy for timing adjustment of ATLAS end-cap/forward muon level-1 trigger system [1, 2]. The Thin Gap Chambers (TGCs) [3] are used for the system. Two type of TGCs, doublet and triplet, are arranged in seven layers (one triplet and two doublets) in each end-cap at ~ 14 m from the interaction point in the beam direction. The size of the whole TGC system is large and it has a large number of channels. Thus a large number of electronics boards is needed. Most of them will not be easily accessible after they are mounted on the detector surfaces. Hence a scheme to set up timing must be defined when the electronics boards are designed.

2 TGC TRIGGER SYSTEM

Figure 1 shows an overview of the TGC level-1 trigger system. The system is divided into several parts and a TGC signal is precessed as follows.

At first, the TGC signal is processed on an Amplifier-Shaper-Discriminator (ASD) board attached with the detector. The signal is then received by a Patch Panel (PP) to identify the bunch crossing. A Slave Board (SB) follows the PP to perform coincidence operations for low- p_T tracks. SBs are directly connected to the corresponding PPs, forming a unit package (P-S Pack; see Figure 2). Output signals from the doublet and triplet SBs are sent to a High- p_T Board (HPB) to be combined for high- p_T tracks. A Sector Logic Board (SLB) follows the HPBs to perform R - ϕ coincidence operations. The result is sent to the Muon Central Trigger Processor Interface (MUCTPI) to be combined with the information on barrel muon trigger system. The result from MUCTPI is sent to the Central Trigger Processor (CTP) and combined with the information on calorimeter system. As a result, the CTP generate a trigger or a Level-1 Accept (L1A) signal. The L1A is sent to the Timing Trigger and Control (TTC) system to be distributed to the read-out electronics with the LHC clock (BC clock) and the synchronization signals (BCR, ECR). Each read-out electronics has a TTCrx chip to receive the signals from the TTCvi.

Since the TGC system contains a large number of channels and trigger planes (one triplet and two doublets) are separated each other, it is impossible to set up the timing of the system by only optimizing the locations of electronics boards and adjusting cable length. Hence the variable delays shown in Figure 1 are introduced. The timing setup with these delays for each part is described below.

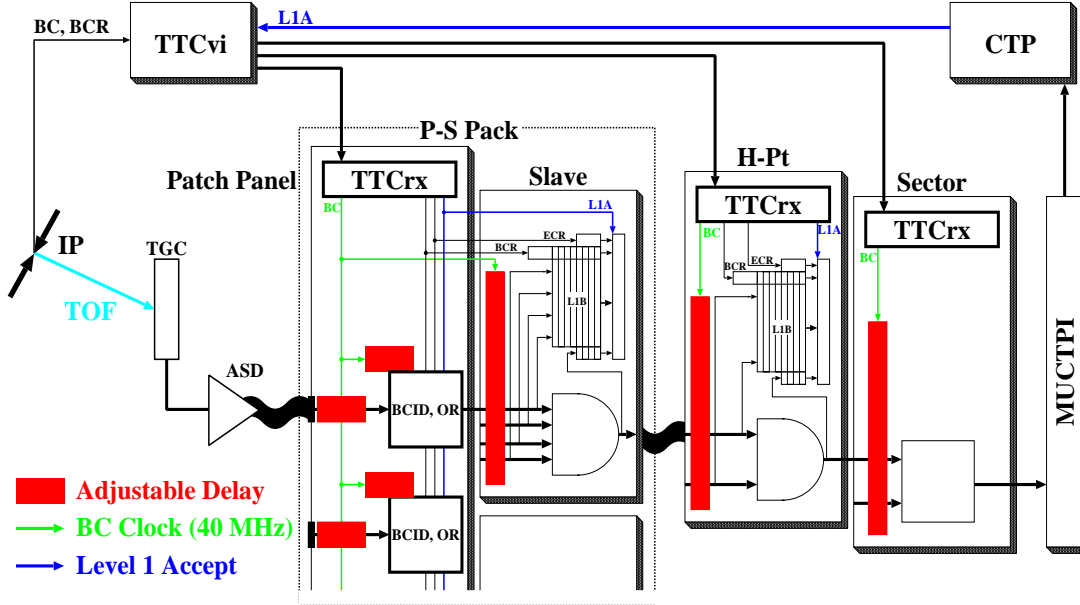


Figure 1: Overview of the TGC first-level trigger scheme. The variable delays are shown as gray boxes.

2.1 Patch Panel

The timing setup in a PP is most important because the asynchronous TGC signals are bunched by bunch-crossing identification (BCID) circuit. The main point is to set up the timing relation between signal and clock to bunch all the signals in the same clock. Since the time jitters of TGC signals are ~ 25 ns, the required precision for the adjustment is less than 1 ns. We plan to set the variable delays in the step of $25 \text{ ns}/D$, where $D = 32$ hence the step is ≈ 780 ps.

The timing setup is as follows. First, the clock arrival time (T_i^c) is adjusted to produce the simultaneous BCID output in each P-S pack. Since the BC clock is served by a TTCrx equipped in a P-S pack, the latency on clock from TTCrx to BCID ($d\theta_i$) is different at each BCID circuit. The adjustment is achieved using delays to cancel the relative difference in clock arrival time. In PPs, 16 channels are grouped in a signal cable, and one delay is used for each cable. The adjusted arrival time of n -th clock for i -th cable is then expressed in ns as

$$T_i^c = \text{OFFSET} + df\theta_l + 25n_i + d\theta_i + adj\theta_i. \quad (1)$$

This is expressed using the measurable delay elements shown in Table 1 and the delay adjustment ($adj\theta_i$). The important thing is that T_i^c includes the BC clock offset (OFFSET), which is the time when the first clock is distributed from TTCvi after the beam crossing. The OFFSET value is obtained only with beams. The method to obtain the value is considered later.

Second, the signal arrival time is adjusted to bunch the signals in the adjusted clock. The difference in the

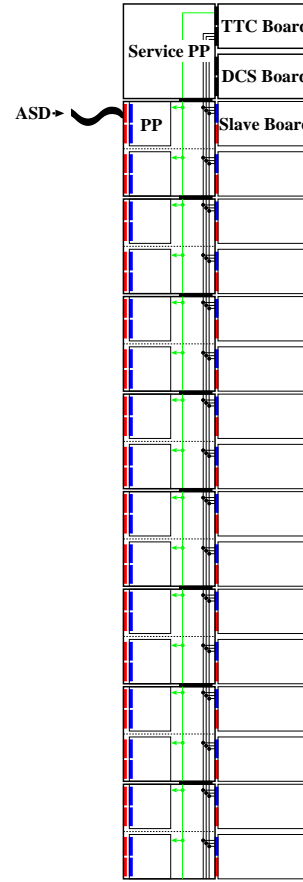


Figure 2: A P-S pack. Showing the wiring of BC, L1A, BCR and ECR distributed from a TTCrx.

arrival time is due to differences in the time of flight (TOF) and cable delay from ASD to PP ($d1_i$). With the delay adjustment of the signal ($adj1_i$), the ideal (no time jitter) arrival time (T_i^s) is expressed as

$$T_i^s = TOF_i + d1_i + adj1_i. \quad (2)$$

Timing relation between T_i^c and T_i^s is shown in Figure 3. Because of the time jitter of signals, the earliest-arriving signal ($T_i^{s'}$) must satisfy the following condition:

$$0 \leq T_i^{s'} - T_i^c < \frac{25}{D} \text{ (ns)}. \quad (3)$$

The earliest-arriving signal has the minimal time jitter; thus it almost corresponds to the ideal signal. Hence $T_i^{s'} \simeq T_i^s$ and the timing has to be set up for all the signals to arrive at the BCID just after the clock edge.

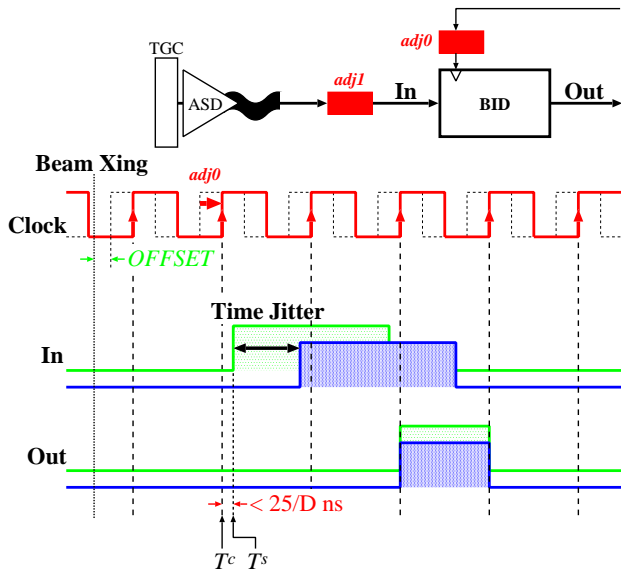


Figure 3: Timing chart for a bunch-crossing identification. $adj0_i$ and $adj1_i$ are delay adjustment on clock and TGC signal respectively.

The variable delays can be set between 0 and 25 ns. We can obtain a set of simultaneous BCID output in each P-S pack if this range is enough to set up the timing. This possibility depends on the design of the P-S pack and the timing setup can be achieved in the current design (see Figure 2).

The settings of variable delays are obtained with only the measurable delay elements except *OFFSET*. Hence the unique timing adjustment is set up if the clock offset is obtained.

2.2 Slave Board

In Slave Boards (SBs), we have to consider the timing of the signals at the coincidence logic and level-1 buffer

(L1B) for readout. Hence we need to adjust the arrival time of signals using variable delays at the entrances of coincidence logic and L1B. Since incoming signals in SBs have already been bunched, only coarse delays are needed. In principle, the delays in the step of 25 ns will work to set up the timing here. However, the step should be a half of 25 ns because we have to prevent signals from arriving near the edge of clock.

The delay adjustment is obtained with only the measurable delay elements (shown in Table 1) in principle. However, the delays are adjusted using test pulses to confirm the correct timing. Note that the delay adjustment for SBs are independent of the clock offset. Once signals are correctly bunched and synchronized in PPs, the timing adjustment in SBs are easily achieved.

The timing setups of L1A, BCR and ECR are also needed because of the difference in the signal-path length between the SBs in a P-S pack (see Figure 2). In our current plan, these setups are achieved by adjusting the L1B length.

2.3 High- P_T Board, Sector Logic, etc.

We should also consider the timing setups for the downstream logic of SBs, such as High- P_T , Sector Logic, etc. These setups are very similar to that for SB. However, much wider range of variable delays are needed since the incoming signals from different parts of upstream logic are combined to perform the coincidence operations. For instance, signals from both the doublet SBs and triple SBs are combined at HPBs and R and ϕ signals are combined at SLBs.

3 SCHEME OF TIMING SETUP

In this section, a possible scheme of timing setup is described. There are three steps in it. First, the timing up to the CTP is set up using test pulses before beams are available. Second, the *OFFSET* value is obtained with beams. Last, the trigger and synchronization signals are adjusted at readout elements. Each step is described below.

3.1 Timing Setup Using Test Pulses

For the TGC system, test pulses are generated in PPs and provided for ASD boards. They return the pulses back to the PPs instantly. These incoming test pulses can be treated as if they were TGC signals and hence the timing can be set up using them. However, the settings of variable delays ($adj0_i$ and $adj1_i$) obtained above are not valid since the test pulses take no account of the difference in TOF . Hence the special timing adjustment is needed for the test pulses. The test-pulse generator has its own delay ($adjT_i$) and such the timing adjustment can be achieved using the delays. $adjT_i$ is a function of $adj0_i$ and $adj1_i$, and it

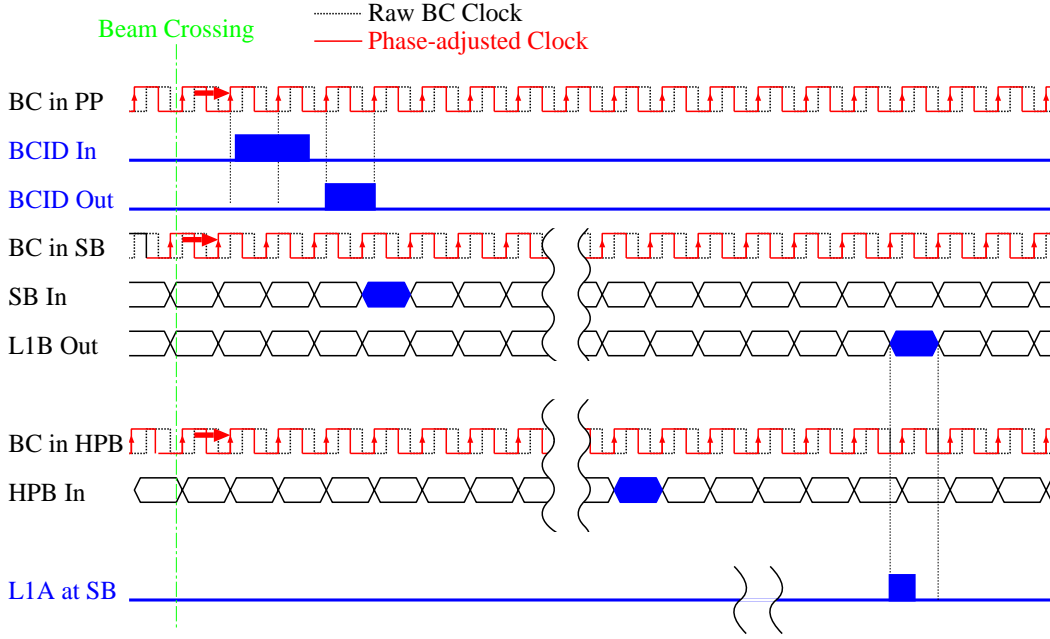


Figure 4: Timing chart of the TGC system with phase-adjusted clocks

is fixed uniquely if *OFFSET* value is known. Since *OFFSET* is not obtained before beams are available, we assume *OFFSET* = 0 at this time and consider it later. This assumption enables us to set up the timing relation between signals. The adjusted test pulses are sent out from the BCID circuits simultaneously in each P-S pack. The timing setup of the whole downstream logic can be achieved using these test pulses.

The outputs from Sector Logic are fed by MUCTPI and CTP and a L1A is generated by CTP. The L1A finally reach the L1B in the front-end electronics via TTCvi and TTCrx. Since the MUCTPI and CTP depends on other subsystems, the exact timing cannot be set up only within the TGC system. However, the total latency on L1A can be estimated with the estimated delay on L1A at the MUCTPI and CTP. Using this information, the timing of L1A at L1Bs can be adjusted. This timing can be readjusted when beams are available.

3.2 BC Clock Offset

The timing relation between signals is adjusted in the previous step. *OFFSET* value is then obtained with beams to set up the timing relation between signals and clocks.

The LHC bunch structure is utilized to obtain *OFFSET* value. As described in TDR [2], we can see the bunch structure in the the histogram of the number of track hits as a function of BCID for correct *OFFSET* value, while no bunch structure appears for any wrong *OFFSET*. Hence *OFFSET* value is scanned until the bunch structure can be seen. Scan-

ning the *OFFSET* value corresponds to adjusting the clock phase. Since the relative signal timing is adjusted using test pulses, the wrong timing of the TGC system is only due to an incorrect *OFFSET*. Hence we can set up the correct timing in BCID by adjusting the clock phase. To keep the timing setup achieved in the previous step, the clock phase is adjusted using the delays in TTCvi. Figure 4 shows the timing chart of the TGC system when the clock phase is adjusted with TTCvi delays.

3.3 Timing Setup of Trigger and Synchronization Signals

In the last step, the timing of L1A and synchronization signals (BCR and ECR) for readout (L1B) is set up.

When *OFFSET* is found and the LHC bunch structure is seen in the histogram above, the BCID may be assigned incorrectly there. This is due to the incorrect BCR timing. Hence the BCR timing is adjusted to see the correct BCID.

Next, the L1A timing is checked at, for the instance, BCID = 1. Though the trigger timing has been adjusted at the step using test pulses, small adjustment may be needed here.

Finally the ECR timing is adjusted to see the correct BCID and trigger.

4 DATABASE OF DELAY ADJUSTMENT

The timing setup described above needs a large number of settings of variable delays over the whole TGC system. Thus these settings should be arranged as a database to achieve adequate timing setup. The delay adjustment in PPs (including the setup of test pulses) is expressed using the measurable delay elements. Even though the timing is set up using test pulses for all the downstream logic from PPs, the initial settings of delays can be estimated from the measurable delay elements. Hence all the delay elements should be arranged into a database to achieve easy, quick setup using test pulses. Main delay elements of the system are listed in Table 1.

Symbol	Delay Element
(PP)	
<i>OFFSET</i>	BC clock offset
$df0_i$	Fiber delay from TTCvi to TTCrx
$d0_i$	Latency on clock from TTCrx to BCID
<i>TOF</i>	Time of flight
$d1_i$	Cable delay from ASD to PP
(SB)	Latency on clock from TTCrx to SB
	Latency on signal from PP to SB
	Latency in coincidence logic
(HPB)	Latency on clock from TTCrx to HPB
	Cable delay from SB to HPB
	Latency in coincidence logic
(SLB)	Latency on clock from TTCrx to SLB
	Latency on signal from HPB to SLB
	Latency in coincidence logic

Table 1: Main delay elements used for the delay adjustment (up to MUCTPI)

5 SUMMARY

We have report on the strategy for timing adjustment of ATLAS end-cap/forward muon trigger system. A basic timing setup utilizing variable delays was described.

The timing setup in a Patch Panel is most important because the bunch-crossing identification (BCID) is performed. Since the TGC signals are asynchronized and their time jitters are up to 25 ns, the required precision for the adjustment is less than 1 ns. The delays in the step of $25 \text{ ns}/32 \approx 780 \text{ ps}$ are introduced to set up the timing. The delay adjustments are calculable from measurable delay elements, such as TOFs, cable delays, etc., and the BC clock offset obtained when beams are available. For all the downstream logic, the timing is set up using test pulses and course delays in the step of $25/2 \text{ ns}$.

A scheme of timing setup using test pulses was described. The timing of test pulses provided by PPs is adjusted to produce a set of simultaneous BCID output in each P-S pack. The timing setup of the whole downstream logic can be achieved using these test pulses up to generating L1A signals. After setting up the timing with test pulses, *OFFSET* value is obtained with beams by utilizing the LHC bunch structure. The wrong timing of the TGC system is only due to an incorrect *OFFSET*; thus the correct timing is achieved by adjusting the clock phase. It is adjusted using the delays in TTCvi to keep the timing setup achieved in the previous step. Finally the timing of L1A, BCR and ECR is adjusted with similar scheme to the TDR.

A large number of settings of variable delays over the whole TGC system are arranged as a database. All the delay elements should be arranged into a database to achieve easy, quick timing setups of all the logic in the system.

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