

The electron/photon and tau/hadron Cluster Processor for the ATLAS First-Level Trigger - a Flexible Test System

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Abstract

The electron/photon and tau/hadron first-level trigger system for ATLAS will receive digitised data from approximately 6400 calorimeter trigger towers, covering a pseudo-rapidity region of ± 2.5 . The system will provide electron/photon and tau/hadron trigger multiplicity information to the Central Trigger Processor, and Region of Interest information for the second-level trigger. The system will also provide intermediate results to the DAQ system for monitoring and diagnostic purposes. The system consists of four different 9U-module designs and two different chip (ASIC/FPGA) designs. This paper will outline a flexible test system for evaluating various elements of the system, including data links, ASICs/FPGAs and individual modules.

1. INTRODUCTION

The cluster processor (CP) system for the electron/photon and tau/hadron first-level trigger [1] will receive digitised data from approximately 6400 calorimeter trigger towers from the Pre-processor system using serial links. The CP system consists of four crates of cluster processor modules (CPMs), each crate processing a quadrant of the calorimeter in ϕ and the complete η range (± 2.5). This is carried out by using 13 cluster processor modules per crate, each processing a 0.4×1.6 ($\Delta\eta \times \Delta\phi$) region of the calorimeter. The partial trigger multiplicity from all the CPMs will be merged on separate cluster hit-counting modules (HCMs), and the final multiplicity result transferred to the central trigger processor (CTP) where the level-1 decision is made.

Read-out driver modules (RODs) in another crate will handle the DAQ data from all the CPMs and regions of

interest (RoI) information for level-2 by using different firmware. The data will be transferred onto the RODs using high-speed serial links, and the RODs will further process and format the data before transferring it to the appropriate destinations via S-links. The DAQ data can be accessed using a single board computer in the ROD crate for system diagnostics and monitoring.

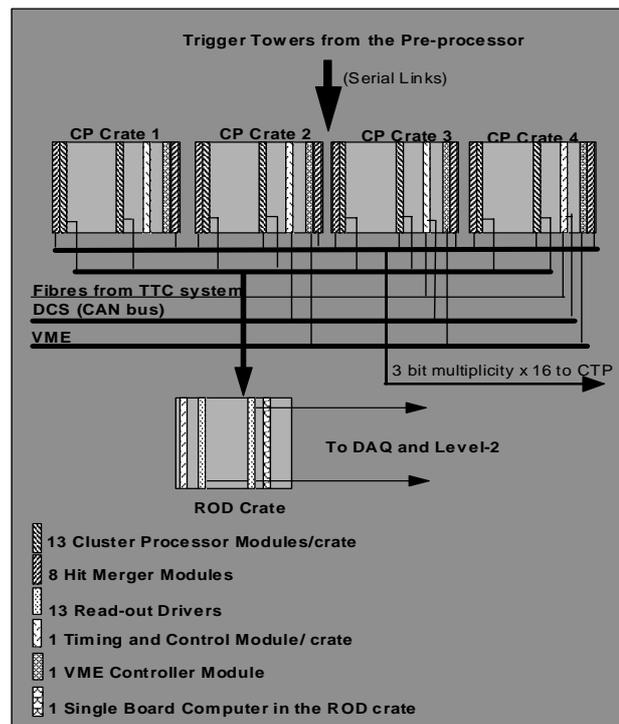


Figure 1. Cluster Processor System

Each of the crates in the CP system will include a timing and control module (TCM) which will interface to the LHC timing distribution system (TTC) and the Detector Control System (DCS).

Four different 9U-module designs and two different chip (ASICs or FPGAs) designs will be required for the CP system.

During the system development and commissioning phases we will require a source of data to drive the inputs of the devices under test, and a means of verifying the resultant outputs. We have designed a data source and sink (DSS) module to handle various test scenarios, including testing, ASICs, FPGAs high-speed links, RODs and CPMs.

2. DATA SOURCE AND SINK MODULE

The data source and sink module consists of a motherboard and daughter card combination (figure 2). The motherboard is a 6U VME board with space for two single Common Mezzanine Card (CMC) standard [2] daughter cards or one double CMC standard daughter card, and space for a timing card such as the CERN TTCrx test card [3] or a 'custom' timing card. The motherboard can also host the S-link standard [4] source and destination cards on the underside of the module.

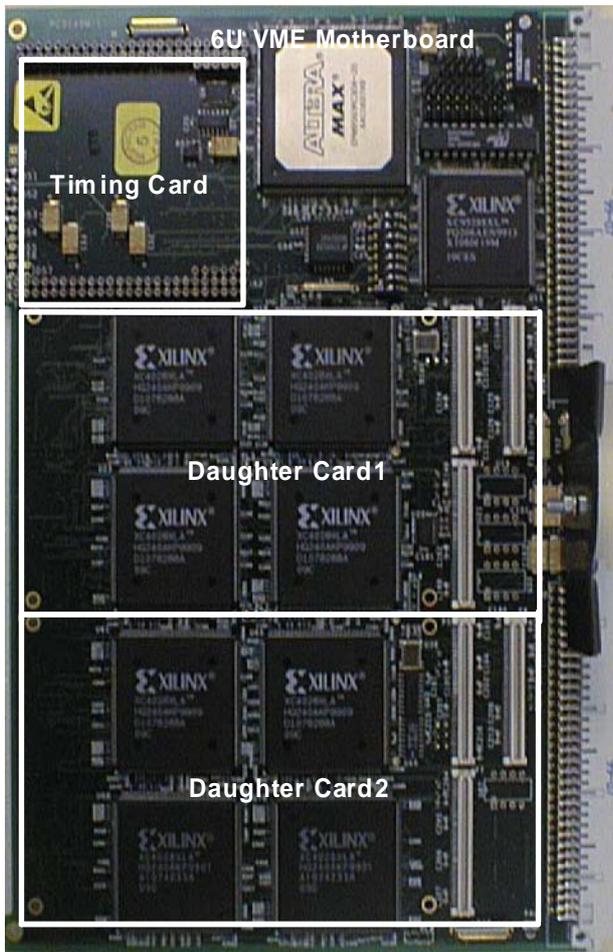


Figure 2. DSS Module

2.1 Motherboard

The motherboard implements common functions, such as a standard A32/A24, D32 VME interface, control and status registers, and a TTC interface. Extensive use of FPGAs gives the DSS module the capability of generating, receiving and comparing programmable test data patterns in real time at least up to 40 MHz. Eight 32K × 32 bit dual-port RAMs and eight FPGAs (data FPGA) will handle the data source/sink requirements, as well as handle all the interface signals required by each type of daughter card. Figure 3 shows a block diagram of the DSS motherboard. Separate FPGAs (S-link FPGAs) and the dual port RAMs associated with the S-link FPGAs will handle the S-link data.

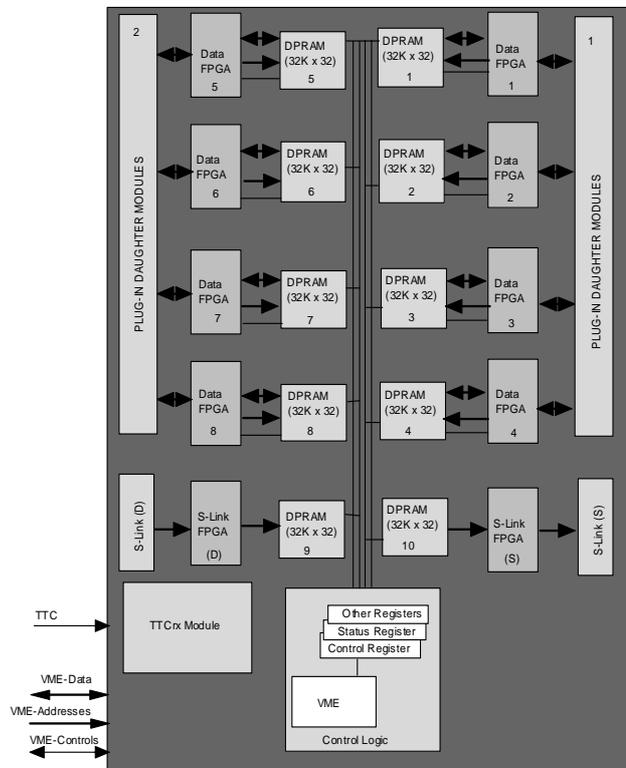


Figure 3. DSS Block Diagram

2.2 FPGA Implementation

The FPGAs used in this design are Xilinx XC4028XLA devices [5]. There are 10 FPGAs on the motherboard, out of which eight FPGAs (data FPGAs) handle data from the two CMC daughter cards, and the other two FPGAs (S-link FPGAs) handle S-link source and destination data and control. The 'data FPGAs' handle source data and sink data in two blocks of four, interfacing to the two daughter cards via the CMC connectors as shown in figure 3. The two blocks of FPGAs can be configured to be either a source or a sink, or both source or both sinks.

2.3 Source FPGA

The source FPGAs (figure 4) will perform the following functions:

1. Provide interface to the daughter cards.
2. Implements a Pseudo Random Bit Pattern (PRBP) generator and checker. Other data patterns such as ramps can also be implemented if required.
3. Directly connect the dual-port RAM data bus on to the connector pins, allowing various test patterns to be generated.
4. Implement the Serialiser FPGA readout logic to test the prototype readout driver.

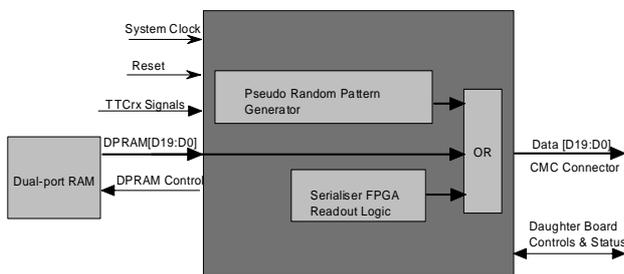


Figure 4. Source Block Diagram

2.4 Sink FPGAs

The sink FPGAs (figure 5) will interface between the dual-port RAM and the daughter cards, recording the data on to the dual-port RAM from the daughter cards, which can then be accessed via the VME. It will also provide:

1. Bit error checking facility on the PRBP data. This data is also written onto the dual-port RAMs.
2. Bit error checking between the received data and pre-loaded data on the dual-port RAM.
3. When an error occurs the data word is recorded onto an internal register with the contents of the address counter, which can be read out via the VME.

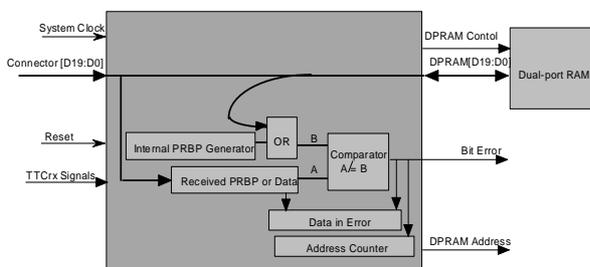


Figure 5. Sink Block Diagram

2.5 Configuring the Data FPGAs

Since the DSS will be used in various test scenarios, to give the maximum flexibility for the module users the data FPGAs can be configured in the following ways.

1. EEPROMs (equivalent to Xilinx XC1701L) on the motherboard or on the daughter card itself (see section on daughter cards) can be used to configure the data FPGAs. These EEPROMs are socketed so they can be programmed with the configuration data using a standalone device programmer.
2. In-System-Programming (ISP) via a JTAG port is provided to download configuration data from a PC.
3. A port via a VME register is provided for downloading the FPGAs as well as the EEPROMs through VME.

2.6 VME Interface

An A32/A24, D32 VME interface, and common functions such as register decoding, and control and status registers, are provided by two CPLDs on the motherboard which can be programmed in-system via a JTAG port.

2.7 CMC Daughter Cards

The CMC daughter cards will implement the physical layer to transmit/receive data up to 80 bits wide. If required the daughter cards can 'personalise' the motherboard to perform the required functions by placing the configuration EEPROM on the daughter cards (automatically disables the EEPROM on the motherboard if present). Figure 6 shows some of the daughter cards required to test the trigger prototypes. The 960 Mbaud G-link receiver and transmitter cards, and the 480 Mbaud LVDS serialiser and de-serialiser cards, have been designed and manufactured to carry out the link tests, the prototype ROD tests and to test the prototype CPMs (see section on testing below)

2.8 Timing Cards

A plug-in daughter card provides the DSS module with the appropriate clock signals. This could either be the CERN TTCrx test card, a custom card or the prototype timing and control receiver module. A custom card has been designed and manufactured to deliver a clock and two de-skew clocks at 40 MHz, and a start/stop signal to the DSS module. These signals can be generated internal to this card or the clock and start/stop signals can be brought onto the card from an external source via the front panel connectors. This card can be used for standalone tests without the need for the TTC system. Using the TTCrx test card and the TTC system (TTCvi, TTCvx) allows you to generate test patterns simultaneously using a broadcast command.

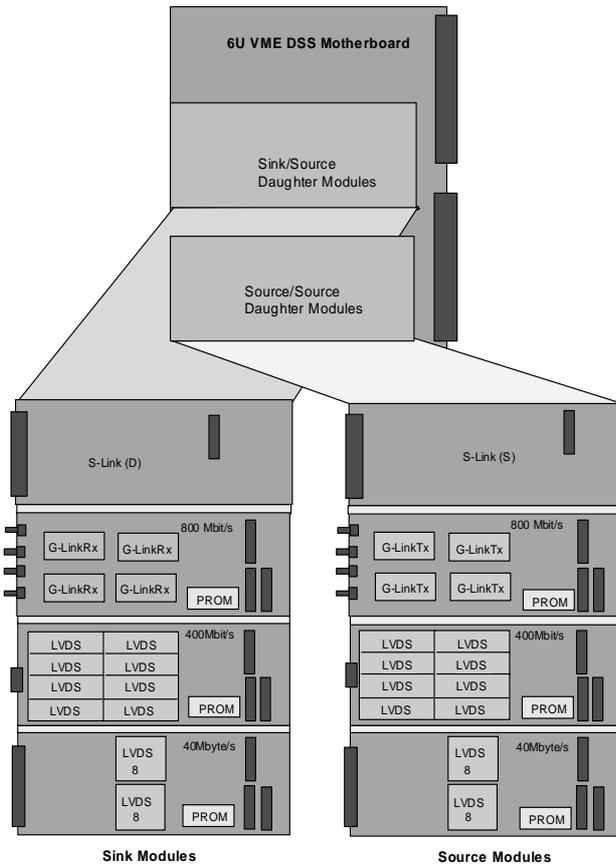


Figure 6. Daughter Cards

2.9 S-Link Daughter Cards

There are connectors on the back of the motherboard for an S-Link source card and for an S-Link destination card. Commercially available electrical parallel S-Link cards will be used for the prototype ROD tests.

3 DSS APPLICATIONS

The DSS module with different CMC daughter cards will be used for testing various prototypes, including; LVDS links, FPGAs/ASICs, RODs, CPMs and HCMs.

3.1 LVDS Link Tests

In the demonstrator system [1] we have successfully shown that we can use the HP G-Links [6] at 960 Mbaud between the Pre-processor system and the cluster processor system up to 10 m with co-axial cables. However, due to the high power dissipation of these device we are considering the use of the newly available LVDS chip sets [7] from National Semiconductor to replace the G-links. Therefore the first use of the DSS module will be to test these LVDS chips with appropriate cables. The LVDS serialiser/de-serialiser chip sets will be used to serialise ten bits on to a 480 Mbaud (10 data bits + 2 start/stop bits) link. The complete data chain including the LVDS chip set, category 5 or 6 halogen-free cables, and 2mm BERG METRAL style connectors will be tested

to establish the maximum (require at least 10 m) cable length with a bit-error-rate better than 10^{-9} per trigger tower for less than 1% false trigger rate. The BERG METRAL connectors are used to bring the signals on to the CPMs via the backplane edge to ease the removal of modules for maintenance, etc.

3.2 ROD Prototype Tests

For ROD prototype testing, the DSS module with the G-Link transmitter daughter card emulating the read-out logic on the CPM, and a S-link destination card receiving the processed and formatted data from the ROD, emulating the read-out buffer (ROB) function will be used in a test system as shown in figure 7.

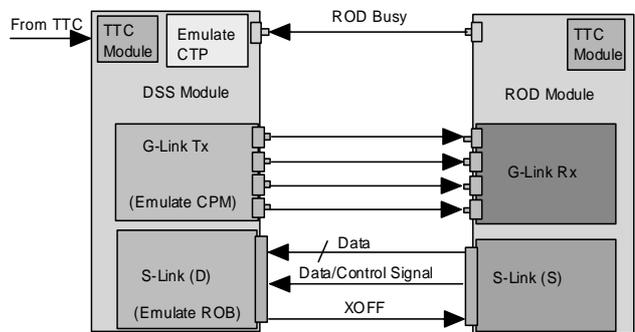


Figure 7. ROD Prototype Test Set-up

3.3 Prototype CP System Tests

Figure 8 shows a test set-up which will test the CP system. Here the DSS modules are used: (a) with LVDS serialiser daughter cards to emulate Pre-processor modules (PPMs), sending test patterns to the CPMs; (b) with S-Link destination daughter cards to emulate ROBs and the level-2 RoI builder module; (c) with LVDS parallel daughter cards to emulate the CTP, receiving the cluster-hit multiplicity from the hit counting modules.

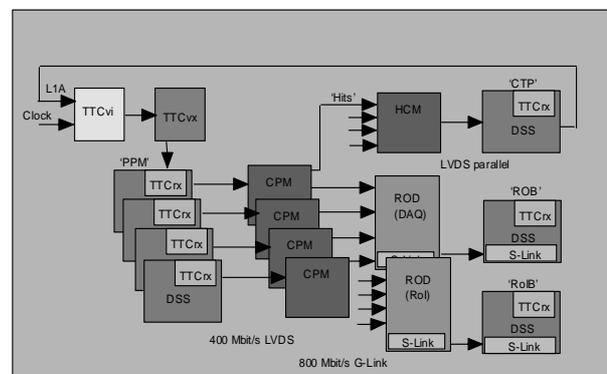


Figure 8. CPM Prototype Test Set-up

3.4 Other Applications

The DSS module can also be used for other applications. For example, clock sequencers and data acquisition modules with an appropriate FADC daughter card. Figure 9 shows a possible implementation of a CCD readout module using the DSS module. In this application one daughter card is used to generate the appropriate clock sequences to the CCDs and a second CMC daughter card is used to receive the analogue data and convert to digital, which can then be read out via the VME. A maximum of eight 10-bit ADCs should be possible on one CMC daughter card (80 bits per CMC card).

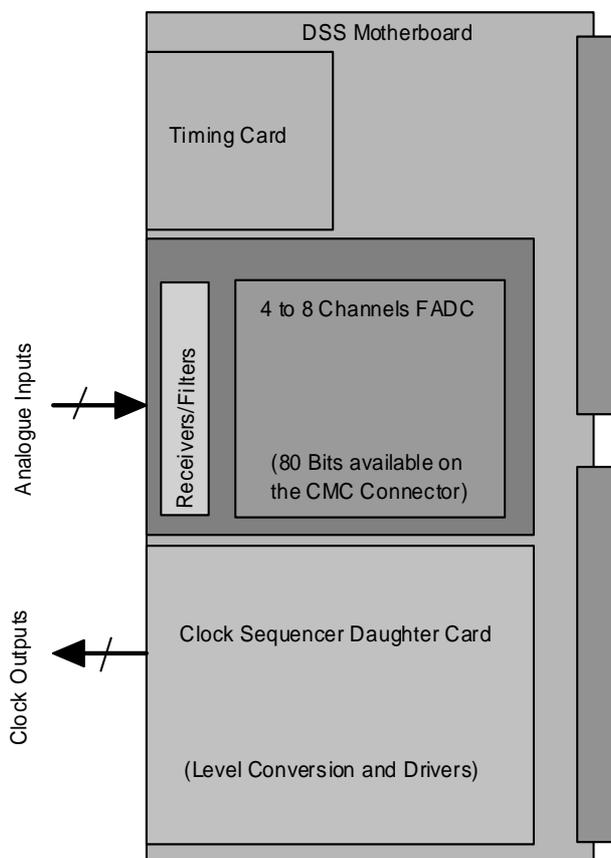


Figure 9. CCD Readout Module

4. SUMMARY AND CONCLUSIONS

We are now in a prototyping stage, and will soon move into designing, implementing and commissioning the final system in ATLAS. Prototypes represent the functionality of the final modules, with a smaller number of channels than in the final modules. To test these prototypes we require a source of data and a way of verifying the results from the prototypes. The DSS module we have designed with the motherboard and daughter card combinations is flexible and is reusable in many combinations, in testing the trigger prototypes, the pre-production and the production modules right through to commissioning and

maintaining the system in ATLAS. Also the DSS module with the appropriate daughter cards could have other applications other than for test data source and test data sink. The first use of the DSS will be to test the LVDS 480 Mbaud serial links. We will maintain a FPGA firmware library on the web that will contain various FPGA designs for the DSS module user [8].

5. REFERENCES

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- [5] Xilinx XC4000XLA data sheet: <http://www.xilinx.com/products/products.htm>
- [6] Low Cost Gigabit Rate Transmit/Receive Chip Set, Technical Data, Hewlett Packard.
- [7] 16-40 MHz 10 Bit Bus LVDS Serialiser and De-serialiser, National Semiconductor, September 1998.
- [8] Contact viraj.perera@rl.ac.uk for further information.