CMS CALORIMETER REGIONAL TRIGGER PROTOTYPES

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Abstract

The CMS calorimeter regional trigger system is designed to detect signatures of isolated and non-isolated electrons/photons, jets, missing and total transverse energy in a deadtimeless pipelined architecture. This system is comprised of nineteen crates of custom-built electronics. Prototype backplane, boards and ASICs built to validate this design are described here.

1. INTRODUCTION

The CMS detector for the Large Hadron Collider (LHC) presents an extraordinary challenge for its trigger and data acquisition system. Its trigger system must carefully sift the 40 MHz data to retain only interesting physics signals at 100 Hz level while discarding the well-known QCD background. The CMS solution to this problem is implemented in two physical levels, one based on custom electronics and the other relying upon commercial processors. The level-1 system uses only coarsely segmented data from calorimeter and muon detectors, while holding all the high resolution data in pipeline memories in the front-end electronics, to produce a trigger decision in 3 ms. Level-1 triggered events at 100 kHz rate are sifted further in higher levels of triggers implemented as software filters.

The CMS level 1 trigger decision is based in part upon local information from the level 1 calorimeter trigger about the presence of physics objects such as photons, electrons, and jets, as well as global sums of E_t and missing E_t (to find neutrinos). Each of these physics is required to pass a series of p_t or E_t thresholds, which are used in making the Level 1 Trigger Decision.

The electron/photon trigger is based on the recognition of a large and isolated energy deposit in the electromagnetic calorimeter by asking for a small hadronic energy deposit in the HCAL in the cluster region. There are different thresholds for inclusive electrons/photons, dileptons, and for very high E_t electrons. The isolation cuts are relaxed and finally eliminated for triggers with increasing E_t thresholds.

2. DESIGN OVERVIEW

The calorimeter level 1 trigger system receives digital trigger sums from the front-end electronics system, which transmits energy on an eight bit compressed scale. The data for two HCAL or ECAL trigger towers, for the same crossing, will be sent on a single link in eight bits apiece accompanied by five bits of error detection code and a 'fine-grain" bit characterizing the energies summed into the trigger towers (i.e. isolated energy for ECAL, quiet first longitudinal compartment for HCAL).

The calorimeter regional crate system uses 19 calorimeter processor crates covering the full detector. Eighteen crates are dedicated to the barrel and two endcaps. These crates are cover the region $|\eta|<3$. The remaining crate covers both Very Forward Calorimeters that extend missing E_T coverage to $|\eta|<5$.

Each calorimeter regional crate transmits to the calorimeter global trigger processor its sum E_t, E_X and E_y. It also sends its 4 highest-ranked isolated and non-isolated electrons, and 4 highest energy jets along with information about their location. The global calorimeter trigger then sums the energies and sorts the electrons and jets and forwards the top four calorimeter-wide electrons and jets, as well as the total calorimeter missing and sum E_t to the CMS global trigger.

The regional calorimeter trigger crate has a height of 9U and a depth approximately of 700mm[1]. The front section of the crate is designed to accommodate 280mm deep cards, leaving the major portion of the volume for 400mm deep rear mounted cards.

The majority of cards in the Calorimeter Level 1 Regional Processor Crates, encompassing three custom board designs, are dedicated to receiving and processing data from the calorimeter. There are seven rear mounted Receiver cards, seven front mounted Electron Isolation cards, and one front mounted Jet Summary card for a total of 15 processor cards per crate. These cards and an additional clock and control card are plugged into custom "backplane" which provides point-to-point links between the cards. VME bus is also provided to these cards using high density connectors in top 3U section of the backplane. In addition there are two slots with standard VME backplane connectors for crate processor and monitoring cards.

2.1 Receiver Card

The Receiver card is the largest board in the crate. It is 9U by 400mm. The rear side of the card receives the calorimeter data on serial copper cables, and converts from serial to parallel format. The front side of the card contains circuitry to synchronize the incoming data with the local clock, and check for data transmission errors. There are also lookup tables and adder blocks on the front. The

[1] J. Lackey et al., CMS Calorimeter Level 1 Trigger Conceptual Design, CMS TN/94-284 (1994), and an update in CMS NOTE-1998/074.

lookup tables translate the incoming information to transverse energy on several scales. They are also used to test for Quiet and Minimum Ionization thresholds for each trigger tower. The energy summation tree begins on these cards in order to reduce the amount of data forwarded on the backplane to the Jet Summary card. Separate cable connectors and buffering are also provided for inter-crate sharing.

Each card is designed to receive 32 high speed copper links from the calorimeter readout electronics. Each link transmits either two towers of hadronic or electromagnetic information per crossing for a total of 64 channels from 32 ECAL and 32 HCAL towers per card. The present design for the data uses a 24-bit frame including 18 bits of data and 5 bits of error detection code. The data consists of 8 bits of energy on a compressed scale and one bit of fine-grain information per tower. The error code is sufficient to detect all single and double bit errors as well as many multiple bit errors. The error bits are necessary for error logging and to zero problem channels. The 24-bit word uses 8/10 bit encoding, which implies a 1.2 GHz serial link. The cable length to the calorimeter electronics is estimated at 20 m.

The rear side of the Receiver card has serial receivers based on the specifications of the Vitesse 7214 4-channel Interconnect Chip. The design provides for cable/connector equalization and the option of transformer isolation on daughter cards.

The front side of the Receiver card contains the synchronization circuitry followed by the memory look up tables, adder tree and backplane drivers. The outputs of the receivers are not only unsynchronized with the local clock but are also not necessarily aligned to the same bunch crossing. The phase alignment circuitry is contained on an ASIC (Phase ASIC). The Phase ASIC deskews the data, decodes the error detection codes and multiplexes the output at 160 MHz. The Phase ASIC also provides test vectors for board and system diagnostics.

In order to achieve maximum utilization of board space, all the logic following and including the Phase ASIC is run at 160 MHz. There are also four Error Detection Codes (EDCs) associated with the four input channels of each Phase ASIC. After synchronization, each EDC is checked against the data. If an error is detected a single bit is set, one for each incoming channel, and appended to the original EDC code.

Lookup tables are required to translate the information coming from the calorimeter readout electronics, in compressed format, onto the several different scales used by the energy adder tree and the Electron Isolation logic. The Hadronic and Electromagnetic energies are individually translated into eight bits of linear E_T with a resolution of approximately 1 GeV. These values are summed to provide total energy in 4 x 4 trigger tower regions of the calorimeter. The summation is performed by an Adder ASIC. Thirty-two towers, in a 4 x 8 array,

are processed on each card. The transverse energy for each of the two 4 x 4 trigger tower regions is independently summed and forwarded to the Jet Summary card. These two 13 bit numbers will be multiplexed onto a single set of 13 differential pairs at 160 MHz.

The electron/photon finding algorithm itself is implemented in a separate card. The data required for this algorithm is transferred between the Receiver cards and the Electron Isolation cards at 160 MHz. In order to retain point to point transmission data must be transmitted through separate drivers on separate backplane lines. Every Receiver card shares its data with at most 6 Electron Isolation cards within the same crate. In addition each Receiver card sends some of its data off crate at 40 MHz to two or three neighboring crates. Crate to crate communication is handled by special cables running between the Receiver cards. This distributes the inter-crate buffering among the eight Receiver cards in a crate rather than attempting to put it all on one or two special cards at the ends of each crate.

2.2 Crate Backplane

The crate backplane is completely custom with a full 9U height. The top 3U is reserved for a 32 bit VME interface. The remaining 6U is used for the high speed data paths between individual cards. All signals in the trigger data portion of the backplane will be transmitted on point to point links at 160 MHz. This data rate was chosen because it offers the opportunity to compress the number of data lines on the backplane and in the pipelined data logic by a factor of four.

The front and rear insertion of cards in the data processing section of the crate was chosen to allow greater separation between cards and to provide a more protected environment for the links connected to the rear mounted Receiver cards. The increased separation will promote better cooling of the cards, and will enable a wider selection of front panel components.

2.3 Electron Identification Card

Electron Identification algorithm within each 4x8 trigger tower region is performed on a smaller 240mm deep card. Data for thirty-two central towers and twenty-eight neighboring towers is required to determine isolation for towers on the edge of the 4 x 8 region. This card receives linearized transverse energy on 7-bit scale for ECAL and 4-bit scale for HCAL and ECAL fine-grain bit from corresponding receiver card. It also receives neighbor tower data from up to three other receiver cards in the crate. Neighbor crate data is transferred through the receiver cards where it undergoes any realignment of phase. The algorithm which finds isolated and non-isolated electron/photon candidates is implemented in an ASIC. Candidate with highest E_T of both types in each of the two 4x4 regions covered by the card are transmitted to the Jet/Summary card.

2.4 Jet/Summary Card

Jet/Summary card receives 4x4 trigger tower energy sums from all Receiver cards in the crate and isolated and non-isolated electron/photon candidate energies from all Electron Identification cards in the crate. It sorts these candidates and forwards top 4 jets, isolated and non-isolated electron/photon candidates to the global calorimeter trigger crates on copper cables. In addition it also contains lookup tables to convert the 4x4 E_T to E_x and E_Y and adder trees to sum up crate wide sums of all three of these quantities.

3. PROTOTYPES

3.1 Work Accomplished

The goals of prototype development for this trigger system are many fold. Our strategy was to build as far as possible full-scale prototypes so that system issues are confronted up front. Pictures of rear and front views of the prototype crate holding prototype backplane and cards are shown in Figures 1 and 2.
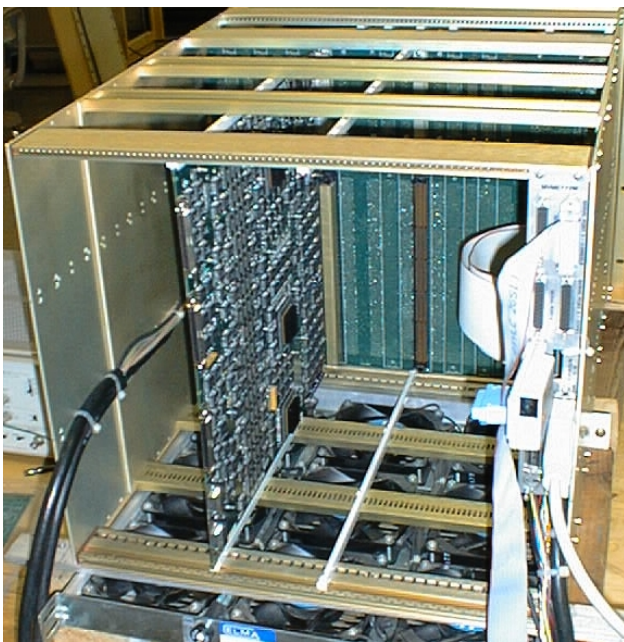

Figure 1: Rear view of prototype CMS calorimeter regional trigger crate showing the custom backplane and a receiver card.

To prove that high speed and high signal density can be handled, we have built a full sized backplane with point-to-point 160 MHz links and VME control. The backplane is a monolithic printed circuit board with front and back card connectors. The top 3U of the backplane holds 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The first two slots of the backplane use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pinout. Thus, a standard VME module can be inserted in the first two stations. The form factor conversion to the remaining slots is performed on the custom backplane. The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed controlled-impedance connector for both front and rear insertion. The design is based around a 340 pin connector, by AMP Inc., to handle the high volume of data transmitted from the Receiver cards to the Electron Isolation and Jet Summary Cards. There are 1419 differential 160 MHz point-to-point links on the backplane between the various cards. The backplane is constructed with five ground and power planes and five signal layers with the differential pairs held to the same layer.

We built a clock and control card to provide the necessary signals to drive other cards in the crate. The signals on even the longest links on this backplane preserve their characteristics well. Results from testing clock signals on the backplane show rise and fall times of 0.8 ns from 20% to 80% height with reasonable signal levels even when measured at the farthest card slot. This performance meets the requirements of 160 MHz operation of the backplane
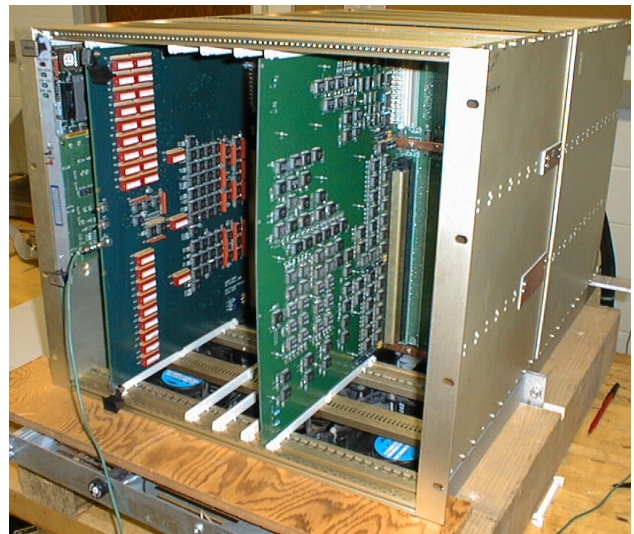

Figure 2: Front view of the prototype crate showing the clock and control and electron isolation cards plugged into the custom backplane.

The receiver card is by far the most complicated item in our design. We have built a full scale prototype of this card, shown in Figure 3, with large amount of ECL SRAM for lookup tables, support circuitry for three Adder ASICs needed on this card and drivers for all backplane lines. In order conserve the board space and to reduce power consumption, the production boards will combine various discrete components used to stage the data on into a multipurpose ASIC that also provides certain card Boundary Scan functionality. VME, Adder ASIC and

inter-crate data sharing circuitry on this card have been tested to function with adequate performance.
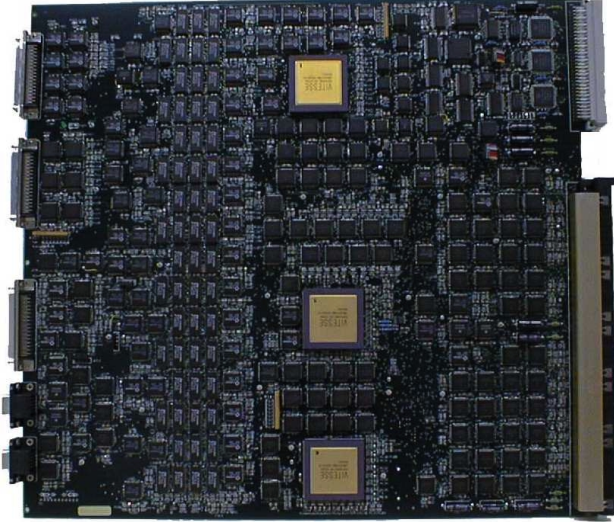

Figure 3: A picture of the front side of prototype receiver card showing the three Adder ASICs used for making 4x4 trigger tower sums used to find jets and determine missing E_T.

The Adder ASIC sums 8 signed 10-bit operands to a single signed 10-bit result at 160 MHz. We fabricated prototype adder ASICs which sums eight 10-bit signed numbers in a total of 4 25 ns clock-steps. These ASICs, built by Vitesse in 0.6 µ H-GaAs technology, chosen for its speed and ECL output capability, have been tested to work at 200 MHz, well above our specifications. The Adder ASIC consists of approximately 11,000 cells and uses 4 W. The tests of the Adder ASIC on the receiver card were successful so that we deemed this design of the Adder as final and are in the process of procuring production quantities.

3.2 Work in progress

The receiver card uses daughter cards mounted on its rear side to receive its input from calorimeter front-end crates. We have designed these daughter cards with serial link chips (Vitesse 7214) and associated signal equalization support. These circuits along and an independent test card are in fabrication. We plan to use these cards to test the feasibility of receiving data on 20 m long copper cables at 1.2 GHz.

Success of our Adder ASIC prompted us to select the same technology for making other ASICs in our system. We have made preliminary designs of Phase ASIC described above, Electron Identification ASIC, Boundary Scan/driver ASIC and Sort ASIC and have agreement with Vitesse to produce these ASICs. Detailed design work is now in progress.

We are also carrying over the knowledge gained in making the prototypes discussed here in designing final backplane and other cards. We are incorporating the refinements made to the electron finding algorithm that resulted in some changes in the dataflow. The Receiver card prototype prompted us to move most of the discrete logic, used on that card to stage data to EID and Jet cards, into the Boundary scan ASIC. Another change we made is to use on card DC-DC converters to distribute needed power at appropriate voltages.

4. SUMMARY

We have made several full scale prototypes of the CMS regional calorimeter trigger system. Successful evaluation of these prototypes has validated key elements of our design. We are in the process of evaluating serial link technology that is crucial for the feasibility of the system. Successful validation of tbe Adder ASIC on tbe prototype Receiver card has prompted us to begin design of all other ASICs required in our system. We have simulated the performance of this system using detailed Monte Carlo [2]. We believe that this system satisfies the CMS physics requirements, while meeting the bandwidth requirements imposed by the data acquisition system. This design with its extensive use of lookup tables has sufficient flexibility for tuning rates and optimizing efficiencies.

5. ACKNOWLEDGEMENTS

[2] S. Dasu et al., CMS calorimeter trigger detailed simulation, CMS NOTE-1998/027.