Irradiation and SPS Beam Tests of the Alice1LHCb Pixel Chip

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(For the ALICE collaboration)

Abstract

The Alice1LHCb front-end chip [1,2] has been designed for the ALICE pixel and the LHCb RICH detectors. It is fabricated in a commercial 0.25 μm CMOS technology, with special design techniques to obtain radiation tolerance. The chip has been irradiated with low energy protons and heavy ions, to determine the cross-section for Single Event Upsets (SEU), and with X-rays to evaluate the sensitivity to total ionising dose. We report the results of those measurements. We also report preliminary results of measurements done with 150 GeV pions at the CERN SPS.

I. INTRODUCTION

The aim of ALICE (A Large Ion Collider Experiment) is to study strongly interacting matter that is created by heavy ion collisions at LHC. The experiment is designed to handle particle multiplicities as high as 8000 per unit of rapidity at central rapidity. Therefore the innermost cylindrical layers need to be two-dimensional tracking detectors with a high granularity. The two innermost layers are made of ladders of hybrid silicon pixel assemblies (readout chips bump-bonded to silicon sensors) at radii 3.9 and 7.6 cm, respectively. A large part of the momentum region of interest for ALICE consists of hadrons with an energy of several hundred MeV, and the momentum and vertex resolution are dominated by multiple scattering. Therefore the amount of material in the acceptance must be minimised. A development is under way

to thin the pixel chip wafers, after bump deposition, to less 300μm. Sensor wafers of thickness 150 to 200 μm can be obtained in production. For the RICH detector of LHCb, the assembly will be encapsulated in a vacuum tube for the detection of the photoelectrons, and the thickness of the assembly is not relevant.

Since the pixel layers are very close to the interaction region, they need to be resistant to Total Ionising Dose (TID) effects and to Single Event Effects (SEE). The expected TID after 10 years of operation at LHC is 500 Krad. The effects of the TID are well known; threshold shifts, leakage currents, and charge mobility reduction as a result of trapped charge and interface states [3]. The SEEs originate from a large amount of charge being deposited by a single event, usually through an interaction of the incident hadron with the silicon atoms. This may lead to [3]:

- Single Event Upset (SEU): a change of a logic level ($0\rightarrow1$ or $1\rightarrow0$)
- Single Event Latch-up (SEL): a high power supply current
- Single Event Gate Rupture (SEGR): a breakdown of a transistor gate.

In this paper we focus on the application in ALICE, and describe tests of the Alice1LHCb pixel chip and of pixel single assembly prototypes, consisting of 300 μm p^+n sensors bump-bonded to pixel chips from wafers of 750 μm thickness.

The pixel front-end chip (Alice1LHCb) contains 8192 readout cells of each 425×50 μm^2 and measures 13.5×15.8 mm^2. It is designed in a 0.25 μm CMOS technology, where the radiation tolerance has been enhanced by the implementation of guard-rings and by using NMOS transistors in an enclosed geometry [4]. The measures that have been taken to reduce the effects of the TID also reduce the probability for Single Event Latch-up. Implementing redundancy for the memory cells in the chip reduces the effects of Single Event Upsets.

In this document, we outline first the performance of the chip, particularly in what concerns minimum threshold and noise, as derived from laboratory measurements. We then report the results of irradiation with x-rays (TID) as well as with heavy ions and 60MeV protons (SEE). Preliminary results of the measurements with singles assemblies in a 150 GeV pion beam at the CERN SPS are presented.

II. Minimum Threshold and Noise

Each pixel contains a capacitor for testing purposes. A voltage step over this capacitor injects a certain amount of charge into each pixel. For different settings of the global threshold the efficiency is measured as a function of the size of the applied voltage step. This gives a calibration of the global threshold in mV as is shown in figure 1. Using the known value of the test capacitor, and additionally by using the X-rays of a Fe^{55} source (which give rise to around 1600 electrons in 300 μm silicon) it is found that a threshold of 20 mV equals a threshold of about 1000 electrons.

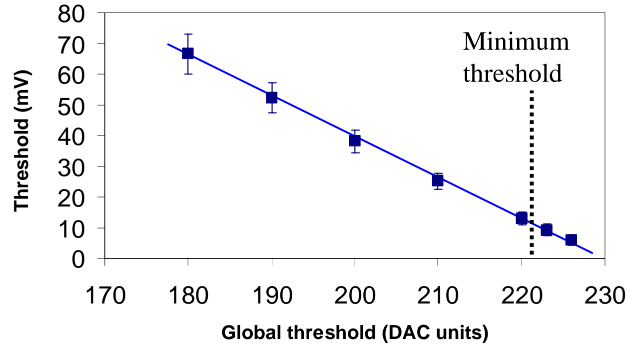

Figure 1: The measured average threshold of the pixel chip as a function of the setting of the DAC that is used to set the global threshold. A threshold of 20 mV is equivalent to about 1000 electrons.

The minimum threshold at which the chip can be operated is around 800 electrons. From the measurement of the efficiency as a function of the size of the voltage step, the noise (σ_{noise}) in each pixel was determined to be less than 110 Equivalent Noise Charge ($4\sigma_{noise}\approx$ difference in threshold when the efficiency is 2% and 98%, respectively). A pixel assembly has only a slightly higher noise (< 120 ENC), while the minimum threshold is around 1000 electrons.

III. Single Event Effects

A hadron with an energy of several GeV does not deposit enough charge through direct ionisation to create a Single Event Effect. However, it may interact elastically and in-elastically with the silicon atoms in the pixel chip. The recoils and fragments will deposit a large amount of charge in the chip, and may therefore lead to single event effects. Both SEGR and SEL are generally not observed for circuits designed in 0.25 μm with special layout techniques. For SEGR the electric fields are not high enough, while the implementation of guard rings prevent SEL to occur. During measurements on the Alice1LHCb chip neither SEGR nor SEL were observed. The SEU do however occur, and we have to measure the cross-section for a SEU in the memory cells of the pixel chip. The cross-section is determined in two different ways. Firstly heavy ions with an LET (Linear Energy Transfer) between 6 and 120 MeVmg^{-1}cm^2 were used, since these deposit a large amount of charge and the probability for SEU is large. From these results the SEU cross-section for other hadrons can be calculated. Secondly the measurements were repeated with 60 MeV protons.

A. Measurements with Ions

In order to vary the value of the LET, different ions can be chosen (Xe^{26+}, Ar^{8+}, Ne^{4+}, Kr^{17+}). Additionally the chip can be tilted with respect to the propagation direction of the ions to increase the path length of the ion through the sensitive part of the memory cells and therefore increase the amount of deposited charge in this region. To determine the number of SEUs the chip is loaded with a test pattern. After irradiation for a certain amount of time (several seconds or minutes) the memory cells are read-out and compared with the loaded test pattern. All differences are attributed to SEUs. It was verified that there are no SEUs without irradiation. The results of the measurements are shown in figure 2. For two pixel chips the SEU cross-section was measured. The results of these two chips are in good agreement. When the LET is larger than 6.3 $MeVmg^{-1}cm^2$, enough charge is deposited to create a SEU. Increasing the LET increases the SEU cross-section. At high values of the LET (> 20 $MeVmg^{-1}cm^2$) the cross-section increases slowly with increasing LET due to the fact that enough charge is available for a SEU, while only the probability to deposit the charge in the sensitive region of a memory cell remains. The curve in the figure represents the Weibull equation [5] that is used to estimate the cross-section for SEU in the case when the chip is irradiated with hadrons instead of ions. The data presented in figure 2 were used to determine the SEU cross-section for protons with an energy of 60 MeV, leading to 9×10^{-16} cm^2 [5].

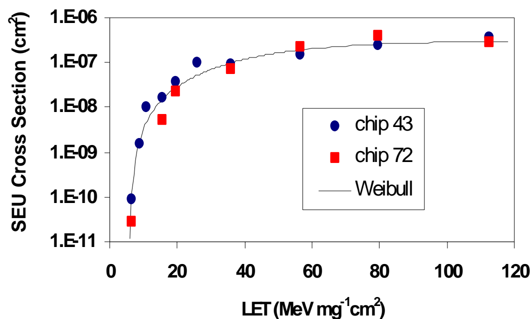

Figure 2: The SEU cross-section as a function of the LET (Linear Energy Transfer) for 2 different pixel chips. The curve represents the Weibull equation and is used for the interpretation of the data

A. Measurements with 60 MeV Protons

The SEU cross-section measurements were repeated with 60 MeV protons in order to confirm the heavy ion results. During 7 hours the chip was irradiated, leading to a fluency of 6.4 10^{12} cm^{-2}. The results of the measurements are summarised in table 1. In total 84 SEUs were found, while 41296 memory cells were irradiated. The SEU cross-section for 60 MeV protons equals thus 3×10^{-16} cm^2. This result is in good agreement with the result for 60 MeV protons as calculated from the heavy ion data (9×10^{-16} cm^2).

Table 1: Number of SEUs and the SEU cross-section per memory cell when irradiating with 60MeV protons.

Fluency (cm^{-2})	# SEUs -	# irradiated cells -	Cross-section (cm^2)
6.4 10^{12}	84	41296	3.2 10^{-16}

In order to obtain an estimate for the number of SEUs in the entire pixel detector of ALICE, the calculations which were performed for the CMS experiment [5] are scaled with the particle flux as expected for ALICE and with the SEU cross-section as measured with 60 MeV protons. The neutron flux in central Pb-Pb collisions at ALICE equals 6.4×10^4 $cm^{-2}s^{-1}$ [6] for the first pixel detector layer. The hadron flux originating from the Pb-Pb interactions was simulated using GEANT [7] and equals 2×10^5 $cm^{-2}s^{-1}$. For the entire ALICE pixel detector these particle fluxes would result in an upset rate of less than 1 bit of one digital to analogue converter every 10 hours. It can therefore be concluded that SEU do not form a threat for continuous operation of the ALICE pixel detector. As mentioned earlier, SEGR and SEL have not been observed during the measurements.

IV. Total Ionizing Dose Effects

The effect of the TID was studied by irradiating the pixel chip with 10 KeV X-rays from a SEIFERT X-ray generator, which is available at CERN. Due to the large size of the chip the irradiation had to be performed on two different positions on the chip in order to cover all the digital to analogue converters (DAC) located at the bottom of the chip, as well as a significant part of the pixel arrays. The bottom left and right (see figure 3) were irradiated to 12 Mrad at a rate of 0.6 Mrad/hour. Due to some overlap of the 2 irradiated regions some parts receive as much as 24 Mrad. The top part of the chip, i.e. rows 0-50, was not irradiated. Figure 3 shows the threshold map of the chip after irradiation. The determination of the threshold of each pixel is explained in section I.

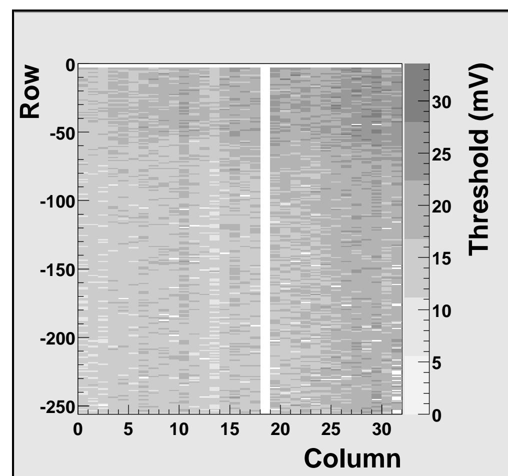

Figure 3: The threshold distribution of the chip after irradiation of the bottom right and left part of the chip to 12 Mrad.

After the irradiation the output voltages of the DACs of the chip were up to 40 mV lower than before due to the threshold shift in the PMOS transistors [8]. For this reason the chip was equipped with a reference DAC, which serves as reference for the other DACs in the chip. After the irradiation the voltage supplied by this reference DAC needed to be increased by 40 mV in order to obtain results as good as the results of the pixel chip before irradiation. There is no significant difference between the threshold map determined before and after the irradiation. The threshold for rows 0-50 is slightly higher, due to the fact that the reference DAC, as well as a two other DACs that control the digital part of the chip, were optimised for the irradiated pixels.

After the irradiation the minimum threshold at which the chip can operate is unchanged (800 electrons), while the noise per pixel is still below 110 ENC. The power consumption of the chip is unaffected by the irradiation and is shown as a function of the total dose in figure 4.

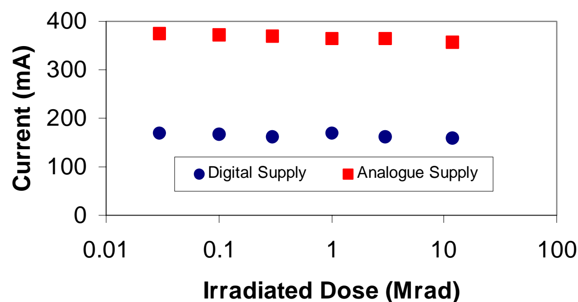

Figure 4: The current of the digital and analogue power supplies as a function of the TID.

V. TEST WITH 150 GEV PIONS AT CERN

A number of assemblies were tested in a beam of 150 GeV pions at the CERN SPS. Two different configurations were used. First, one pixel assembly was tested together with scintillators for triggering and efficiency determination (with an uncertainty of about 1%). At a later stage more pixel assemblies were added to be able to perform tracking and therefore improve the efficiency determination. The results given in this paper concern mainly the first configuration. The results from the extended configuration will be presented at a later stage. The efficiency was determined using four scintillators which select a small area, several mm^2, of the chip. An efficiency of 100% means that for each trigger there was a hit in our pixel assembly. First the efficiency was studied as a function of the strobe delay.

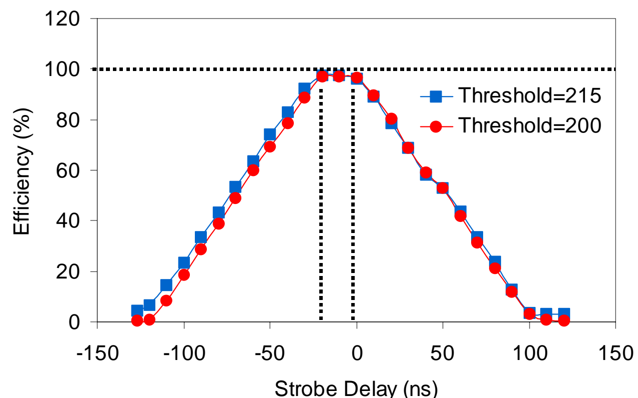

Figure 5: Efficiency as a function of strobe delay

The strobe is generated by the scintillator trigger signal and its duration could be varied for testing purposes from 100 to 200 ns. At the CERN SPS the particle bunches arrive randomly with respect to the 10 MHz clock of the chip. The strobe width was set at 120 ns, and the trigger delay was changed in steps of 8 ns. The results are shown in figure 5. Two different threshold settings were used, namely 200 and 215 which correspond to 2000 and 1000 electrons, respectively. The shape of the curve is as expected, and indicates a plateau of 20 ns. With a strobe width of 100 ns there would no plateau. There is no significant difference between the results for the different thresholds.

Furthermore the efficiency was studied as a function of the detector bias voltage. The results are shown in figure 6. These results show that the detector can be operated with full efficiency, over a large voltage range.

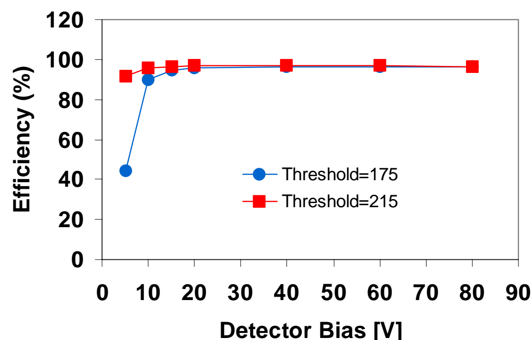

Figure 6: The efficiency as a function of detector bias voltage. The curve with a threshold setting of 175 (approximately 4000 electrons) is shown for illustration purposes only, the chip will be operated at a threshold setting around 215, corresponding to 1000 electrons.

Additionally the efficiency and cluster size was studied as a function of the incident angle of the particles. For this purpose the assembly could be tilted using a remote controlled

stepping motor. The results are shown in figures 7 and 8 for different thresholds. As mentioned before the chip will be operated with threshold settings in the range of 200-215, corresponding to 2000 to 1000 electrons, respectively.

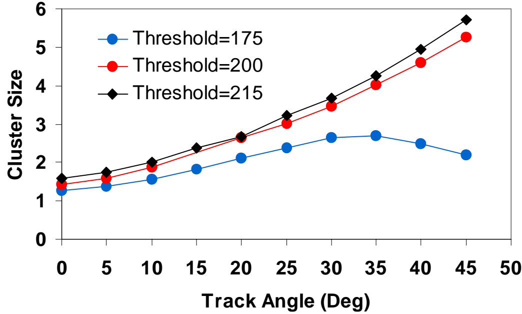

Figure 7: Cluster size as a function of the angle of the assembly. At zero degrees the substrate is perpendicular to the particle beam.

The data in figure 7 show an increase of the cluster size with increasing assembly angle. For very high thresholds the cluster size decreases as result of the decreasing charge deposition per cell when more cells are traversed. There is again no significant difference between the results with a threshold setting of 2000 and 1000 electrons.

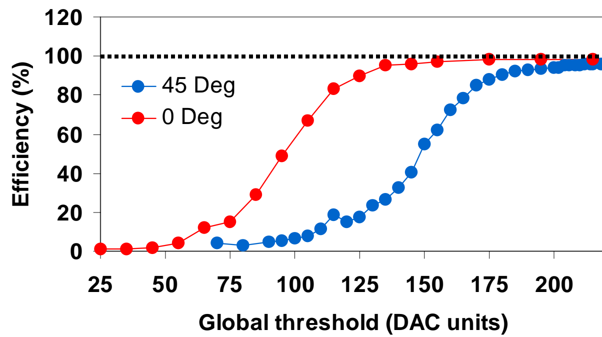

Figure 8: The efficiency as a function of the threshold setting for zero and 45 degrees.

The data in figure 8 show that the efficiency in the operation range (threshold setting between 200 and 215) is high, also at a substrate angle of 45 degrees.

VI. CONCLUSIONS

The Alice1LHCb pixel chip was successfully tested for total ionising dose and single event effects. It has been shown that the performance of the chip does not degrade after a total ionising dose of 12 Mrad. No SEGR and SEL were detected, while the SEU cross-section was determined to be small, (3×10^{-16} cm^2). This cross-section would lead to the upset of 1 bit per 10 hours, of one digital analogue converter of one chip for the complete ALICE pixel detector. The tests with 150 GeV pions show that the pixel assemblies perform well concerning the timing resolution, the efficiency and the cluster size.

VII. REFERENCES

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