Radiation test and application of FPGAs in the Atlas Level 1 Trigger.

V.Bocci[(1)], M. Carletti[(2)], G.Chiodi[(1)], E. Gennari[(1)], E.Petrolo[(1)], A.Salamon[(1)], R. Vari[(1)],S.Veneziano[(1)]

(1) INFN Roma, Dept. of Physics,
Università degli Studi di Roma "La Sapienza"
p.le Aldo Moro 2, 00185 Rome, Italy

(2) INFN Laboratori Nazionai Frascati,
Via Enrico Fermi 40, Frascati (Roma)

Abstract

The use of SRAM based FPGA can provide the benefits of re-programmability, in system programming, low cost and fast design cycle.

The single events upset (SEU) in the configuration SRAM due to radiation, change the design's function obliging the use in LHC environment only in the restricted area with low hadrons rate.

Since we expect in the Atlas muon barrel an integrated dose of 300 Rads and $5.65 \cdot 10^9$ hadrons/cm^2 in 10 years, it becomes possible to use these devices in the commercial version. SEU errors can be corrected online by reading-back the internal configurations and eventually by fast re-programming.

In the frame of the Atlas Level-1 muon trigger we measured for Xilinx Virtex devices and configuration FlashProm:

- The Total Ionizing (TI) dose to destroy the devices;
- Single Event Upset (SEU) cross section for logic and program cell;
- An upper limit for Latch-Up (LU) event.

With the expected SEU rate calculated for our environment we found a solution to correct online the errors.

System Description

The Atlas level-1 muon trigger [1],[7] is based on dedicated, fast and finely segmented muon detectors (RPC).

The system is segmented in 832 trigger and readout modules (PAD) and 832 splitter modules used to fan-out the FE signals located in the RPC zones.

The main components of the PAD are:

- The four coincidence matrix chip (CM)
- The Pad logic chip (PL)
- The fieldbus interface based on CANBus ELMB
- The optical link.

The CM chip selects muon with predefined transverse momentum using fast coincidence between strips of different planes.

The data from two adjacent CM in the η projection and the data from the two corresponding CM chip in the

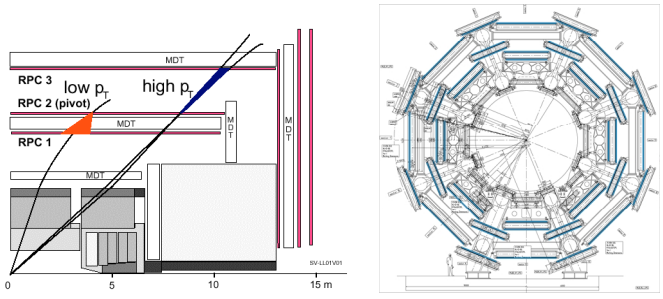

Figure 1. RPC location in the Atlas experiment.

ϕ projection are combined in the Pad Logic (PL) chip. After the measurements of the characteristic of FPGA devices in a radiation environment, we decided to use for the Pad Logic chip. Pad logic chip, covers a region $\Delta\eta x\Delta\phi = 0.2x0.2$, associates muon candidates with a region $\Delta\eta x\Delta\phi = 0.1x0.1$

(RoI). It selects the higher triggered track in the Pad solves overlap inside the Pad and performs the readout of the CM matrix data.

I. Radiation Environment

The radiation dose accumulated on the muon spectrometer depends from the zone. The simulated radiation levels [2] for ten years of operation of the Atlas muon detectors for various RPC chamber without safety factor is given in table 1. The

Table 1: Table 1: Simulated radiation environment in ten years of operation

	SRL_{tid} (Gy $10y^{-1}$)	SRL_{see} (>20 MeV h cm^{-2} $10y^{-1}$)
BMF	3.02E+00	4.69E+09
BML	3.04E+00	5.65E+09
BMS	3.03E+00	4.73E+09
BOF	1.19E+00	4.08E+09
BOL	1.33E+00	4.21E+09
BOS	1.26E+00	4.10E+09

simulated maximum value over 10 years of operation for TID (Total Ionizing Dose) is 3.04 Gy (304 Rad) and a total flux of $5.65 \cdot 10^9$ hadrons.

II. Xilinx Virtex and Flashprom Architecture.

The Xilinx Virtex devices [3] have a regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs).

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. The VersaRing I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking. The configuration of each CLB and IOB and the interconnection between different elements is programmed using a substrate of SRAM cells. The Virtex devices are custom built by loading configuration data into these internal SRAM cells. The numbers of configuration flip-flop exceed the number of logic flip-flops inside CLB and IOB of one order of magnitude.

In the master and selectmap mode it is possible to program the Virtex using an external nonvolatile memory with programmed inside the custom built design.

The 18v02 memory devices are using CMOS FLASH process for memory cell. The Flash process leaves the possibility to reprogram the device and appear to be resistant to SEU and TID. The high data bandwidth between the Flashprom and the Virtex device give the possibility to reprogram the FPGA in few milliseconds.

III. SEE Test at the CYClotron of LOuvain-la-NEuve

A. Measure of logic Flip/Flop hadrons cross section.

The XCV200 Xilinx Virtex FPGA and the 18v02 Flashprom [4] were irradiated with 60 MeV protons at the CYClotron of LOuvain-la-NEuve (CYCLONE) of theUniversité Catholique de Louvain, in Belgium. To perform such irradiation a special prototype board containing a XCV200 and a flashprom 18v02 were used (Figure 3).

The main purpose was to study SEE effects on the logic flip-flops in the configuration area and in the flash memory.

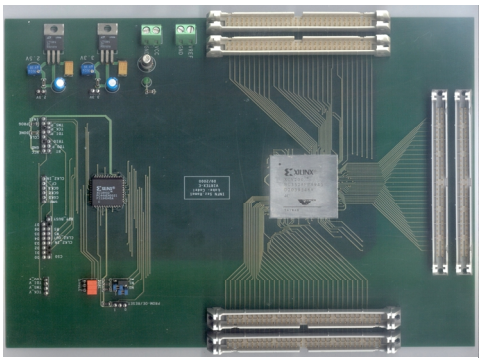

Figure 3. XCV200 Bga352 prototype board.

The Virtex was programmed (Figure 4.) with a 2048 bits circular shift register at the reset loaded with a 1010…10 pattern.
A very small part of the logic was dedicated to correct SEU errors and do detect such type of events
The circular shift circuit is very sensitive to SEU in the program area any break in the flips-flops chain stop the regular function.

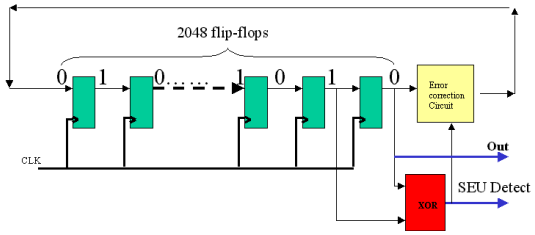

Figure 4. The circular shift register circuit used to determine the flip-flops logic cross section.

Two devices were programmed with this circuit and clocked using a 40 MHz clock. After an exposition to

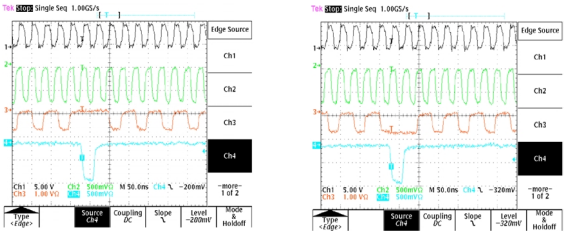

Figure 5. SEU events in logic flip-flops. Zero to One transition and one to zero transition.

$6.14 \cdot 10^{10}$ protons/cm^2 we observed five SEU events like Figure 5 and 23 events like figure 6.

The signature of events in Figure 5 is typical of a logic

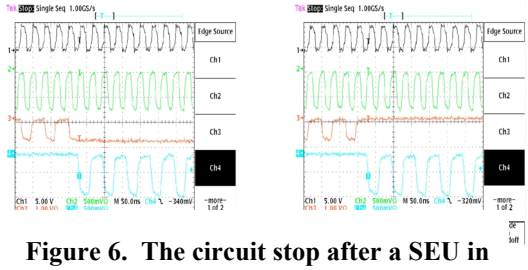

Figure 6. The circuit stop after a SEU in the program area.

flips-flops SEU instead the Figure 6 events shown a stop in the normal behavioral of the circuit caused from an error in the Virtex program. From this test the logic flip-flop Xsection/bit=$3.98*10^{-14}$cm^2.

No Latch-up events were observed.

B. Measure of SEUs in the Flashprom.

A total fluence of $8 \cdot 10^{11}$ protons/cm^2 was divided among four 18v02 2 Mbit flashprom devices. No SEU was observed with a limit for the Xsection/bit < $6 * 10^{-19}$ cm^2.

At about $2*10^{11}$ protons (corresponding to a total dose of 28 Krad for protons of 60 Mev in silicon) the programming feature stop to work.

C. Measures of SEUs in the Virtex program memory.

Two devices were programmed with the circular shift register and irradiated with the 60 Mev protons beam.

We perform a read back of the device using the fast selectmap mode. We do the comparison between the read-back stream and the original one, masking the meaningless bit as specified from xilinx documentation [5].

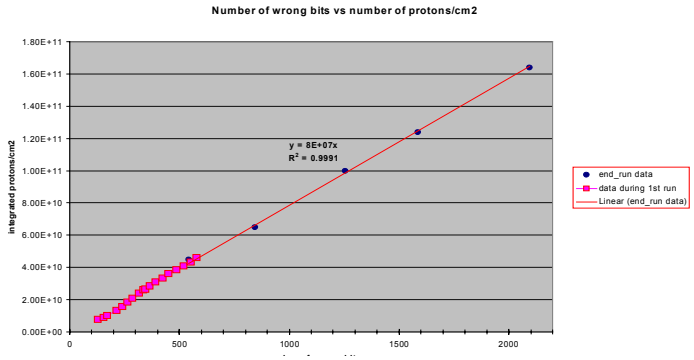

Figure 7. Total fluence vs numbers of bits corrupted.

For each run we accumulate thousands of bits error to have enough statistic. The results of various runs are shown in the Figure 7.

The results were compatible with a Xsection of $1.25 \cdot 10^{-8}$ cm^2 per device that correspond at Xsection/bit of $1.25 \cdot 10^{-14}$

A total fluence $5.44 \cdot 10^{11}$ protons was divided among 2 devices. We collect one event with an architectural break (wrong response from the read-back engine) the error was recovered after a reset.

No Latch up was observed.

IV. TID (TOTAL IONIZING DOSE) TEST WITH A ^{60}CO GAMMA RAY SOURCE.

We use for the total ionizing dose the ^{60}Co source in the Istituto Superiore di Sanita' in Rome.

The source gives a rate of 380 Rad/min.

A. TID effects in Virtex FPGA

We tested tree devices, the first and the second device were loaded with the circular shifter register instead the third one was used to test the Xilinx without a loaded configuration

Table 2.

	Xilinx1	
TID	**operation**	**current**
0 Krad	readback ok	40 ma
0 Krad	circuit wok	10ma
73 Krad	readback ok	40 ma
73 Krad	circuit wok	10 ma
83 Krad	circuit wok	10 ma
83 Krad	readback no working	150 mA

during communication with jtag tap.

The Tables 2,3,4 shows the data log of the currents sinked from the devices.

The first device (xilinx1) worked correctly up to 73 Krad, including a reconfiguration and read-back, the circuit continue to work up to 83 Krad but at this value was impossible to reprogram the device. We note a strong increment of the current 150 mA instead of the 40 mA.

The second device (xilinx2) worked correctly up to 65 Krad but we note a factor two in the sinked current, 80 mA instead of 40 mA,. The device stopped to work at 72 Krad with the same behavioral of xilinx1.

Table 2.

	Xilinx2	
TID	**operation**	**current**
0 Krad	readback ok	40 ma
65 Krad	circuit wok	10ma
65 Krad	readback ok	80 ma
72 Krad	circuit wok	10 ma
72 Krad	readback no working	150 mA

In the xilinx3 we monitored only the current of the device during the communication with the jtag interface without configure the device.

This current was stable up to 92 Krad then started to increase slowly, at 112 Krad was impossible to communicate with the jtag machine and the device stopped to work.

Table 3.

	Xilinx3	
TID	**operation**	**current**
0 Krad	readback ok	35 ma
92 Krad	the current start increasing	37 ma
112 Krad	the jtag does not work	45 ma

All the devices work without any problem up to 60 Krad.

The Atlas requirement for the RPC zone is 4.2 Krad, that include a 20 safety factor. The device meets very well the requirement.

B. TID effects in the 18v02 Flashprom .

Two 18v02 flashprom were tested.

The behavioral of the two devices was very similar and shown in the figure 8.

The current sinked from the device start to increase at 20 Krad at the 33 Krad was impossible to reprogram the device.

Also in this case the device meet the Atlas requirements.

The device stop to work with a total dose of 33 Krad in this value is similar with our measurements with protons (28 Krad).

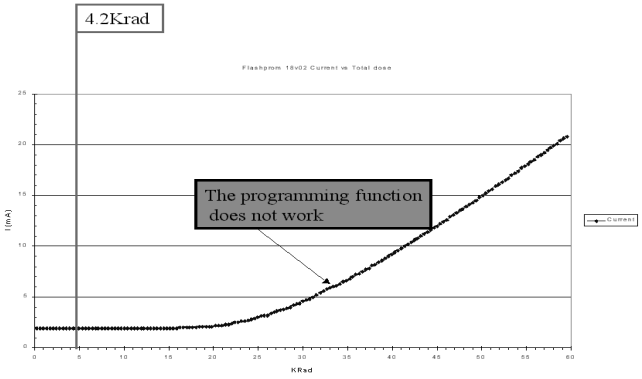

Figure 8. Current vs total dose for a 18v02 Flashprom.

V. ANNEALING AFTER IRRADIATION WITH ^{60}CO GAMMA RAY SOURCE.

After the irradiation we put all the devices inside an oven at 100 ^{0}C. We log the current sinked from any device.

The xilinx after 12 hours of annealing restarted to work correctly we note a big jump in the current reversing exactly our TID measurements Figure 9.

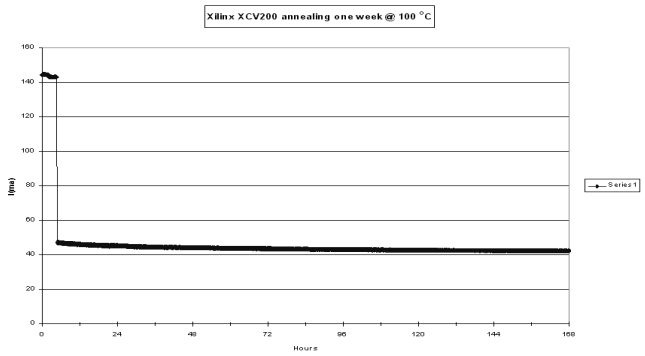

Figure 9. current sinked from xcv200 during the annealing.

The flashprom restarted to work after few hours and after one day returns at the normal current Figure 10.

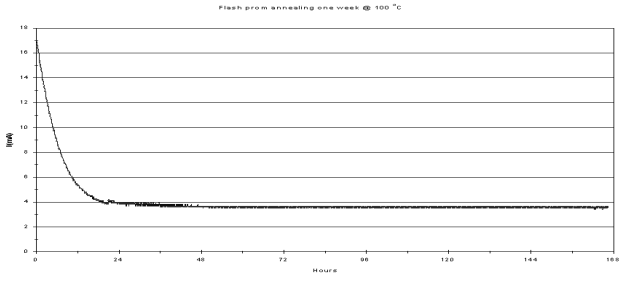

Figure 10. current sinked from the 18v02 flashprom during the annealing.

All the devices working well after the annealing and the process seem to delete any effects of TID.

VI. THE FPGA SUBSYSTEM.

After the resuts coming from the test we decide to implement the pad logic using a subsystem based on a Virtex FPGA, two Flashroms and a microcontroller is used to download and read back the Virtex configuration.

The system is checked by a simple task running in the ELMB CANbus microcontroller [6], capable of accessing these devices via the ISP and JTAGbuses (Figure 11.).

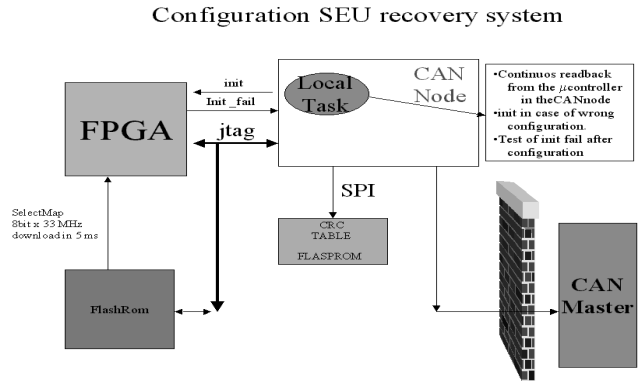

Figure 11. FPGA subsystem to recover SEU in program area.

The system reads back continuously frame by frame the configuration inside the Xilinx using JTAG and checks the consistency for each frame with a precalculated CRC value stored in the SPI Flashrom (Figura 14). In case of error the

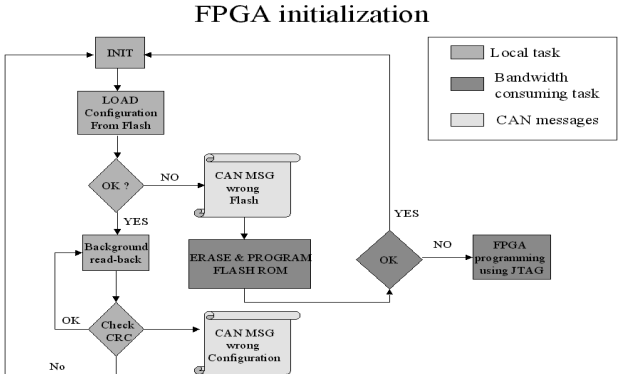

Figure 14. Flow chart of the FPGA initialisation and check process.

microcontroller rewrites part of the configuration correcting the wrong frame or reload the entire configuration.

In the Atlas radiation environment with the $X_{sect}=1.25*10^{-8}$ cm^2 and a flux of $5.65*10^9$ hadrons/10 years we aspect 6.25 SEUs in one year

Using the ATLAS safety factors $SF_{sim}=5$ for the simulation uncertainty and $SF_{lot}=4$ for the chip lot uncertainty we have SEU with $SF=6.25*5(SF_{sim})*4(SF_{lot})=125$ in one year.

VII. CONCLUSIONS

The XCV200 Xilinx Virtex FPGA and 18v02 Xilinx Flashprom were irradiated with protons and gamma ray. The SEU logic cross section is similar to other devices with 0.25µm technology.

For the Xilinx Virtex XCV200 the measured logic Xsection/bit= $3.98*10^{-14}cm^2$ and the measured configuration Xsection/device= $1.25*10^{-8}$ cm^2.

The 18v02 Flashprom Xsection/bit < $6 * 10^{-19}$ cm^2.

The SEU coming from the configuration memory get worse the problem of one order of magnitude respect to the pure Asic design. The TID tolerance is more than Atlas LVL1 maximum requirements 4.2 Krad . All the XCV200 tested devices worked without problem up to 60 Krad.

The 18v02 Flashprom program feature work up to 30 Krad and the device steel work at 100 Krad.

The immunity of Flashprom technology to SEU can be used for fast reprogramming of Xilinx configuration on board. The availability of CPU power from DCS node can be used to continuously check the Xilinx program.

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