Low Dose Rate Effects And Ionization Radiation Tolerance Of The Atlas Tracker Front-End Electronics.

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Abstract

Ionization damage has been investigated in the IC designed for the readout of the detectors in the Semiconductor Tracker (SCT) of the ATLAS experiment at the LHC, the ABCD chip. The technology used in the fabrication has been found to be free from Low Dose Rate Effects which facilitates the studies of the radiation hardness of the chips.

Other experiments have been done on individual transistors in order to study the effects of temperature and annealing, and to get quantitative information and a better understanding of these mechanisms. With this information, suitable irradiation experiments have been designed for the chips to obtain a better answer about the survivability of these chips in the real conditions of the ATLAS detector.

I. INTRODUCTION

The specific characteristics of the silicon detectors to be used in the Inner Detector of the ATLAS experiment that will be installed in the Large Hadron Collider (LHC) at CERN, together with the large amount of data required to be processed in a very short period of time, force the 'front-end' electronics designed to do this job to be placed very close to the actual detectors. This means, in fact, that the ICs for the immediate data acquisition and pre-processing of the signals coming from the detectors will be working in the active area of the experiment, very close to the collision point. The ICs will, therefore, be operated in a very harsh environment due to the amount of radiation in that area.

For this reason, radiation-hard microelectronic technologies have to be used, and the radiation hardness of the ICs should be verified previous to the installation in the experiment. This is the framework of this work, in which the radiation hardness of the two bipolar microelectronic technologies that have been proposed for the experiment is being evaluated, and the total ionization radiation damage expected for the ICs measured.

A basic approach to test the radiation hardness of the ICs designed for the experiment is, in principle, to irradiate them in a short period of time up to the total dose expected in the real case, and then measure their performance to see if their parameters remain within specs. The problem, however, is usually not so straightforward. In the last years it has been reported that bipolar transistors can suffer more radiation damage when irradiated at low rates than when irradiated at high rates [1], [2]. This means that an irradiation experiment done at higher dose rates than the actual rate can underestimate the damage. These phenomena are called Low Dose Rate Effects (LDRE) of the bipolar transistors.

Therefore, a more conservative approach for the test would be to irradiate the chips in the real conditions of the experiment. Then we would have the damage in the real case. But this possibility, though achievable in some particular cases due to the lower doses involved, is not realistic in the majority of the high energy physics or astrophysics applications, in which the long term operations of the experiments lead to high energy depositions during the whole life of the experiment but still at very low dose rates.

This is the case of the ATLAS experiment which is intended to operate for 10 years with a total expected energy deposition (considering the stopping periods) of 10 Mrads(SiO2), but at a dose rate of 0.05 rads(SiO2)/s [3]. In these circumstances an experiment to check the radiation hardness of the chips in the real conditions would take approximately 6.5 years which is not practical.

Many different approaches have been tried to test dose rate effects on a bipolar technology, and late studies have shown that high temperature irradiations at high dose rates can mimic the effects of low dose rate irradiations [4]-[6], but no one approach has yet been presented which covers all the possibilities and, therefore, there is still a lack of a universal hardness assurance approach for bipolar technologies. Nevertheless, it has been seen that these effects are strongly technology dependent which means that, in many cases, some devices will not suffer from LDRE for the particular conditions of the experiment. In such cases the first approach described above could be used for hardness assurance studies, avoiding a lot of trouble in complicated and long term LDRE studies.

In this work, the ionization radiation hardness of the IC designed for the front-end readout of the detectors of the ATLAS-SCT (ABCD chip) is evaluated taking into account the possible presence of Low Dose Rate Effect in the technology (DMILL).

II. TESTING PLAN

Four experiments have been devised in order to study the LDRE in the DMILL technology and the ionization damage characteristics on it:

i) Experiment 0, the sensitivity to LDRE of both technologies is evaluated irradiating test structures at a wide range of dose rates, but only to a dose that is reasonably achievable at the interesting low rates, 1 Mrad in our case.

ii) Experiment A, after evaluating the sensitivity of these technologies to LDRE, the actual value of these effects is measured for the total dose of interest, and the final damage on the transistors measured for the full total dose at the dose rate of interest.

iii) Experiment B, the test structures are irradiated at a high rate up to the total dose of interest and at different temperatures in order to identify an appropriate temperature (optimum temperature) for the accelerated tests which best mimics the damage produced at a low rate irradiation.

iv) Experiment C, Accelerated tests are carried out on the ICs at high dose rate and up to the total dose of interest using the optimum temperature if necessary.

III. EXPERIMENTAL PROCEDURES

All irradiations have been done using three different Co60 sources which provide 1.2 and 1.3 MeV gamma radiation which is widely used in ionization damage studies. A Pb+Al shielding box has been used together with geometrical considerations in order to avoid dose enhancement effects according to standards [7], [8], guaranteeing less than a 20% systematic error in the dosimetry. Thermoluminiscent devices (TLD) have been used, also according to standards [9], in order to identify the irradiation positions for the different dose rates, obtaining a statistical deviation of less than a 5%. The devices were kept biased during irradiation in order to be closer to the real life conditions and low mass materials have been used for the supporting boards. The temperature control has been provided via resistive tape heaters and liquid cooling for actuators. Thermocouples and Resistance Temperature Detectors (RTD) in physical contact to the chips were used for the measurements.

The Gummel Plots and common emitter current gains (β) of the transistors have been extracted before and after irradiation. Consecutive measurements have been made on every transistor, right after the irradiation, and for several weeks later until the annealing process has been completed. Two main parameters have been used to characterize the damage produced by radiation [9]: the excess base current density (ΔJb), defined as the difference between the base current density before and after irradiation at a base-emitter voltage of 0.7 V; and the relative beta change ($\Delta\beta\%$), defined as the difference in the common emitter current gain, at the same base-emitter voltage (0.7 V), before and after irradiation normalized to the one before irradiation. Temperature has been controlled during the measurements to make sure that it stays within a ± 2 °C margin. Still, a commonly used correction for small temperature differences has been used for the base current by applying a factor to the post irradiation value which is equal to the ratio between the pre and post irradiation value of the collector current (which is known not to be affected by radiation).

Test structures containing sets of bipolar transistors from the same technology in which the ABCD [10] chip is made have been used. Two different transistor sizes have been used for the irradiations and small differences have been seen between the radiation damage for each. The sizes of the transistors tested are 1.2 μm x 1.2 μm for the "minimum" transistor and 1.2 μm x 10 μm, for the, so called, "primary" transistor.

IV. EXPERIMENT 0: LDRE SENSITIVITY

The purpose of this experiment is to evaluate the sensitivity of the DMILL technology to LDRE. This first step is extremely important because it has been seen that LDRE are strongly technology-dependent, and in many cases a particular technology can be free of them or at least they might not show in the range of dose rates of interest of the experiment. In those cases tests of radiation damage can be done directly at high dose rates saving a lot of effort in complicated LDRE studies.

A first study of the annealing of the damage produced by the radiation from the moment just following the irradiation and the damage measured after a certain time has been carried out in order to be sure that these effects don't interfere with the effects produced by the low dose rates [11]. The results show that, in all the cases, he annealing, if it appears, is beneficial (the damage is reduced), stops after at most three weeks, and can not be accounted for the differences in the damage for different dose rates. In the following all the data points represents measurements taken at least three weeks after irradiation.

For this experiment the transistors have been irradiated at a very wide range of dose rates and all of them up to a total dose of 1 Mrad(SiO2) in order to obtain data even for the very low dose rates in a reasonable period of time. The dose rates chosen cover a range of 4 full decades and the values are: 0.05, 0.28, 1.33, 31.1, 112, 575 rads(SiO2)/s.
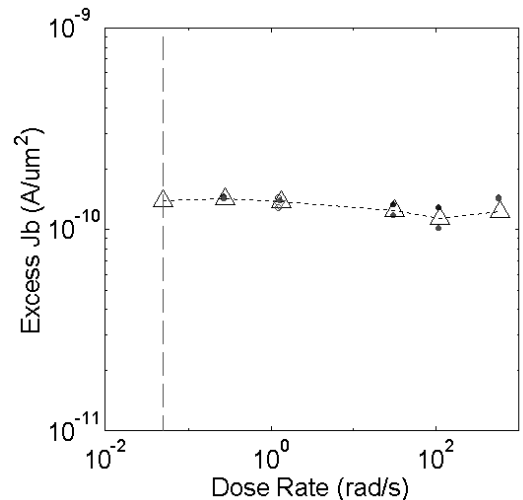

Figure 1: Excess base current density (ΔJb) versus dose rate for DMILL transistors from Experiment 0.
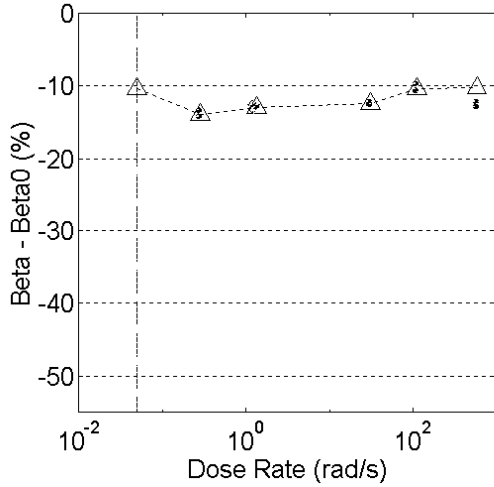
Figure 2: Relative beta change ($\Delta\beta\%$) versus dose rate for DMILL transistors from Experiment 0.

The results of this experiment are shown in Figure 1 and Figure 2 for the DMILL transistors, in which both excess base current density (ΔJb) and relative beta change ($\Delta\beta\%$) are shown versus dose rate, all for the same total dose of 1 Mrad. All the data points correspond to the final measurement after annealing has been completed. It can be seen that there is no evidence of low dose rate effects in these transistors, or it is negligible. Similar plots are shown in Fig. 3 and Fig. 4 for the CB2 transistors. It is clear in these plots that these transistors suffer total dose effects showing appreciably more damage at low dose rates.

V. EXPERIMENT A: MAPPING OF THE DAMAGE VS. TOTAL DOSE

In view of the results from Experiment 0, two main consequences can be obtained. The first one is that it is necessary to know if there are still no LDRE for the DMILL technology at higher doses; and the second one is that an estimation of the extent of these effects is necessary for the CB2 transistors.

For both of these measurements long term, low dose rate irradiations should be done up to the total 10 Mrads and at 0.05 r/s dose rate, which are the real conditions in ATLAS-SCT. These experiments are not realizable because they would take too long to give results. A solution to the problem is to map out the damage on the transistors vs. the total dose taking intermediate measurements of the damage for increasing total doses up to 10 Mrads. This way one can perform low dose rate irradiations up to a certain achievable total dose and estimate the damage at the final total dose by extrapolation. Furthermore, one can see if irradiations done at different dose rates lead to a "rigid" shift of the curves or, on the contrary, they change the shape or slope of them. If the curves suffer rigid shifts for different dose rates, we can be assured that the differences between low and high dose rate irradiations are maintained for high total doses.

The conditions of the four different mapping experiments that have been performed for this purpose can be seen in Table 1.

Table 1: Conditions of the four mapping experiments.

Exp#	Dose rate (r/s)	Total Doses (Mrads)									
1	112	1	3	5	7	10					
2	112	0.5	1								
3	1.24	1	1.4	2.2	2.4	3.2	5.2	6.2	6.8	7.8	
4	0.05	0.06	0.10	0.16	0.25	0.35	0.50	0.67	0.81	0.90	1.00

In Figure 3 and Figure 4 we can see the results of these experiments in terms of the excess base current density and the relative beta change. It can be seen that for all dose rates the excess base current density is linear vs. total dose for a logarithmic plot on both axis (dependency type: $\Delta Jb \propto (dose)^a$; a = constant). The relative beta change follows also a linear dependency with total dose but in this case for only a logarithmic abscissas axis (dependency type: $\Delta\beta \propto \log(dose)$). It also can be seen that the graphs for all four irradiations are parallel, and in fact superposed, meaning that the damage is the same for all transistors regardless of the dose rate and for the whole range of doses, indicating that there are no LDRE for these transistors up to 10 Mrads.
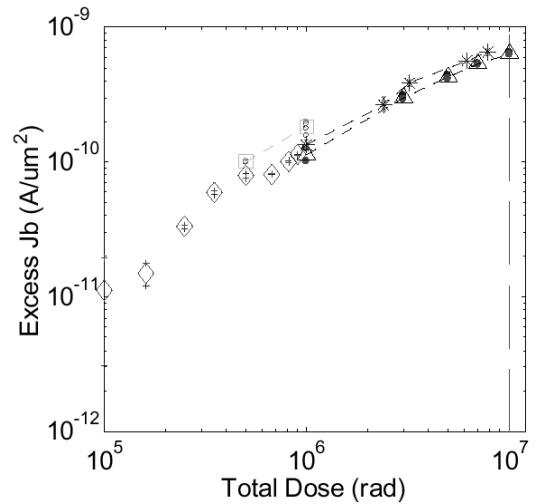

Figure 3: Excess base current density (ΔJb) versus dose rate for DMILL transistors from Experiment A.
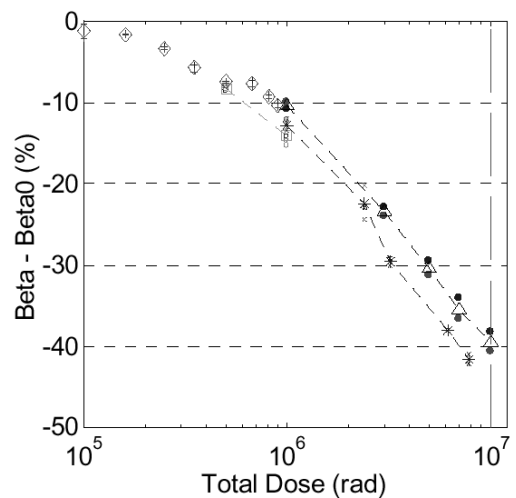

Figure 4: Relative beta change ($\Delta\beta\%$) versus dose rate for DMILL transistors from Experiment A.

The results show that the figures for the total ionization damage of the bipolar transistors of the DMILL technology are 8 x 10^{-10} A/cm^2 for the excess base current density and -45% for the beta change, giving a final value of the transistors current gain (for the emitter sizes used in the experiments) around 90 to 125.

VI.   EXPERIMENT B: TEMPERATURE

Given the fact that Experiment A has demonstrated that the DMILL technology doesn't suffer from LDRE at least up to the conditions of interest for ATLAS-SCT, it can be concluded that accelerated tests are not necessary for the hardness assurance testing of the ABCD chip. Therefore it is not necessary to find the optimum temperature for these irradiations, which was the initial goal of Experiment B.
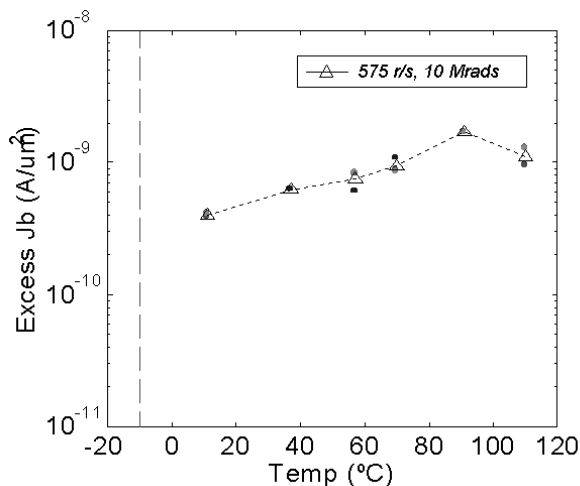

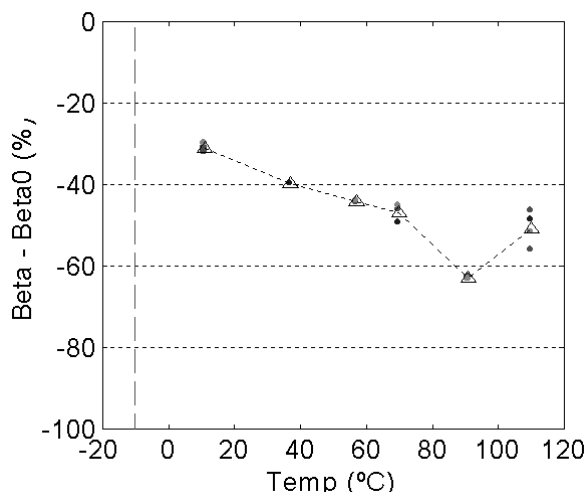Figure 5: Excess base current density (ΔJb) versus temperature for DMILL transistors from Experiment B.

Figure 6: Relative beta change ($\Delta\beta$%) versus temperature for DMILL transistors from Experiment B.

Nevertheless, a set of experiments at different temperatures has been carried out with the bipolar transistors of this technology in order to obtain the variations of the damage in the transistors for different temperatures of

irradiation. The actual working temperature of the chips in the real ATLAS-SCT environment is not as yet fixed, and a low optimum (worst case) temperature with a sharp slope in the damage at low temperatures would make the hardness assurance testing more difficult.

Different irradiations have been done of the bipolar transistors all of them up to the total ATLAS-SCT dose of 10 Mrads and at a very high dose rate (575 rads/s). The temperatures used in the study have been: 11, 37, 57, 70, 91, and 110 °C.

Figure 5 and Figure 6 show the results of Experiment B for the test structures of the DMILL technology. It can be seen that the worst case temperature appears at around 90 °C which is a high enough temperature for the slope to be smooth at low temperatures. Nevertheless, it can be seen that de different in the damage for an irradiation done at the expected actual working temperature of the ICs at the ATLAS-SCT (10 °C), and an irradiation at room temperature is appreciable, and should be taken into account in future irradiation tests of the ABCD chips.

VII.   EXPERIMENT C: FINAL TEST

The Results from Experiment A and Experiment B demonstrate that the DMILL technology is free from LDRE at the range of total doses and dose rates of interest in the ATLAS-SCT experiment, and that the difference in the damage for the actual operating temperature and room temperature is low. This results validates the previous high dose rate irradiation tests carried out by the collaboration with that result that the ABCD chip remains under specifications for the total life of operation [12].

Nevertheless, the actual ABCD chips have been irradiated in order to obtain the figure the damage produced on them by 10 Mrads of ionization radiation. The irradiations have been done at high dose rate (575 rads/s), up to the total dose of 10 Mrads and at room temperature. The results from these irradiations are currently being analyzed.

VIII.   CONCLUSION

The technology used in the fabrication of the ICs proposed for the front-end readout of the ATLAS-SCT (DMILL) has been tested for ionization damage and considering low dose rate effects. The results show that this technology, used in the fabrication of the ABCD chip, does not suffer from LDRE, or at least by a negligible amount. This result indicates that irradiations performed to test the radiation tolerance of the ICs can be done at high dose rates without underestimating the damage to the chips. This will save much effort in long term irradiations or accelerated tests.

The results also show that the variation of the damage produced on the chips for different irradiation temperatures are not very large for the range of low temperatures, but still should be considered if the chips are in the edge of their survivability after the irradiation tests.

Finally, the non-existence of LDRE in the DMILL technology validates and confirms the results of previous irradiation tests within the collaboration indicating that the

ABCD chip will remain under specifications after he 10 years of operation in the ATLAS-SCT environment.

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