DISTRIBUTED MODLAR RT-SYSTEMS FOR DETECTOR DAQ, TRIGGER AND CONTROL APPLICATIONS

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Abstract

Modular approach to development of Distributed Modular System Architecture for Detector Control, Data Acquisition and Trigger Data processing is proposed. Multilevel parallel-pipeline Model of Data Acquisition, Processing and Control is proposed and discussed. Multiprocessor Architecture with SCI-based Interconnections is proposed as good high-performance System for parallel-pipeline Data Processing. Tradition Network (Ethernet –100) can be used for Loading, Monitoring and Diagnostic purposes independent of basic Interconnections. The Modular cPCI –based Structures with High-speed Modular Interconnections are proposed for DAQ and Control Applications. Distributed Control RT-Systems. To construct the Effective (cost-performance) systems the same platform of Intel compatible processor board should be used.

Basic Computer Multiprocessor Nodes consist of high-power PC MB (Industrial Computer Systems), which interconnected by SCI modules and link to embedded microprocessor-based Sub-systems for Control Applications. Required number of Multiprocessor Nodes should be interconnected by SCI for Parallel-pipeline Data Processing in Real Time (according to the Multilevel Model) and link to RT-Systems for embedded Control.

Introduction

RT-Multiprocessor Systems should have scalable architecture for high-performance Data Acquisition, Trigger Processing and reliable Control in future
Experimental Physics. Multilevel Information Data-Flow Model for
RT-Systems in Experimental Physics Including DAQ, Trigger Data Processing and Control Applications are proposed and analysed. Modular Multiprocessor System Architectures with Scalable Open System (SOS) Architecture for System Area Networks (SAN) is discussed.

Information Model of data-fl0w in Experimental includes systems –
Data Acquisition (DAQ), Trigger Processing (TRIP) and Control systems
- all of them follow the needs and tasks of Front-end Electronics of Modern detector. There are 3-4 equivalent vertical levels of data processing in each system. The higher level the less data events volume and lower data event frequencies. High-speed Data flows on lower level of the Model require parallel data processing using many microprocessors.

A lot of Experimental Research Centres (including Physics and Medicine applications) require parallel computing with high-speed interconnections based on new SOS-Architecture for Distributed SAN Data Processing. Basic. Modular SAN-components are single-chip microprocessors on Nuclear structure level (N-module), which connect to SMP-architecture on the board on Atomic structure level (A-Module). A lot of A-modules interconnected as a node by Link modules (L-modules) on Macro structure level (M-modules). Basic Distributed systems organized in different topologies (Basic Ringlet, equidistant multiprocessor, 2-D and 3-D topologies).

One of the best approaches is to construct an effective (cost/performance) modular Multiprocessor system with flexible SCI-based Network Architecture. The advanced Scalable Open System (SOS) Network Architecture based on SCI link-modules and PC MB or PXI/cPCI modules for Distributed RT Systems, including DAQ, Trigger Data Processing and Control Applications in different fields are proposed and discussed. The Information Model of RT-Multiprocessor Scalable Modular Systems are based on parallel-pipeline Interconnections for Data Acquisition, Trigger and Control Data processing. It can be constructed (according to the multilevel Information Model) from a functional

single-chip multiprocessors on N-level, SMP-modules on A-level and macro-modules of basic structure components.

1. Multi-level Information Model of Data Flows in RT-system

The Multilevel Information Model of automated Complex in Experimental Area includes Data Acquisition and Control systems, based on existing standards. Proposed four-level Model includes parallel-pipeline Data Acquisition (DAQ) with reduction of data-flow from detector electronics. Data Reduction and Processing reduce event frequency (events selection) and volume of data on each level of the system. Reduction of data-flow (Volume, Frequency), Reconstruction and complex analysis of events in real time requires high-performance Multiprocessors working in real time (RT-systems). Experimental Area and Control Applications requires parallel Data Acquisition (DAQ), optimal control and distributed data processing according to requirements. All Interconnections between processor on any level of the Model require high-speed data transfer and parallel-pipeline data processing on the base of System oriented Network. Distributed parallel-pipeline data processing requires good scalability of high-performance multiprocessor systems according to Source Data Flow and topology of the experiment. Some subsystems monitor detector electronics and slow control equipment.

Data-Flow on each level of parallel data processing is reduced on events volume and frequency and can be appreciate as follows

$$DF(i) = I(i) * F(i),$$

where **I(i)** – Event Data Volume on i-level

F(i) – Frequency of Data Events on i-level

Data-Flow Volume on i-level will be

$$I(i) = Q(i) * I(i-1),$$

where **Q(i)** – Event Volume Reduction Coefficient on i-level of Data processing.

Event frequency on i-level will be

$$F(i) = R(i) * F(i-1),$$

where **R(i)** - Event Frequency Reduction Coefficient on i-level of Data Processing.

Event rate for LHC detector after the first level trigger is very high (100000 Hz).

Data Volume includes Inner Tracking (1 MB per 15 ns), calorimeter (200 Kbytes per 16 ns) and muon tracking, which are filtered by a second level trigger (in local segment data buffers and overall decision). The output event rate

F(1) = 100 kHz and F(2) = 1 kHz and F(3)= 100 Hz. . The Global decision takes 1 millisecond. The reduction coefficient should be R(2) = 100 and R(3) = 10.

Control Data Volume on i-level will be appreciate as

$$C(i) = K(i) * C(i-1),$$

where **C(i)** – is Control Data Volume on i-level of the information Model.

K(i) - is Control Data Reduction Coefficient on i-level of the Model

Effective Computer Control depends on Control Data Reduction and distribution this functions on subsystems. All subsystems should be connected in Integral

High-performance Distributed multiprocessor systems should be designed on the base of flexible System Area Network (SAN) Architecture for Scalable Open System (SOS) approach, using high-modular hardware and software, working in Compact Real Time (RT) Systems.

2. System Architectures for Parallel Data Processing

A lot of Computer Systems architecture for Distributed and Parallel Data Processing exist today, including Symmetrical Multiprocessing (SMP), Massively-Parallel Processing (MMP), Cluster Systems (RMC and NUMA).

A RMC (Reflecting Memory Cluster) is a clustered system with a memory replication or memory transfer mechanism between nodes and traffic interconnect. Some vendors use the term NUMA (Non Uniform Memory Access) to describe their RMC systems, others used term Shared-Memory Cluster (SMC) to describe NUMA and RMC nodes (can be easy confused with the shared memory inside SMP- nodes). The Term Global shared-memory system is not the best descriptor also. There are multiple memories (multiple memory maps) and OS, reflecting a portion of memory to one another.

Academic community sometimes uses the term “node” to refer to the small part of processors and memory section in a CC-NUMA systems, but commercial community not use this term because of the confusion with the definition of a cluster node. For example, the first developer of SCI systems Sequent names multi-quad system as a single-node, since only one instance of the OS is running over all quads. Correct terminology is

required also for describing of modern Scalable modular system. Structure Analysis and Synthesis of Scalable Computer Systems with Modular Structure in real time applications are one of the fundamental Problems in Computer Science. Following Sequence terminology clustered systems with two or more nodes (running a unique copy of the OS and applications), which share a common pool of storage simultaneously, is considered as a Single Computer System.

Scalable Coherent Interconnections (SCI) developed as one of the best System Area Network, because of bus limits a number of parallel processors in Distributed Data Processing systems.
A first attention to SCI-based Control System was given by author in DESY (Germany) and in KEK (JAPAN).
This paper proposed effective Scalable RT-System Development with high-modular structure for DAQ, Control and Distributed Data Processing. The system includes a Microstructure level of general purpose (Pentium-1,-2,-Pro) or specialize Microprocessors as a Computer Nuclear. On the Atomic structure level they are constructed on the board as standard A-Module of the system with 1 or more microprocessors. Functional A-Modules can be connected by bus interface, which limits a number of processor units on the same bus.

The first developer of SCI-based high-power modular multiprocessor system with hardware coherency (high-priced) was Sequent. Advanced Integrated RT-systems with Effective SOS-network Architecture on the base of standard Compact-PC modules or PC-board and Link-modules (Dolphin's communication modules) for effective cost/performance systems according to proposed multilevel Physical Model are discussed and analysed for Advanced DAQ, Control and Distributed Data Processing Applications. One of the best way to construct cost/performance RT-systems is to use PC MB, connected by System Area Networking with different topology according to application.

3. SAN-Architecture for Scalable Open System Multiprocessors

The Physics Model of Scalable Modular System includes multilevel parallel-pipeline Communications for multiprocessor open systems interactions working as a Big-Bus SMP system for users. Data Acquisition, Control and Data processing systems can be constructed as a multilevel system from a functional single- or multiprocessor modules (Atomic micro structure level of a system), including micro-modules of a Processor Chip (Nuclear structure level) on the board, connected by bus interconnections into the standard Macro-modules (Molecular macrostructure level). PC MB should be select for effective cost/performance RT-Systems. Required number of Distributed processor modules or macro-modules interact each other through Link-modules, bridges and switches on parallel-pipeline interconnections. RT-System can be constructed in required topology according to the application.

Success of modern Microelectronics Technology (up to 0,1 inch) opens new possibilities in Computer System Design in Y2K. Multilevel Physics Model of Distributed Systems is based on Conceptual requirements of Information Model and includes high-modular structure on all levels of the Model. Conceptual approach to the Structure of a system includes basic: Nuclear structure level (micro-module or chips), Atomic structure level (functional module in a standard boards) and Molecular structure level (Macro-module integrated in a PC MB, VME/VXI Crate, Compact PC or SCI). All high modular structure levels of Integrated System should support effective Interaction of distributed processor and memory modules with help of distributed link modules on the base of the conceptual approach to the Scalable System Area Network (SAN) Model development.

On Nuclear level of System Model micro-modules(**N –modules)** include single-chip general-purpose processor, memory, I/O controllers and communication.. Selection of the best type of Microprocessor depends on application requirements. Special- or general-purpose processor can be selected for different applications. For high-performance signal processing in real-time a Single- or Multiprocessor DSP with memory inside the chip can be used, but for effective (cost/power) DAQ, Control and Parallel Data Processing better to use modern compact general-purpose processors. Single-chip Microcomputer (processor with Memory in the chip) has shorter link, better access and data transfer time than out of chip on the same board, because it has shorter connections and cache of 1-st (and 2-nd level) inside the chip. Power Single-chip Multi-Processors is also reality today. New compatible L-modules for OEM developers produced by some companies include bridge Chips and Link Controllers. There are 4, 8 and 16 slot version of crates for Modular cPCI systems from Motorola, PEP Modular Computers, AdLink and PXI version for Modular Instrumental Systems from National Instruments Inc.

PCI-SCI Modular Bridge Chip (PSB) with a unique protocol converter suited for clustering and high-performance RT-System for DAQ and Trigger applications. The PSB-32 is designed to meet the requirements for high availability clustering and remote I/O applications. In a unique architecture combining both direct memory access (DMA) and remote memory access (RMA).

High performance message passing protocols and transparent bus bridging operations are supported. By using the DMA controller contents of memory can be copied directly between PCI buses in a single copy operation with no need for intermediate buffering in adapter cards or buffer memories. This feature greatly reduces latency and lowers overhead of data transfers. The DMA controller supports both read and write operations. The remote memory access (RMA) feature of the PSB enables ultra-low latency messaging
and low overhead and transparent I/O transfers. In RMA mode, PCI bus memory transactions are converted into corresponding SCI bus memory transactions allowing two physically separate PCI buses to appear as one. This feature allows applications to send data between system memories without using of operating system services, reducing latency and overhead. The PSB has built-in address translation, error detection and protection mechanisms to support highly reliable connections. The PSB chip is based on the ANSI/IEEE SCI-standard.

Basic parameters of Bridge chip:
- *PCI 2.1 compliant, 32 Bits, 33 MHz*
- *ANSI/IEEE 1596-1992 SCI standard*
- *Chaining (Read/Write) DMA Engine*
- *Up to 4096 map entries in SRAM*
- *512 Kbytes page size compatible*
- *Host bridge capability (PCI arbiter)*
- *B-Link™ Compliant Performance104 Mbytes/sec RMA, 73 Sec/sec DMA*

SCI Link Controller Chip (LC3, *compatible backwards with LC2*) is the first implementation of the Scalable Coherent Interface standard with duplex bandwidth of 800 Mbytes/s. The LC3
is targeted for use in a wide range of systems where high bandwidth combined with low latency is required. Typical target systems are computer clusters, tightly coupled parallel computers, high performance I/O systems and switches. The LC3 guarantees delivery of SCI packets with payloads up to 64 bytes of data. Internal buffers allow for pipelining of packets for high throughput operation, yet supports virtual cut-through routing for low latency access. The LC3 offers local high-speed bus performance characteristics, with LAN flexibility and scalability at a very competitive price. The chip uses high speed single-directional low voltage differential signaling, running on standard low cost cables to attain a 800 Mbytes/s (6.4 Gait/s) data transfer rate with routing latency as low as 70 ns. System scalability is accomplished through a high-speed backend interface (BXBAR™) with built-in switching capability allowing system growth to beyond 1000 nodes.

LC3 SCI Link Controller parameters:
- *ANSI/IEEE 1596-1992 SCI standard*
- *ANSI/IEEE Std 1596 LVDS Link*
- *ANSI/IEEE 1159.1 (JTAG) support*
- *BXBAR™ Crossbar switching*
- *800 Mbytes/s Duplex link bandwidth for high performance applications*
- *Virtual channel (VC) based buffer management*
- *Table-based packet routing supporting complex topologies*
- *Two-wire serial EEPROM interface*
- *Queuing structure capable of storing 15 requests and 15 responses*

Atomic structure level on the Processor Boards (**A-modules**) of the Model includes special-purpose (DSP) or general-purpose processor (PC MB), memory and I/O subsystem components. Typical examples are computer modules like VME/VXI, PXI/cPCI or modern Lita-PC Mother Board (MB). The simplest construction of effective Distributed Data Processing system for DAQ, Trigger and Control Application can be based on a compact PC MB with single, two (Dual) or four (Quad) microprocessors on the board.

Number of modules on the same bus is limited (up to 16). Symmetrical Multiprocessing (SMP) is basic Software Model for Multiprocessors. This is one of a best decision for Trigger subsystems modules.

A lot of A-Modules should be interconnected in similar SMP mode
in different distributed topologies according to real detector on the base
of San-architecture (using SCI). Embedded subsystem (A-module or
M-modules) on macro level used often for slow control and monitoring wit Ethernet10/100 interconnections.

Distributed SAN Interconnection level (L-, B- and S-type Modules) depends of communications requirements and link-modules parameters. The cost of communication speed decreases faster than the cost of pins and board space. Tradition communications are usually based on bus, but any practical solution would involve the use of packet-based signaling over many independent point-to-

point links, which eliminated the bus bottleneck problem, and introduced a new problem - how to maintain cache-coherence in the shared-memory model of system. Bus is used for up to 16-32 processor max on the same bus, but Scalable Coherent Interconnections (SCI) is good connection for SOS- architecture with many processors
in a single system for DAQ, Control, Parallel Data Processing and DB.
A wide range of application can cover the whole range from high-end multiprocessors to workstation cluster and LAN.

The distributed SCI-based SAN Architecture shares a 64-bit address space, where the high order 16 bits are used to rout packets to the appropriate node. System topology can be based on a simple ringlet, multi-ringlet, bridges or powerful switches for Parallel-pipeline communications between processors
and memory. Interconnection should
be based on Link modules (L-Modules)
or Switch modules (S-Modules). SCI
is based on point-to point connections
and supports transactions all processor modules at the same time. Commercial Dolphin's L-modules provide 800 Mbytes/s bi-directional SCI link effective transfer
of a large volumes of Distributed data. Application-to-application latency is small (2.3 micro second) and reduces the overhead of inter node control messages, leading to the best possible scalability for multi-node applications. Dolphin's S-Modules for System Area Networks provide 4 x 800 Mbytes/s duplex ports and 2 x 800 Mbytes/s duplex ports.

Internal Switch provides 1.28 Bytes bandwidth, port-to-port latency of 250 nanoseconds and dual fans for reliability. These parameters provide good interactions between distributed modules. Large Integrated Complex should be based on Bus-like SOS Networks architecture with distributed memory for effective DAQ, Trigger and Control in Distributed Data Processing. High-performance PXI/cPCI modules have mezanin interface for standard PMS-modules which be effective used for interconnections between systems components.

PMC-SCI Adapter Module is a general-purpose interface for connecting PMC based cPCI-systems through SCI links onto Integrated SAN-based RT-systems (for DAQ, Trigger and Control) with Memory-mapped Distributed data processing. The module can be utilized in different applications such as scalable interconnection of I/O, bus-to-bus bridging and computer clusters. Its 800 Mbytes/s bi-directional SCI link is good for moving large volumes of data. Small application-to-application latency (2.3 micro second) reduces the overhead of inter node control messages, leading to the best possible scalability for multi-node applications. SCI's performance is achieved by taking maximum advantage of fast point-to-point links, and bypassing the time consuming operating system calls and protocol software overhead found in traditional networking approaches. SCI provides hot-plug cable connections; and redundant SCI modules can be used to increase fault tolerance. It supports SCI ring and switch topologies. Large Multiprocessor clusters can be built using Dolphin's interconnect switches.

PCI-64 adapter Module opens effective way to build PC-based System Area Networks for Distributed data processing, clustering of computer and servers on the base of SCI. It has similar parameters as PMC PCI Module. PCI and VME configurations can be combined.

Basic Technical Parameters of PMC- PCI Module:

Link Speeds - 400 Mbytes/s
(800 Mbytes/s duplex)
SCI Standard - ANSI/IEEE 1596-1992
PMC Specification - PMC IEEE 1386.1 Standard, 32 and 64-bit,
33 MHz PCI Bus (rev. 2.1 170 Mbytes/sec operation).
Performance - Up to 170 Mbytes/sec throughputs, 2.3 microsecond latency
Power Consumption - Static: 5W,
- Dynamic: 6W
Cable Connection - Parallel STP Copper Cable (1-7,5m)
- Parallel Optical Link PAROLI-SCI (1-150m)
Topologies - Point-to-Point and Switch

Modular SCI Switch (MS-6E) with high data throughput and low message latency for SAN provides 4 x 800 Mbytes/s duplex user ports, 2 x 800 Mbytes/s duplex ports. Internal Switch provides 1.28 Bytes bandwidth, port-to-port latency of 250 nanoseconds,
dual fans for reliability and increased circuitry lifespan. Clusters are supported by hot plugging.MS-6E switch is a high-performance solution for System Area Networks and server clusters.

Cluster nodes connect through four duplex 400 Mbytes/s ports. For scalability to larger clusters, the MS-6E supports redundant expansion ports, which allow up to 12 switches to be cascaded for System Area Networks of up to 32 ports. The MS-

6E can also be configured as a standalone 6-port switch.

The SCI architecture is designed to grow to as many as 64k nodes, which leaves plenty of headroom for future expansion. The SCI Switch's "port fencing" feature guarantees that a node failure will not prevent the cluster from functioning. Hot-plug-gable ports allow the addition or removal of nodes without halting cluster applications.

The switch is built around open standards and supports the IEEE/ANSI SCI standard and adapter module for standard buses such as PCI and Sbus. The dual expansion ports provide highly reliable redundant links. Dual fans increase MTBF and circuitry life span. Cable Connection is based on Parallel STP Copper Cable up to 5m or Parallel Optical Link PAROLI-SCI up to 150m. It has compatibility with 19" racks for ease of mounting and auto- ranging power supply.

Macro-structures on Molecular level (M-modules) depends of system topology. A lot of Multiprocessor cPCI Crates as a nodes can be interconnect
by System Area Networks ("Big Bus" Interconnections) into a large (up to
a Kilo-Processor) systems to support Distributed Integrated RT-Systems for DAQ, Control and Data Processing Applications. A number of A-modules on the Bus is limited up to 16 (max 32) because of physics parameters and not good scalability. A set of A-Modules in single Crate or Multi-Crate systems is sectioned as a Macro-module of the System Model. Sectioning of modules are based on exist standard Compact PC, VME/VXI, PC MB or SCI. Multi-Crate systems are one of the way to construct big systems. Big Bus-like approach is used to develop System Area Networks (SAN). SCI is one of the best approach to Scalable Multiprocessor System Architecture with following advantages.

Interactions between modules within RT-system are based on small packet transfer with split transactions. There are **high interaction** of N-Nodes on shared memory resources (example direct access to memory in SMP systems), **weak interactions** between A-modules (example message passing
in MPP systems) and **intermediate interaction** on the base of external memory devices (disks, tapes in Clustered systems). High SCI interactions are based on small packet transactions (send and response packets with echo). Packet Formats include ***writexx, readxx, movexx*** and ***locksb*** commands, where ***xx*** – represent one of the allowed data block length (number of data bytes, on the right after the packet header).

Scalability is fundamental requirement for high-performance Modular Multiprocessor Systems. All requirements of application are changed and can be much more tomorrow than today. Number of processor should be used up to Kilo-Processor system.
Good linear Scalability is a problem for high-performance computer system today. Addition of A-modules, L- and S-modules in RT-system support good scalability and provides more performance and throughput of the Multiprocessor system.

Distributed-memory Model for Multiprocessor system with SOS-architecture should be fundamental to support high-performance parallel-pipeline data processing (computing)
in RT-application. Direct access any processor to any memory in single address space of the Integrated System is similar to SMP model. Big address fields (64 bits) supports or each node up to 256 Tbytes memory. Register field in high part of node memory (256 Mbytes) includes registers with ROM (2K), initial units space (+2K) and available space. Much additional problems in integrated Kilo-processor system exist with cache-coherency.

Cache coherency in multi-processor systems is required to support data availability for all processor during distributed data processing (parallel computing) in real time.
Coherency is the problem in distributed multiprocessor systems, which include many processors, attempting to modify a single datum or holding their own copies of it in their cache at the same time. Coherency, implemented by software or hardware, is request to prevent multiple processors from trying to modify the same data at the same time. The cache-coherency protocol based on the snoopy bus is back plane limited and it should migrate to a more scalable modular multiprocessor system as hardware cache-coherency.
Topology of modular RT-Systems can be constructed from required set of Modules (A-Modules, L-modules, B- or S-module) according to application.
It should be a matrix for DAQ-systems, if data sources are based on matrix detectors, or 3D-topology, if experiment based on 3-D detectors.
In Control Fields the system should have topology according to the structure of accelerator part (linear or ring). MB-based module is connected by L-modules in System Area Network
with required topology. N-node as microprocessor chip (or as a small mezzanine-board) connected by L-modules in different system topology.

Technology Independent System architecture are ready to support a new technology and provide long living time of systems and up-grading modules on different level. SCI-based SOS network Architecture with high-modular structure not depend on changed technology and should consist of required modules.

Standard Construction of special **Mechanics** required for **SCI** standard Modules and Crates**.** To simplify problem PC mechanics and PC-boards with PCI local bus should be used as a platform for A-modules in Distributed systems. Hard disks should be used as reliable distributed external memory near each processor module. Tradition Ethernet should be used as additional communication media for system initializing, user access and serves.

Summary.

System area Network Architecture
for Scalable Open System s should be used for effective (performance/price) construction of multilevel Data Processing RT-Systems for Detector DAQ and Trigger Application on the base of Small PC MB or PXI/cPCI and SCI Link-modules. Hardware coherency in multiprocessor systems supports high-performance at high price, but Software coherency provides good performance at low price.

Distributed Multiprocessor System on the base of PC MB (A-modules) and Link-modules (L-modules or S-modules) without hardware cache-coherency are discussed as example of low-cost effective approach to DAQ and Control RT-System. There are commercial link-modules for SOS–systems interconnections (Dolphin's PMC-SCI Module for modular RT-system, PCI-64 Adapter Module for PC-based distributed data processing and Switch for high-speed interconnections between ringlets).

Different topologies should be constructed with these modules according to requirements of application. DAQ and Trigger Systems with 2-D Matrix topology should be used, which can consist of 4x4=16 single-processors modules (A-type). Toroidal Topology or 3-D Matrix system topology should be used for 3-D detector.
Modules for short distance (up to 5 meters) are based on cooper link. Long distance Module (up to 1-2 km) are based on fiber optics links. For more performance 2-4 processor on a board SMP-module should be used.

Control Systems can be divided on a number of sectors, which should have subsystems (sub-matrixes), interconnected by the same way. The best connections for long distance for Control and Monitoring are fiber-optics modules. Control and Experimental areas should be interconnected in Distributed Integrated systems on the base of system Area Networking technology. For slow control tradition standard connections (CAN) or Ehernet can be used. A set of functional link-modules (L-module without hardware coherency) accessed from Dolphin described below.

All general problems of Scalable Microprocessor system Developments and Applications were discussed in conferences starting from ICSNET'91-95 symposiums on modular systems and networks in S-Petersburg till this year and all future publications open on the intranet sites of Elics Community http://elics.org.ru/ and ware published in paper Proceedings.
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Multimedia Presentation and Picture for this Manuscript are below in Appendix.