Readout System for the CMS RPC Muon Trigger

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Abstract

The CMS detector contains the RPC chambers- a dedicated trigger subdetector- to identify muons, measure their transverse momenta p_T, and determine the bunch crossing from which they originated.The RPC Muon Trigger algorithm is based on muon track search and classification in raw data from the RPC chambers. Large part of the RPC trigger electronics will reside in the control room (approx. 90 meters from the detector) where all trigger data are concentrated. Dedicated synchronous compression - decompression algorithm is needed to sent all data for each bunch crossing via optical links.

The RPC Readout system uses the same data as Trigger system and will be placed in the Trigger Racks.

The idea of readout system and its limitations are discussed below. The paper includes description of prototype boards and tests in the synchronous CERN LHC like test beam H2 in May 2000.

I. INTRODUCTION

Electronics of the RPC Muon Trigger system is distributed on the CMS detector as well as in the counting room. Fig. 1 shows the functional blocks of the electronics. Analog electronics will be placed directly on the chambers (preamplifiers, discriminators, test circuits, etc). Also part of digital electronics will be placed there (synchronizers, TTCrx, control-diagnostic circuits). The rest of digital electronics (Trigger Boards which identify muons and measure their momenta and Readout Boards) will be located in the counting room.

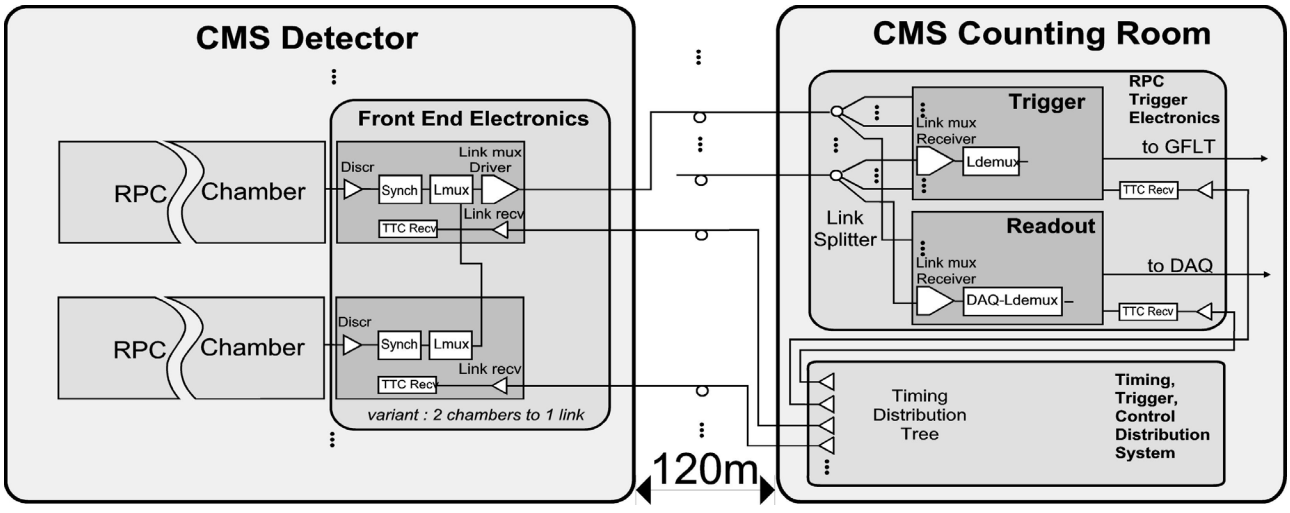

Figure 1: Functional blocks of the RPC Muon Trigger electronics

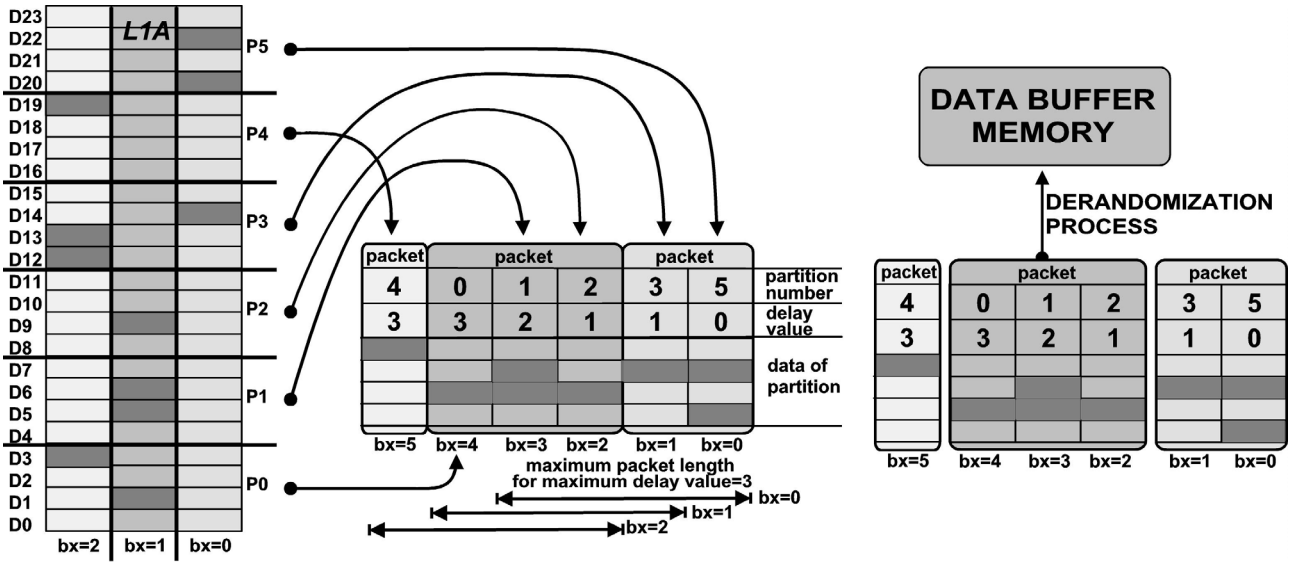

Figure 2: Algorithm of compression and decompression for 24-bits input data divided into 6 partitions

Muon search algorithm requires all of the hits from RPC chambers to be delivered to the counting room [1]. These hits are transmitted from the detector by fibre optic links. LMUX device realizes an algorithm of synchronous compression, while the (DAQ)LDEMUX device that of synchronous decompression (see Fig. 2). The customized compression/decompression algorithm considerably reduces the number of links, thus leading to considerable saving of money, but causes additional constant delay for all transmitted signals between detector and counting room [2].

Compression and decompression algorithm is based on the fact that the rate of hits (dominated by machine induced neutron/gamma background) for a single bunch crossing in a RPC chamber is relatively low. Fig. 3 shows the expected rate background hits for the CMS detector.

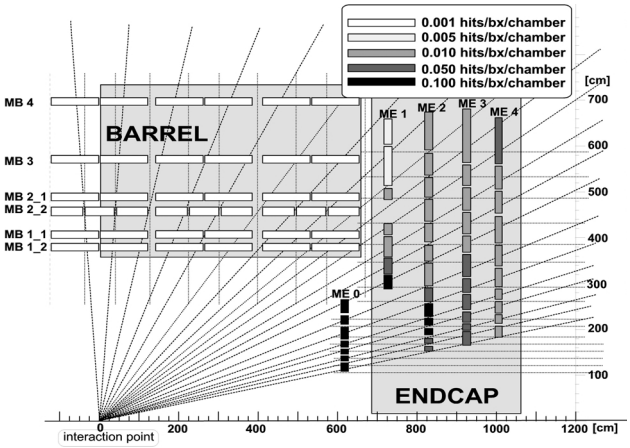

Figure 3: Expected rates of hits for the RPC Detector

The bandwidth of the link system (and readout system) is defined by the compression/decompression algorithm and structure of link system. The required bandwidth is based on results of theoretical analysis; the most severe background conditions are expected for station ME1 close to the beam pipe (in the RE1/1 chamber).

The results of rate analysis presented in Tab. 1 depends on the link system bandwidth. We assumed Poisson distribution and require that $I(t)=I_0\exp(t/\tau)$.

Table 1: Analysis results of packets quantity from RE1/1 stations connected to 48 optical links (worst rate case)

number of packets/event	no noise	100Hz/cm^2 noise
average/link	0.04	0.065
average/crate	3.14	4.59
max/crate (10^6 events)	14	17

Fig. 4 shows the simulated distribution of number of transmitted data packets assuming that 48 links are read out by a Master Card (corresponding to RDPM unit) and losses of trigger efficiency cannot exceed 1%.

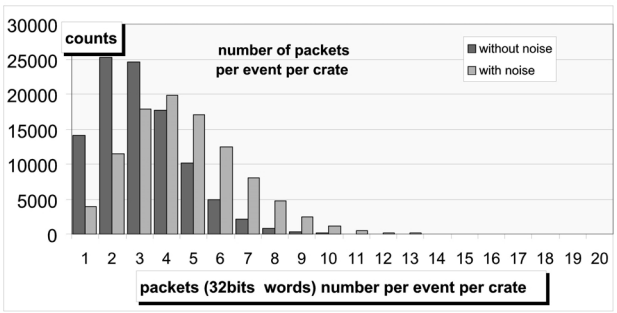

Figure 4: Histogram of event size expressed in no of packets

The analysis permit lead to following constructional parameters:

- one data packet corresponds to one data word sent to RDPM,

- maximum size of event sent to RDPM reaches about 1kB, while the average size of an event is 300 bytes.

Both sizes are considerably less than 2kB page size fixed for CMS experiment, and allow for large margin of safety [3].

II. Readout System design

Structure of readout system is based on results of simulation analysis presented above. Readout system uses the same compressed data packet as Trigger system and will be placed in Trigger Rack. Accepted solution of Readout System design is presented on Fig. 5.

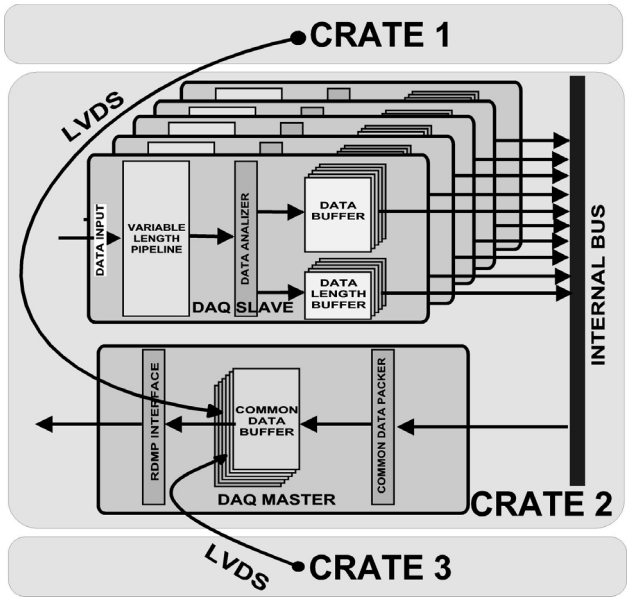

Figure 5: Readout System structure in the Trigger rack

Positions of readout boards and back-plan connections of the trigger crate are shown in Fig. 6.

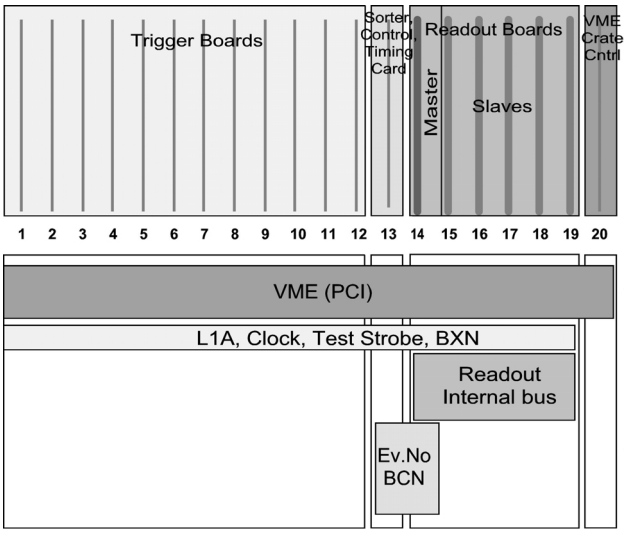

Figure 6: Readout boards positions and back-plane structure

Single module of Readout System serves 40 optical links and cooperates with one RDPM. The large number of links requires the division of the R/O system into two functional parts:

1. Slave Readout Board (SRB): compressed data streams from optical links are derandomized synchronously with a L1Accept. One SRB serves 8 optical links. All SRB work in parallel. There are SRB in 18 TC (version Trigger and Readout).
2. Master Readout Board (MRB) in every TC (version Trigger and Readout); one in every second TC is connected to the CMS DAQ. MRB work in two stages:
    a. they simultaneously take data stored in buffer memories of SLBs within their crates, then
    b. DAQ MRB executes the final data concentration from two TCs and makes these data available to the RDPM.

A. Slave Readout Board

Slave Readout Board derandomizes compressed data streams delivered from chambers RPC by splitters and optical links. Derandomization principle for single data stream from an optical link is shown on left side of Fig. 7 Data packets corresponding to a given trigger signal (L1Accept) are stored in a fixed page of the buffer memory (DPM) together with information about the number of event packets. Thus data from the same event (bx) are stored at the same address space of the DPMs.

Right side of Fig. 7 presents structure of an SRB. Each of 8 channels is served by a single RLDEMUX (PLD or ASIC) and one buffer memory (DPM). VME (or PCI) interface steers the board. SBR is equipped with the JTAG interface for test purposes.

B. Master Readout Board

Master Readout Board concentrates data from buffer memories placed on SRBs. First stage of concentration is executed simultaneously in every MRBs and relies on creation common "data crate event" for each crate separately. Example of such process is shown on the left side of Fig.7 .Then the DAQ MRB, equipped with an interface to RDPM (in central crate on Fig. 5) merges both "data crate event" in one common "data rack event" intended for the RDPM. The synchronous transmission in pipeline mode (discussed in next chapter) between SRBs and MRB via local readout bus (see left side of Fig. 8) is used in a TC.

Right side of Fig. 8 presents the structure of MRB. There are internal LVDS buses between MRBs with CONCENTRATOR (PLD or ASIC) and one buffer memory (DPM). VME (or PCI) interface steers the board. MBR is equipped with the JTAG interface for test purposes.

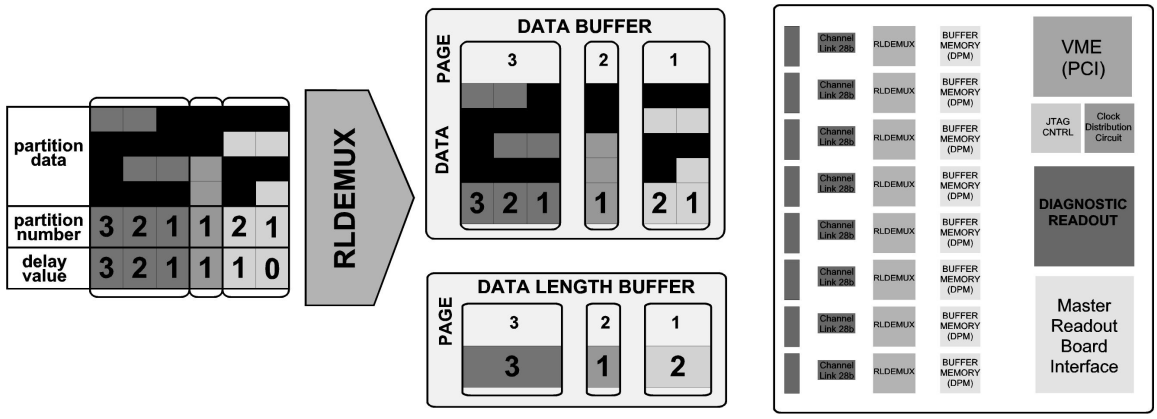

Figure 7: Principle of work (left) and functional scheme (right) of the Slave Readout Board

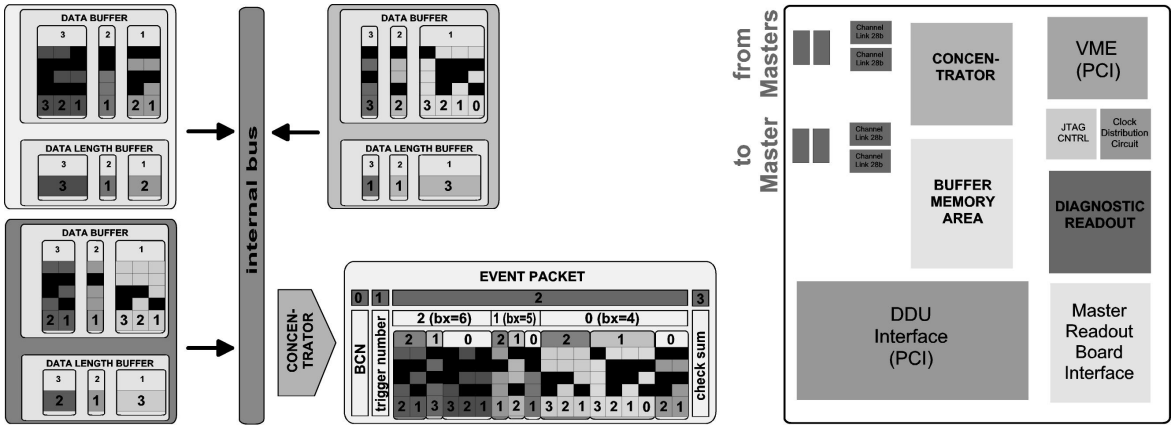

Figure 8: Principle of work (left) and functional scheme (right) of the Master Readout Board

III. READOUT BOARD PROTOTYPE

Readout system tests were realized in Altera CPLD device in 1999-2000. Description of the Slave Readout (SR) and Master Readout (MR) algorithms were realized in AHDL (Altera Hardware Definition Language) using Altera's MAX PLUS II development system compilation. Prototype was tested on synchronous LHC-like test beam at CERN in May 2000.

A. Prototypes design

The principle of work of test readout system is based on two successive stages:

1. data packet derandomisation in SR blocks. Each SR block receives data stream Both SR blocks work in parallel,
2. building of common event in MR block. The data for this event are taken successively from SRs via the local bus. MR block steers the DAQ-SLAVE block by dedicated local bus: clock, trigger and addresses signals are distributed.

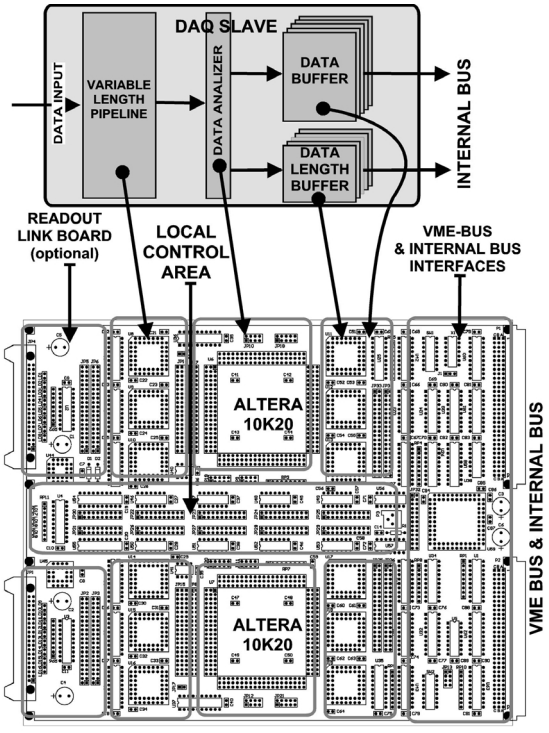

Figure 9: Slave Readout board prototype

Fig. 9 shows Slave Readout test board. There are two SR modules on the test board. LENGTH PIPELINE, DATA BUFFER and DATA LENGTH BUFFER are realized in the DPMs. DATA ANALYZER, in which an algorithm of synchronous data decompression is realized, is placed in the Altera EPF10K20RC240-3 chip. The input signals of compressed data stream could be fed-in in two diffwrent ways:

- Electrically, by front panel connectors; this mode is used for test connection with FDMP,
- Optically, through the interface of fibre optic link.

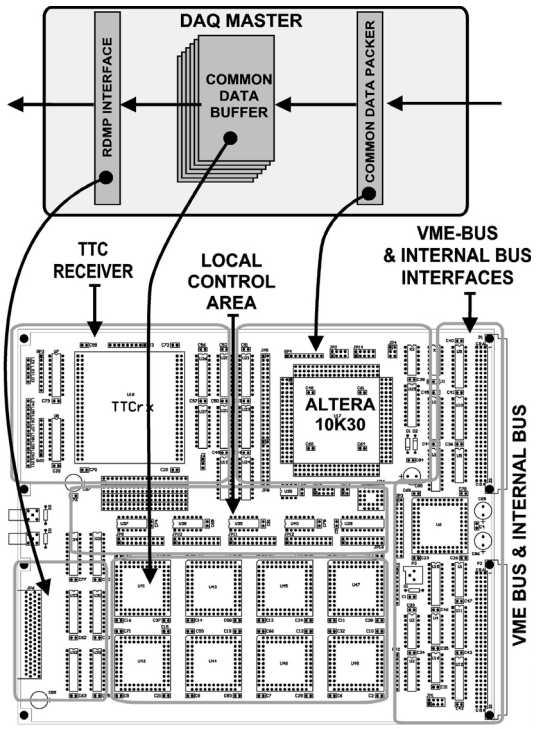

Figure 10: Master Readout board prototype

Fig. 10 shows also the Master Readout test board. There is one MS module on the test board. EVENT DATA BUFFER is implemented in DPM. COMMON DATA PACKER, which builds common event packet, is placed on the Altera EPF10K30RC240-3 chip. The board may work autonomously (has an internal clock and requires external trigger signal) or cooperates with a TTC circuit (and then additionally stores event number and bunch crossing number). The event packet, stored in event data buffer, is accessible via:

- VME interface for computer reading system,
- standardized DDU interface

The Readout test system assumes nominal parameters for CMS RPC trigger and works with a nominal clock- 40 MHz. Synchronous communication was implemented. This solution allows for application of 40 MHz clock for data transmission with assumed memory access time equal from 15 to 20 ns. The total data reading time, from many DAQ-SLAVES, w as minimized.

B. Prototypes test on test beam at CERN

The prototype of the readout system has been successfully used during LHC-like beam tests (May 12-24 2000). Fig. 11 shows the layout of electronics used for these tests.

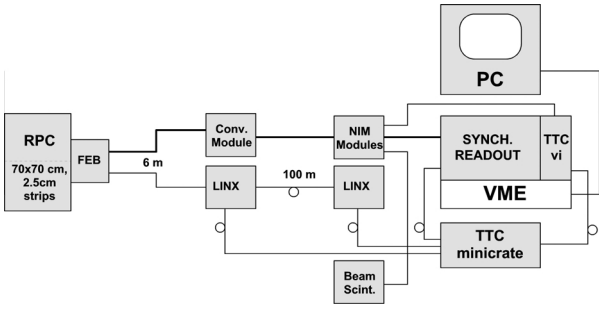

Figure 11: LHC-like beam RPC test setup

Fig. 12 shows histogram of data taken from one strip of RPC chamber. The algorithm of RPC signal synchronisation has been realized in NIM electronics.

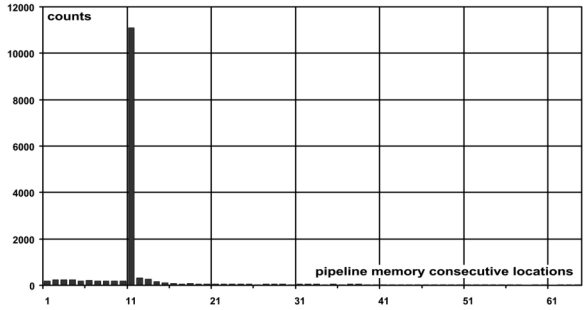

Figure 12: RPC signal registered by the readout system

The beam structure has been observed in row RPC data The main results of these tests are following:

- the principle of RPC signal synchronisation algorithm proven,
- the procedure of bunch synchronisation for RPC validated.

IV. REFERENCES

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[2] K. Poźniak et al. „Resistive Plate Chamber (RPC) based muon trigger system for the CMS experiment – data compression/decompression system", Nucl. Instr. and Meth. in Phys. Res A 419, pp. 701-706, 1998

[3] A. Racz „CMS DAQ Synchronization" Synchronization Workshop Nov 11, 1998, CERN