First-Level Endcap Muon Trigger System for ATLAS

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Abstract

The first-level endcap muon trigger system have been designed for ATLAS experiment. The system has the main tasks which are to identify bunch crossings and to make trigger decisions for high transverse-momentum muon candidates. There are various requirements for trigger electronics to be satisfied, and several implementations using ASICs and FPGAs satisfy the requirement. We present the trigger scheme and overall of the system design.

I INTRODUCTION

The ATLAS trigger and data-acquisition system consists of three stages of online event selection. The first-level (LVL1) trigger system [1] receives the information on events at an interaction rate $\sim$ 1 GHz from 40 MHz of bunch-crossing rate, and has to reduce the selected-event rate up to $\sim$ 75 kHz (upgradable to 100 kHz). The ATLAS LVL1 trigger system uses signals from both the calorimeters and muon detectors. Independent, pipelined trigger processors run for both the sub-systems at the bunch-crossing rate; the results of these systems are combined to generate the final LVL1 trigger decision.

This paper will describe the design of LVL1 endcap muon trigger system. The muon trigger system uses signals from only the trigger chambers, which are fast and finely segmented detectors.

The endcap system employs Thin Gap Chambers (TGCs) [2], which are similar to multi-wire proportional chambers, and have 320K channels of anode wire-groups and orthogonal readout strips. Signal efficiency is $> 99\%$ for 25-nsec gate; thus each bunch crossing is identified. Combinations of hits in TGCs are utilized to make trigger decisions for high transverse-momentum (p_T) muon candidates. The trigger system has been designed with fulfilling several requirements for trigger electronics.

II REQUIREMENTS

A detailed study has been made of the requirements for the LVL1 muon trigger [3]. Main requirements for trigger electronics are shown as follows:

- The trigger system has to be operated with wide p_T threshold, 6-35 GeV, with >90% efficiency. This wide range covers not only search physics requiring higher p_T muons at high luminosity, but B physics requiring inclusive muons at low luminosity. Six different thresholds are required.
- An average acceptance of $\geq$90% in the pseudorapidity range $\eta < 2.40$.
- The endcap region is divided into totally 144 trigger sectors. The two highest-p_T tracks have to be selected in each trigger sector.

- The latency of trigger decisions at front-end electronics is required to be less than 2.5 μsec, including 0.5 μsec for contingency.

III TRIGGER SCHEME

A *Trigger Chamber Layout*

The LVL1 muon trigger is generated with the trigger detectors: Resistive Plate Chambers (RPCs) in the barrel ($\eta < 1.05$) and TGCs in the endcaps ($1.05 \leq \eta < 2.70$). These chambers are arranged as shown in Figure 1. The TGCs are arranged spokewise in three different planes (M1, M2, M3 and EI/FI in the figure) in each side at $|z| \sim 14$ m and one more inner plane (EI/FI) at $|z| \sim 6.9$ m. M1 consists of triplets which are units with three wire-layers and two strip-layers; M2, M3 and EI/FI consists of doublets which are units with two of wire-strip layers. Each plane is divided into forward (inner) and endcap (outer) regions at $\eta = 1.92$. Anode wires of TGCs are laid in the azimuthal direction and provide signals for r information; orthogonal cathode strips provide signals for ϕ.

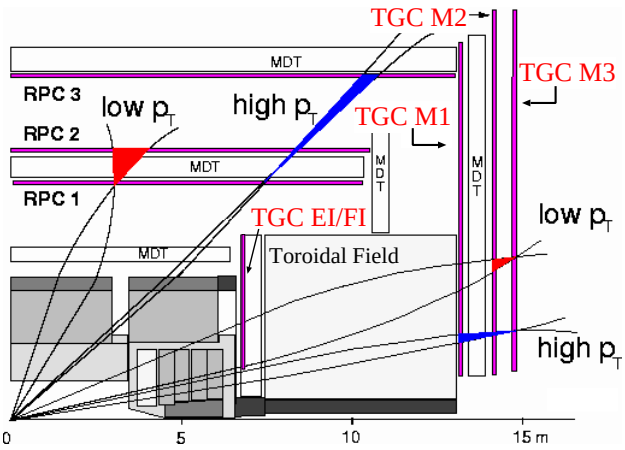

Figure 1: Chamber layout and trigger scheme

B *Main Scheme*

The trigger is based on the measurements of muon trajectories through these layers. The ATLAS has air-core toroidal magnets creating magnetic fields for muon detection. As shown in Figure 1, a muon is bent in the fields; the information on its charge and momentum is extracted from the deviation of the bending path with respect to the non-bending projection toward the interaction point (IP). The trigger plane farthest from the IP (M3) is called the pivot plane and the straight line from the IP to the hit on the plane is referred as the path of infinite-momentum particle. The larger a muon momentum, the smaller the deviation of the muon track and the track hits are closer to this straight line. High-p_T muons therefore can be selected by setting the maximum deviation. The maximum deviation corresponds to the trigger threshold.

The two different lever arms from M3 to M1 and M2 provides the different measurements of deviations. They allow the thresholds to cover a wide range of momenta: M2 and M3 cover a lower-momentum range; additional M1 allows a higher-momentum range.

A muon track is identified by requiring coincidence criteria for hits in layers. In the first stage, the following local criteria are required:

1. For wire hits in M2 and M3, it is required to satisfy 3-out-of-4 coincidence around the straight path within a certain deviation.

2. For wire hits in M1, it is required to satisfy 2-out-of-3 coincidence around the same path.

3. For strip signals, same as Condition 1 except the different limit of deviation.

4. For strip hits in M1, it is required to satisfy 1-out-of-2 (OR) coincidence around the same path.

In the second stage, decisions on Condition 1 (3) and 2 (4) are combined and two-fold coincidence is required for wire (strip) hits to obtain the higher-momentum tracks.

These coincidence operations are performed for r and ϕ independently. In the third stage, the results from the operation are combined as shown in Figure 2. The trigger

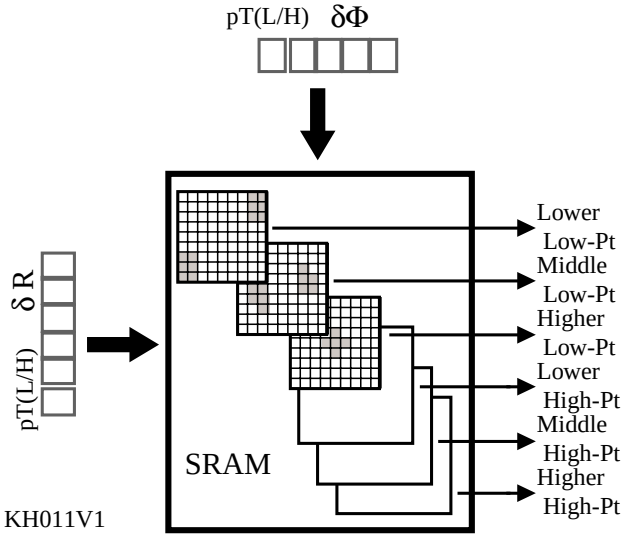

Figure 2: r-ϕ coincidence

windows are formed in r-ϕ space and p_T thresholds are determined by the sizes of the windows. Six different sizes are provided for six different threshold.

In the final stage, the results of the r-ϕ coincidence and the information from EI/FI are combined to eliminate charged particles with momentum $\sim$ 100 MeV (so-called

"100 MeV" background [4]), which have potential to cross the trigger planes and fire the trigger. The final trigger decision in the endcap system is made by selecting two highest-p_T tracks in each trigger sector.

C Chamber Boundaries

In order to accomplish a good acceptance, TGCs are arranged so that they overlap with the neighbors and cover gaps between them. The overlaps are made only enough to cover the bending for the muons with momentum in the required range.

The overlaps may cause double-counting of single muons. The following techniques are introduced to minimize double counting.

Wire overlaps in r: On the pivot plane, wire-groups overlapped are OR'ed together. As a result, TGCs work as if they are combined into a single virtual chamber in r and a track makes a unique hit there.

Strip overlaps in r: Fake strip hits caused by double counting are eliminated in r-ϕ coincidence since the wire overlaps are already solved.

Strip overlaps in ϕ: On the pivot plane, the strip overlaps are masked to avoid double counting. The masking is programmable to optimize the trigger efficiency and double-counting rate.

Wire overlaps in ϕ: Fake wire-group hits caused by double counting are eliminated with the information on strip hits whose double counting is already solved.

These techniques are common for both within forward region and within endcap. Overlaps should be considered between forward and endcap, and endcap and barrel regions. The edges of strips of the pivot chambers in the forward region are cut away to eliminate double counting between forward and endcap regions. Double counting between endcap and barrel regions is eliminated by the Muon CTP Interface (MUCTPI).

D System Segmentation

TGC trigger system is divided into 48 endcap sectors and 24 forward sectors in each side. Each endcap sector contains 148 (37 η by 4 ϕ) Regions of Interest (RoIs); forward sectors contains 64 (16 η by 4 ϕ) RoIs. Each RoI contains 8 wire-group channels by 8 strip channels.

System segmentation is different between the detector and trigger logic since the chamber layout shown is not projective toward the IP. Hence the virtual pivot plane is divided into projective segments for wire-groups. Strips segmentation can be succeeded for trigger system.

IV SYSTEM DESIGN

The system design to perform the trigger scheme is described here.

Figure 4 shows an overview of the TGC trigger system. The system is broken down into several parts based on the trigger stages shown above.

Signals from wire-groups and strips are processed on Amplifier-Shaper-Discriminator (ASD) Boards [5] attached to TGCs. Each ASD Board handles 16 channels of signals.

Digitized signals from ASD Boards via LVDS links are then received by Patch Panels (PPs) to identify bunch crossing. OR'ing and system segmentation for the trigger logic is also performed by communicating with adjacent boards. PPs have the other functions as backplanes for ASD Boards and following Slave Boards (SLBs).

SLBs perform local coincidence operations. Five kinds of coincidence logic are necessary. Information on local hit positions r, ϕ, and deviations Δr, $\Delta\phi$ are encoded and sent in LVDS level.

SLBs are directly connected to the corresponding PPs, forming a unit package, called P-S Pack. P-S Packs are sit on the outer surfaces of TGC wheels, M1, M3 and EI/FI. The sizes are approximately 50 cm $\times$ 300 cm for M1 and 50 cm $\times$ 475 cm for M3.

Output signals from the M1 and M3 SLBs via $\sim$ 15-meter LVDS links are fed into a High-p_T Board (HPB) to be combined for higher-momentum tracks. In order to perform the coincidence operation for projective segments, two triplets and three doublets are fed into a coincidence matrix for wire, while OR logic is implemented for strip. Hit information is encoded and serialized using G-link protocol. HPBs are placed as 9U-VME boards in crates on the outer rim of M1. Output signals from the HPBs are sent to the following Sector Logic (SL) Boards via 90-meter optical links

SL Boards perform R-ϕ coincidence operations. Output signals from EI/FI SLBs are also fed into the SL for final trigger decision. Finally two highest-p_T tracks are selected in each trigger sector. SL Boards (9U VME) are located outside the cavern, in USA15.

The result from SL is sent to the MUCTPI to be combined with the information on barrel muon trigger system. The result from MUCTPI is sent to the Central Trigger Processor (CTP) and combined with the information on calorimeter system. The CTP finally generate a LVL1 Accept (L1A) signal. The L1A is sent to the Timing Trigger and Control (TTC) system to be distributed to the front-end readout electronics.

At each trigger stage, the track/hit multiplicity allowed in the system is limited to minimize the logic size, number of connections and costs. The rules of the constraints are summarized in Figure 3. Ranges of Δr and $\Delta\phi$ are large enough to cover the momentum range and are fixed as shown in the figure. Local coincidences at every stage are programmable to provide tighter conditions for more efficient trigger and background robustness.

The major functions of PP, SLB and HPB, including the selection rules shown above, are implemented using full-custom ASICs. SL is implemented using FPGAs and

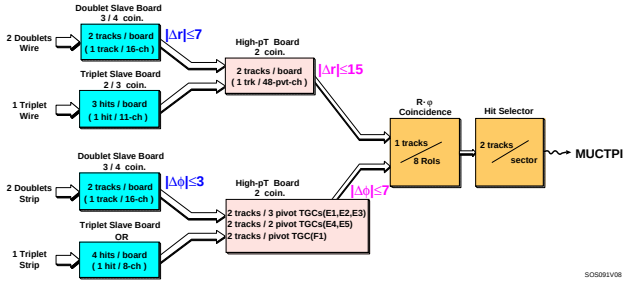

Figure 3: Constraints on track/hit multiplicity of the trigger logic

SRAM look-up tables so that the r-ϕ coincidence is fully programmable.

V DEVELOPMENT STATUS

We are prototyping three kinds of ASICs as summarized in Table 2. Details on prototyping are presented in this conference [6]. SL is also being designed as prototype-0 using Vertex series FPGAs. We also have begun the board layouts, crate and backplane designs.

IC	Spec.	Process	Scale (#gates)	Ready By
PP	fixed	Rohm 0.6 μm	10k	Octoer
SLB	not fixed	Rohm 0.35 μm	350k	2001
HPB	fixed	Hitachi 0.35 μm	20k	2001

Table 1: Summary of full-custom CMOS prototype-0

VI PERFORMANCE

The total latency of the system has been estimated by considering the local simulations of logic, measurements using partial prototypes and knowledge of cable lengths. The breakdowns are summarized in Table 2. The total is

Stage	Logic	Propagation	Sub-Total
TOF to TGC		3	3
TGC to ASD	1		1
ASD to PP	1	2	3
PP to SLB	2		2
SLB to HPB	4	3	7
HPB to SL	5	18	23
SL to MUCTPI	8	1	9
Total	21	27	48

Table 2: Contributions to the estimated latency up to MUCTPI (in bunch-crossings)

estimated to be 1.2 μsec including 0.6 μsec of propagation time. Additional 0.8 μsec for MUCTPI up to front-end read-out electronics gives a total latency of muon trigger system 2.0 μsec, satisfying the requirement.

Trigger performance, such as efficiencies, trigger rates, etc., has been checked with simulation. New object-oriented simulation is in preparation to confirm the detailed trigger logic.

VII SUMMARY

We have designed the first-level endcap muon trigger system for ATLAS. The system is designed to perform bunch-crossing identification and trigger decisions for high-p_T muon candidates. The system is designed to meet the requirements for trigger electronics and will perform with p_T threshold grater than 6 GeV using programmable coincidence windows. Main logic is implemented using full-custom ASICs and FPGAs. Prototyping of ASICs is in progress; details are presented in another presentation. We also have begun the board layouts, crate and backplane designs. A slice of the full system using prototype components will be tested in 2001.

VIII ACKNOWLEDGMENTS

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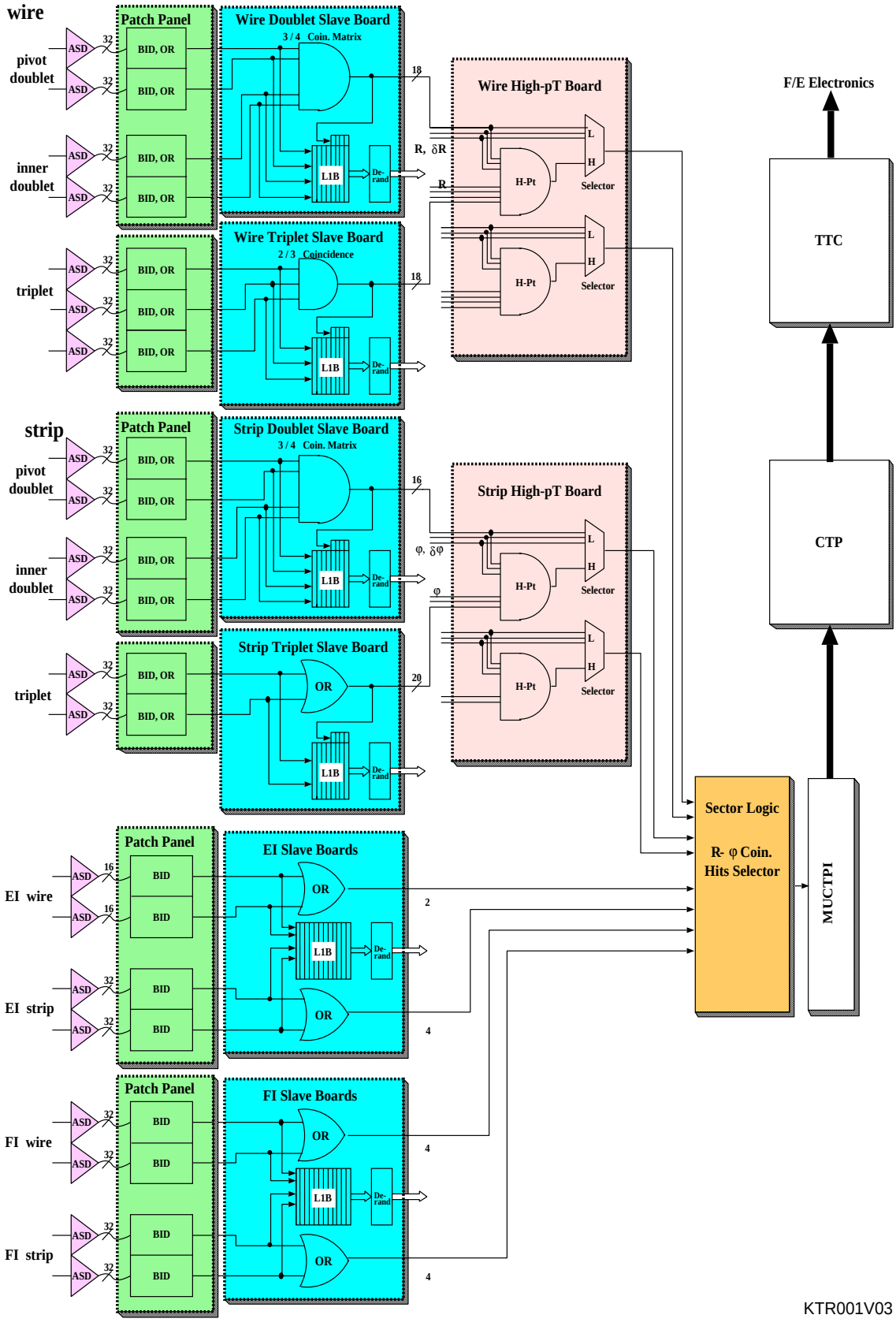

Figure 4: Overview of the TGC trigger scheme