Test results of the ALICE SDD electronic readout prototypes.

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Abstract

The first prototypes for the front−end electronic of the ALICE silicon drift detectors has been designed and tested. The integrated circuits have been designed using state−of−the−art technologies and, for the analog parts, with radiation−tolerant design techiniques. In this paper the test results of the building blocks of the PASCAL chip and the first prototype of the AMBRA chip are presented. The prototypes fully respect the ALICE requirements; owing to the use of deep−submicron technologies togheter with radiation−tolerant layout techniques, the prototypes have shown a tolerance to a radiation dose much higher than the one foreseen for the ALICE environment.

I. THE ALICE SDD READOUT ARCHITECTURE

The SDD (Silicon Drift Detectors) are expected to provide high detection efficiency over the whole detector surface, a spatial precision of the order of 30 μm, a two−track separation down to O(600) μm.

In addition the detector should provide a charge resolution such that the dE/dx resolution is dominated by Landau fluctuation, from which the truncated mean of the four ITS dE/dx samples is around 10% for M.I.P.

A. SDD readout requirements

The charge released by the minimum ionizing particle in an SDD is about 4 *fC*. For hits far from the anode pads the charge collected by one is typically one−third to one−half of the 4 *fC*; thus the tails of the hit signal, essential for the position determination, will consist of less than 1 *fC*.

The range of useful signals is limited between the noise level (250 e^-) and 28−32 *fC*, but higher signals (up to 160 *fC*) are possible.

The charge generated by a particle crossing the detector, depending on the crossing point and therefore on the drift time, can be collected by one anode as a fast gaussian signal (σ < 5 *ns*) or by several anodes (up to five) as a slower gaussian signal (σ = 30 *ns*), due to the diffusion during the charge drift through the detector.

In order to obtain the required precision the signal has to be sampled at quite high frequency (around 40 *MHz*); the dynamic range is 10 bits while an 8 bit linearity is sufficient.

Due to the high sensitivity of the SDD to temperature variations and the very stringent requirement on the material budget which does not allow a very massive cooling system, the allowed power consumption for the electronic readout is very low (below 5 *mW*/channel).

Table 1 summarizes the SDD readout requirements.

Dynamic range	0.04−32 *fC*
Max signal charge	160 *fC*
σ range	5−30 *ns*
Noise	250 e^-
Sampling frequency	40 *MS/s*
No. of bits	10
Max drift time	6 μs
Max power per channel	5 *mW*

Table 1 : SDD readout requirements

B. System architecture

The basic principle of the SDD readout scheme is to amplify the signal coming from the detector, convert it locally to a digital representation, and send the data directly to the DAQ. This architecture offers two main advantages, compared to schemes in which the analogue data are transmitted far from the detector or to schemes with distributed intelligence :

- Converting the signal into digital samples immediately after the preamplifier avoids signal degradation during data transmission.

- Sending data directly to the DAQ system, without online data analysis, allows the use of more powerful and flexible offline data–analysis tools. Moreover, early failure detection is easier if raw data are directly sent outside the experimental area.

In principle this architecture would require a low noise preamplifier, a fast ADC and some data–formatting logic. In practice the architecture is more complex, in order to cope with the limited power and the material budget.

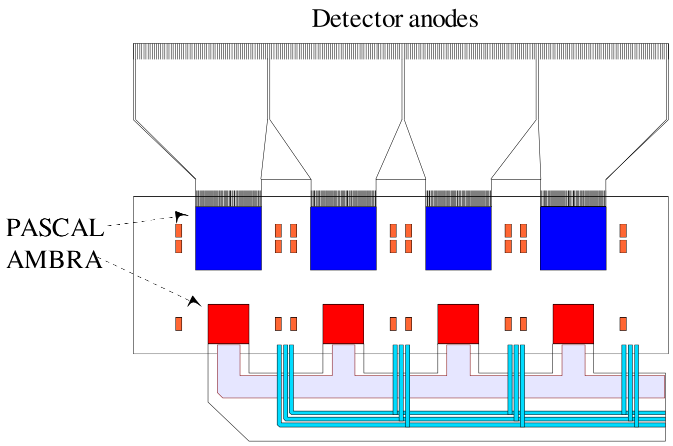

Figure 1 : Front–end unit

The required sampling frequency is 40 *Mhz*. At this speed it is extremely difficult to design an ADC with a power budget of only 5 *mW*/channel; the adopted solution is based on an analogue memory to store temporarily the samples. When a trigger signal validates the data the analog memory content is frozen (after an appropriate delay to account fot the total detector drift time) and the conversion process is started. In this way the ADC is activated only when the data are valid and can work at conversion rates lower than the sampling rate. Of course the conversion time should be kept as low as possible in order to minimize the dead time. The size of the analog memory should be large enough to cover the detector drift time, which is $\leq 6\ \mu s$; at 25 *ns* sampling time 240 cells are required. A number of 256 cells has been chosen to be able to accommodate changes in the detector parameters.

The front–end readout unit, shown in fig. 1, is a hybrid circuit containing four submodules of the preamplification, analogue storage and ADC architecture and multi–event buffer integrated circuit pair. The four submodules are arranged in two ASICs :

- PASCAL : based on 64 acquisition channels (preamplifier plus a 256 cells analog memory), 32 successive approxi–mation A/D converters and a control and interface unit.

- AMBRA : basically 2x16 kbytes SRAM buffers, plus the interface and arbitration logic.

II. Pascal prototypes

PASCAL is the most complex ASIC of the SDD readout chain. In order to prove the feasibility of the circuit, several prototypes have been designed and tested.

C. Preamplifier prototypes

The first preamplifier prototype, designed in 0.8 μm technology, has been tested both on a bench and in various test beams attached to the detector. The architecture is a two stage configuration based on the active feedback principle and can exploit both linear and square root compression transfer curve. Details on the circuit and on the test beams can be found in [4] and [5].

The final version in a 0.25 μm commercial technology is currently under test. A leakage current compensation circuit has been added to this version.

D. Analogue memory prototypes

The analogue memory final protoype, currently under test, is an extension of a test chip designed for the CERN RD49 project.

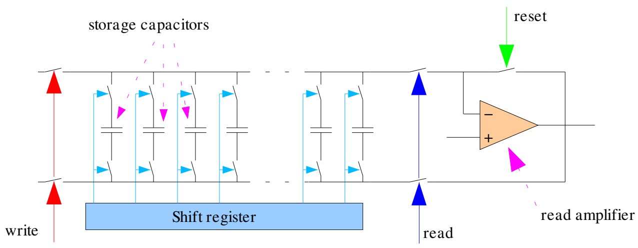

Figure 2 : Analogue memory scheme

The memory architecture is shown in fig. 2 and is based on a voltage–in, voltage–out architecture; during the write phase the write switches are closed while the read switches are open. The reset switch is also closed in order to maintain the read amplifier in a closed loop configuration. The shift register sequentially connects the analogue memory cells to the input via minimum size switches; in order to avoid charge sharing between adjacent cells a non–overlapping logic is added on these control lines.

In the read phase the write switches are open and the read switches are closed; the memory cells are sequentially connected to the read amplifier in a feedback configuration. The readout of each cell is completed by the cell reset via the reset switch.

A different clock frequency for write and read operation can be selected through an internal multiplexer. The write and read reference voltage are independent and can be used for voltage translation.

Gate capacitance has been used as storage capacitance because of its very high capacitance per unit area (5.5 *fF/μm*^{2}); in order to increase the linearity in range of interest, an N+ poly in an N−well has been used.

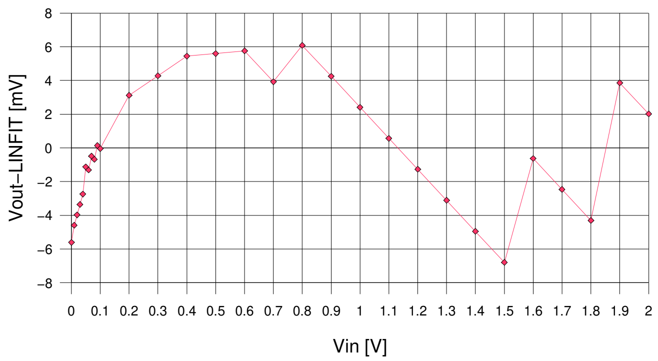

Figure 3 : Analogue memory non−linearity

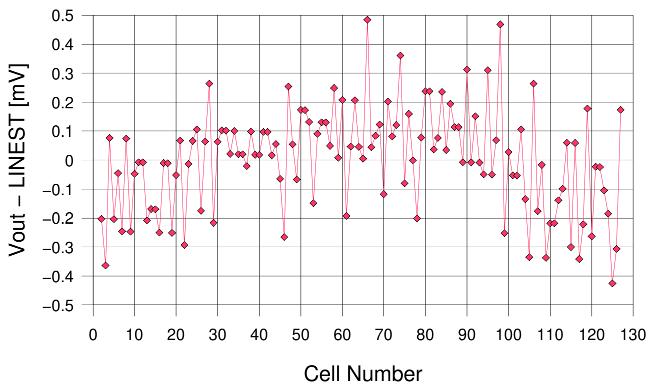

Figure 4 : Analogue memory pedestal variation

The test chip is designed in a 0.25 *μm* commercial technology with radiation tolerant techniques. The write frequency is 40 *Mhz* while the read frequency is 2 *Mhz* and is limited by the settling time of the read amplifier. With a 600 *fF* storage capacitance the cell area is only 56.1x11.1 *μm*^{2}.

The 2x2 *mm*^{2} prototype chip contains eight 128−cells channels and dissipates 31.6 *mW*. The linearity is better than 0.5% over a 2 *V* input range, while noise and pedestal variation over the 128 cells are less than 1 *mV*.

Figure 3 and 4 shows the non linearity and the pedestal variation of the test chip.

The effect of the capacitors non−linearity for low voltage values is visible on the left part of fig. 3 while the sharp transitions on the center and the right side are due to the decreased resolution of the measurement system for higher voltages.

Owing to the use of enclosed devices and guard rings, no significant variations in the chip behaviour have been observed after a 10 *Mrads* irradiation.

E. ADC prototypes

The final A/D converter prototype, designed in a 0.25 *μm* technology with radiaton tolerant layout techniques, has been tested. The converter is based on the successive approximation technique; a switched capacitors net provides both the DAC and the subtraction functions, so no operational amplifiers are needed.

In this scheme the capacitive DAC size doubles for each bit added to the converter resolution; in order to obtain 10 bit in a reasonable area, a 8+2 scheme has been chosed. After a first 8 bit conversion, the two LSBs are determined with a capacitive sub−DAC attached to the main DAC termination capacitance.

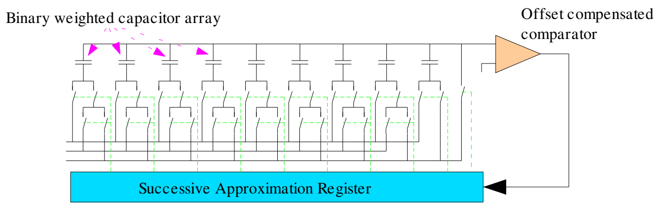

Figure 5 : ADC scheme (2−bit subdac not shown)

The 2x2 *mm*^{2} test chip, designed in collaboration with the CERN RD49 program, contains 2 ADCs and a copy of the offset compensation comparator for test purposes. The single converter size is 1x0.32 *mm*^{2}.

For 500 *ns* conversion time, the FFT test gives a SNDR > 58 dB (Fig. 6) while the histogram test gives a INL between −1.5 and 2 LSB (Fig. 7) with no missing codes and a DNL between -−0.8 and 1.5 LSB (Fig. 8). The ENOB is greater than 9. The performances decrease as the conversion time is reduced and for 250 *ns* the ENOB is around 8 bit.

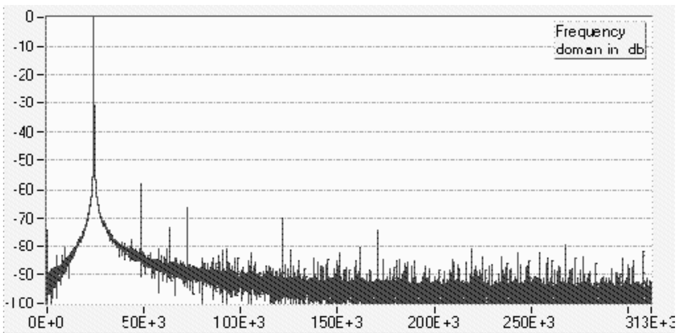

Figure 6 : FFT for a 25 kHz input sinewave

HSPICE simulations suggest that the performance degradation at clock frequency above 20 Mhz is related to the resistance of the reference lines. Preliminary tests on the new version confirm the simulation results.

Tests under an X–ray source for total dose effects has shown no significant changes in the behavior for doses up to 10 *Mrads*.

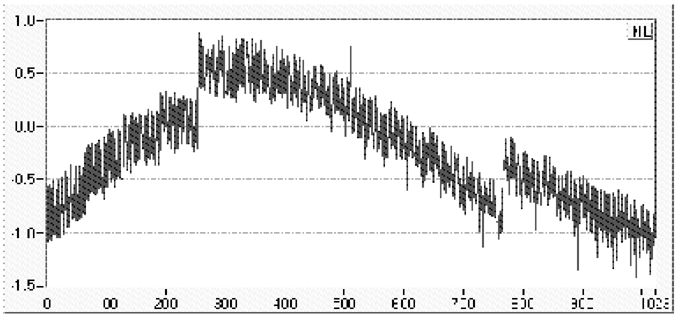

Figure 7 : INL for a 25 kHz input sinewave

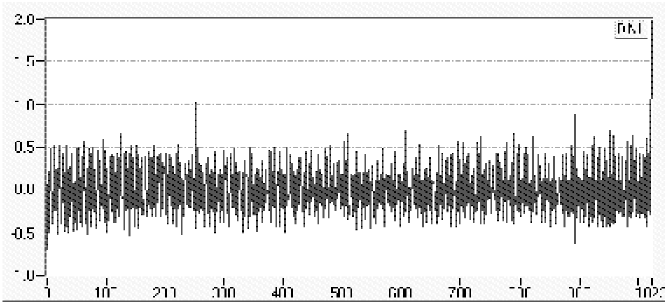

Figure 8 : DNL for a 25 kHz input sinewave

III. Ambra prototype

The first version of the AMBRA chip has been designed in a 0.35 μm commercial technology and tested. The chip size is 3.8x4.4 mm^2; the chip area is dominated by the RAMs.

The arbitration and interface logic works up to 100 *Mhz*, while the RAM maximum frequency is limited to 50 *Mhz*, well above the 40 *Mhz* required frequency.

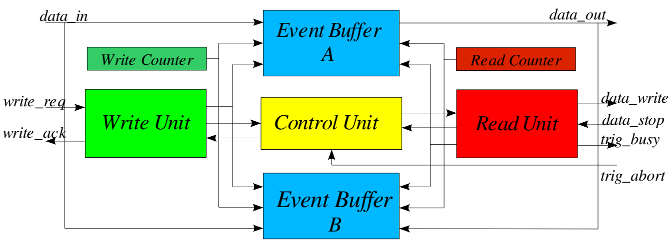

Figure 9 : AMBRA scheme

The power consumption is negligible in idle state (600 μW), is 69 *mW* in write only state and 133 *mW* in read/write.

The testability of the circuit has been addressed in the following way :

- in terms of incoming tests a multiplexed flip–flop strategy has been adopted
- in terms of on–board testability a IEEE 1149.1 compliant interface (JTAG) has been integrated in the ASIC

The chip, designed with no radiation tolerant layout techniques, has been tested under an X–ray source. After 300 *krads* and 1 *Mrad* the circuit was still working, while after a 5 *Mrads* dose memory fails were observed.

The memories used in the circuit were directly provided by the silicon foundry; their early failure is probably due to some more aggressive design rules used by the foundry for those standard blocks.

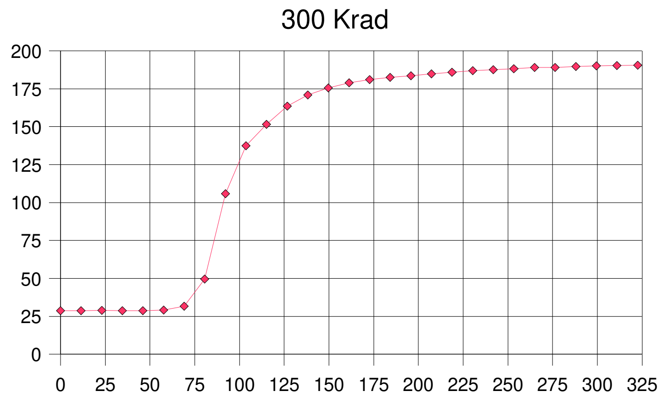

Figure 10 : supply current during a 300 krad irradiation

A very fast increase of the leakage current has been observed after 50–60 *krads*. The current increases of an order of magnitude after 200 *krads*; after that the current slope decreases.

Fig. 10 and 11 shows the supply current monitored during irradiation. The irradiation rates were 10.65 *Krad/min* and 5.759 *Krad/min*, respectivly.

A partial recovery of the current has been observed few hours after the irradiation; the final current, however, remains 2–3 times higher than the original one.

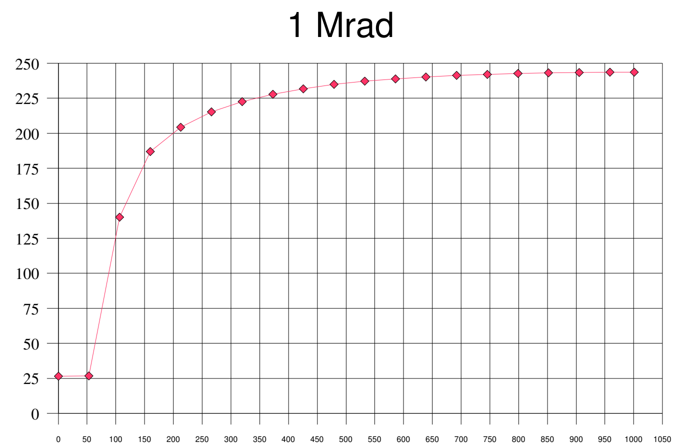

Figure 11 : supply current during a 1 Mrad irradiation

IV. Conclusions

The preamplifier, the analog memory and the A/D converter prototypes fulfil the requirements for the ALICE SDD readout and have been used as building blocks of the first PASCAL prototype, currently under test.

The chosen quarter micron technology, combined with the radiation tolerant layout techniques, provides a radiation resistance much higher than the levels foreseen for the ALICE environment.

The next step is the test of the mixed signal aspects in the full chip.

The 0.35 μm CMOS version of the AMBRA chip fulfil the specifications in term of functionality, clock frequency and power consumption. Conservative considerations relative to the leakage problem under irradiation suggests to design the second version of the chip with a radiation tolerant library.

V. References

[1] ALICE Inner Tracking System TDR, CERN/LHCC 99−12, p. 107−126

[2] Proceedings of the Fifth Workshop on Electronics for LHC Experiments, CERN/LHCC 99−33, p. 138−142

[3] Nucl. Ph. A 661 (1999) 694c−697c

[4] Proceedings of the Fourth Workshop on Electronics for LHC Experiments, CERN/LHCC 98−36, p. 499−502

[5] Nucl. Instr. and Meth. A 450 (2000) 338−342