PRODUCTION TESTS OF MICROSTRIP DETECTOR AND ELECTRONIC FRONTEND MODULES FOR THE STAR AND ALICE TRACKERS

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Abstract

A compact front-end microstrip detector module has been designed and prototyped. It includes a Double-Sided (DS) Silicon Strip Detector (SSD) and the related Front End Electronics (FEE) located on two hybrids, one for the N side and one for the P side [1]. Bumpless Tape Automated Bonding (TAB) [2], [3], [4] is used to connect the detector to the dedicated ALICE128C FE chip [5], [6], [7] located on the hybrids by means of microcables. These microcables are bent in order to fold over the two hybrids on the DS SSD. This module meets the specifications of two experiments, ALICE (A Large Ion Collider Experiment) at the LHC collider at CERN [8], [9] and STAR (Solenoid Tracker At Rhic) at the RHIC collider at BNL (Brookhaven National Laboratory) [10]. This self-consistent FE module has been tested in the PS and SPS beams at CERN for signal, noise and resolution and in the Vivitron beam for radiation hardness. The related results have been presented [1], [9], [11]. At present, the production of these modules is starting for the STAR experiment whereas the corresponding production for ALICE belongs to a near future. Careful controls and tests are essential at each production step as described in this report.

1. INTRODUCTION

The STAR SSD layer overlaying the Silicon Vertex Tracker (SVT) requires 320 working detector modules i.e. the production of a total of 400 modules. The ALICE Internal Tracker System (ITS) requires 1700 similar modules i.e. the production of more than 1800. The very low power consumption of these modules allows air-cooling in STAR but water-cooling has been kept in ALICE, representing the only significant technical difference between the two applications.

Whereas the tested prototype modules have been mainly manufactured inside the laboratory, production of more than a few units must be transferred to industry.

Manufacturing such a module relates to three main tasks: producing the components of the module, assembling these components and testing each component and subassembly after each step as displayed in figure 1. All the test results are transferred to a production data base which provides network access to the data for the whole collaboration by means of any net browser at the web address http://star.in2p3.fr and/or http://ssd.if.pw.edu.pl .

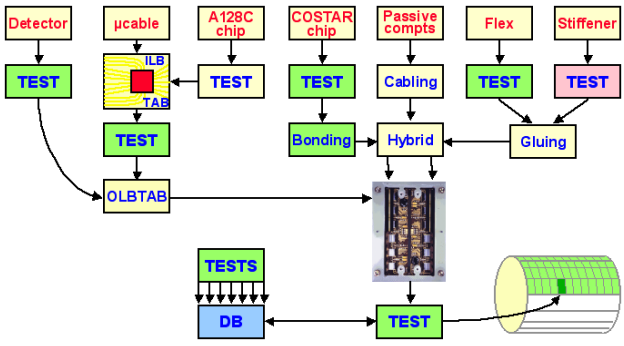

Fig. 1: Manufacturing and testing of a module.

Each module is a mechanically self-consistent assembly of one DS SSD and two FEE hybrids, connected together by TABed microcables.

Each of these FEE hybrids includes a flex cable, part of the hybrid in charge of interconnecting active and passive components on the hybrid, the stiffener supporting the flex cable, the passive electronic SMD components, the ALICE128C FE chips, the COSTAR control chip [12].

2. DOUBLE SIDED SSD

The 75 × 42 × 0.3 mm DS SSD includes 768 AC coupled strips on each side with a pitch of 95µm at a stereoscopic angle of 35 mrad. Guard and bias rings are all together ≤ 1 mm wide.

Production specifications have been described in the CCTP document [13]. The main features relate to a unique operating voltage below 55 volts in between depletion voltage and breakdown voltage, a biasing current $i_{bias} \leq 2\mu A$, a guard ring leakage current $i_{guard} \leq 5\mu A$, and a number of dead coupling capacitors on each side below or equal to 10.

More than 440 detectors have been delivered by Eurisys and tested in our laboratory on a probe station in order to select 400 detector working inside the specifications. The test itself is done by mounting the bare detector in an epoxy frame (figure 2) which enables handling, identification, and connection to the test equipment for biasing by means of two bonds on each side. This frame and the related bonds are removed later before the module assembling step. The test measurements are transferred into the production data base.

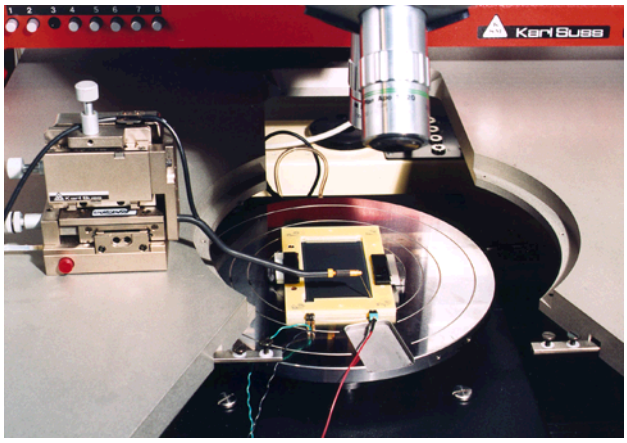

Fig. 2: Measurement of a DS SSD in it's frame.

2.1 *Operating voltage and current*

The operating voltage V_{op} is derived from the operating range defined between the depletion voltage V_d and the breakdown voltage V_{bd} defined as the biasing voltage corresponding to the maximum allowed current. Deep investigation has been made in order to define those in a reliable way. Depletion voltage V_d can be investigated by measuring, as a function of biasing voltage, the bias current i_{bias}, the bulk capacitance C_{bulk}, the bulk resistivity ρ_{bulk} and the interstrip capacitance $C_{interstrip}$, on the N side. Figure 3 shows $i_{total} = i_{bias} + i_{guard} = f(V)$ in black, $1/C^2_{bulk} = f(V)$ in blue and $\rho_{bulk} = f(V)$ in red.

The $i_{total} = f(V)$ graph shows a weak slope in the plateau area due to the nominal guard ring leakage. The $1/C_{interstrip\ N} = f(V)$ graph (not represented) shows the same plateau as the $i_{total} = f(V)$ graph.

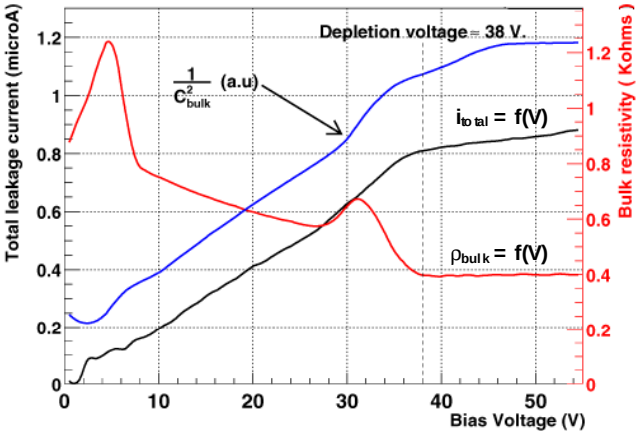

Fig. 3: Operating range of DS SSD STAR171.

The same detector has been assembled in a module and connected to the front-end electronics. Noise measurements of the strips provide also a good information on the depletion. Figure 4 shows the $i_{total} = f(V)$ graph in black squares and the RMS noise graph in red dots. They all show the same plateau for the same voltage range.

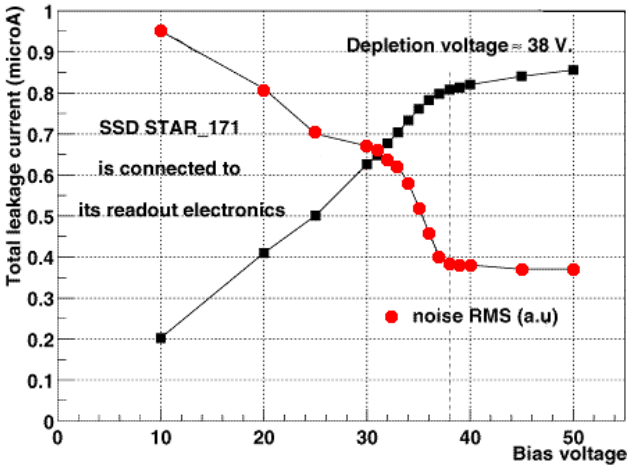

Fig. 4: Total current and noise as a function of voltage.

So, it has been demonstrated that the only $i_{total} = f(V)$ measurement provides consistent and exhaustive information on i_{bias}, i_{guard}, V_d, V_{bd}, and V_{op}.

Figure 5 represents the number of detectors as a function of their possible operating voltage. This plot is made by considering a detector as "1" inside the operating range and as "0" outside this range and adding together these values over the whole set of measured detectors.

This graph shows that about 75% of the detectors can theoretically be operated with a unique common biasing voltage of 53 volts. Once the V_{op} has been defined, one can measure the corresponding operating total current i_{tot} whose mean value 1.65 µA appears in figure 6.

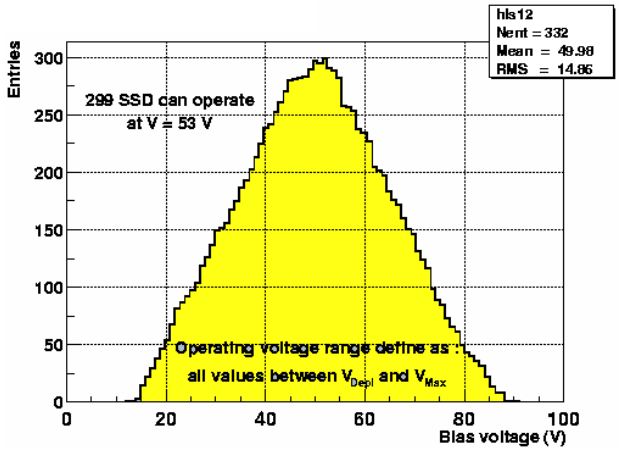

Fig. 5: Sum of the operating ranges of 332 detectors.

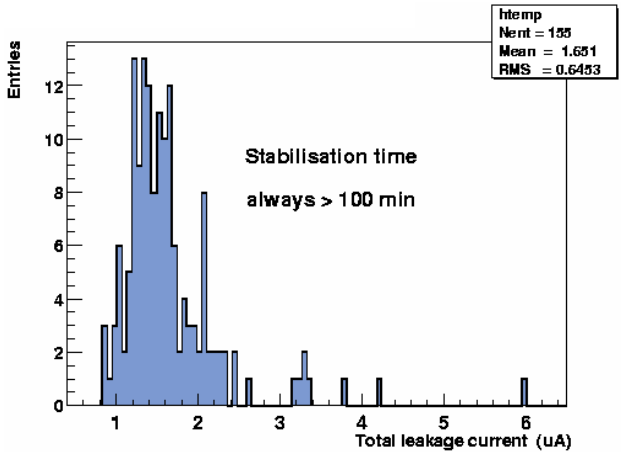

Fig. 6: Total current i_{tot}: mean = 1.65µA

2.2 Coupling capacitors

The FEE is located on two separate but identical hybrids, one connected to the N side and one to the P side of the detector by means of capacitors integrated on top of each strip for AC coupling. Dielectric characteristics of the insulation, i.e. leakage current and capacitance, are obviously important for detection efficiency and data consistency. Measuring both leakage current and capacitance enables cross checking, the latter also validating the contact quality. During these measurements, a DC voltage of 100 V is applied across the capacitor to check if it stands the operating voltage. These parameters are measured for each strip by stepping through the contact pads with a test probe. This option avoids all the switching and probe card problems without taking significant more time yet. The corresponding data are registered in the data base. The related distributions are presented on figure 7 left for the P side and right for the N side. A capacitor is considered as dead if it leaks or if the capacitance is out of range. The mean number of dead capacitors is below 2 units on both sides. 85% of the DS SSDs have at most 4 dead capacitors on both sides i.e. less than about 0.5% of the 768 strips of each detector side.

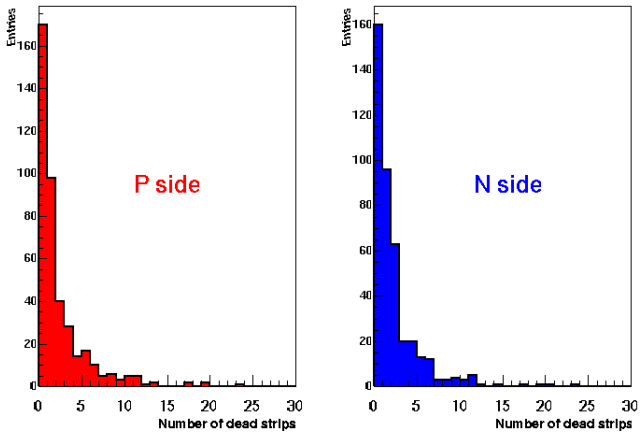

Fig. 7: Dead capacitors on P side (left) and N side (right)

2.3 Detector quality

Compiling the results of these different measurements provides a global information about the quality of the produced detectors as presented on table 1.

Class	Quality	Nb. of SSDs	%
1	Perfect	258	65%
2	Good	74	18%
3	>10 dead strips/side	20	5%
4	High currents	14	3%
5	Dead	20	5%
6	Vd > 55V	13	3%
7	To be tested again	1	/

Table 1: Quality of the 400 measured DS SSD.

2.4 Strip leakage current

For production, we consider that the $i_{total} = i_{bias} + i_{guard} = f(V)$ measurement described in 2.1 and the coupling capacitor measurement described in 2.2 are consistent to characterize a detector. We chose to avoid any disturbance of the main detector by DC test pads. If needed, it is possible to measure the strip leakage current on a test structure located on the same wafer as the real detector. It should be below 5 nA/strip. Furthermore, if the number of leaking strips becomes significant, the problem is detected by the measurement of i_{bias}. So, the strip leakage current is not measured in production, mainly for throughput reasons.

3. ALICE128C FRONT-END CHIP

Each detector module includes two FE hybrids including each 6 FE ALICE128C chips [1], [3], [9]. So producing 400 detector modules for STAR (320 on the experiment + spares) requires 12x400=4800 working chips. 6000 tested chips have been ordered at AMS, the test being a rough test made on the wafer. After cutting, sorting in boxes and TABing of these chips onto microcables, they are measured again in our laboratory

before sending for TABing onto the hybrids and detectors. Testing of these chips has been made easy by integrating inside the chip, from the design level, JTAG operated remote access to all the digital and analog parameters and also to a programmable on-chip pulse generator for each analog channel [14].

3.1 Manufacturer production and test on wafer

From 6000 tested production chips ordered at AMS, we got 5656 "good" chips, 5355 "bad" inked chips having been rejected by the rough wafer tests.

3.2 The use of microcables

The TABed microcables, providing electrical connection between the DS SSD and the FE chips and between the FE chips and the hybrid, allow for a mechanical freedom in the positioning of the hybrids supporting the FE chips versus the detector. Au layered Cu microcables (17 µm Cu on top of 70 µm Kapton) are used for STAR [3] whereas Al microcables (14 µm Al on top of 12 µm Kapton) will be used for ALICE [4]. Their use eases also the chip test and avoids the use of the probe station.

3.3 Laboratory test of the TABed chips

The accurate testing of these chips is then made at the laboratory after TABing of the chips onto microcables and mounting them in a plastic tests frame for easy handling and testing. So, the chip in its plastic carrier [3] plugs easily into the test socket of the automated chip test equipment presented in figure 8. The overall duration of the automated test is below 5 minutes per chip. The test results are recorded into the production database for later use.

The test includes 7 main steps.

- Power the chip and check "+i" and "–i" which should both be negligible.
- Test the digital part of the chip by means of JTAG.
- Bias the chip by sending via JTAG the 7 analog operating parameters.
- Check again "+i" which should stay at about the previous level and "–i" which should increase by 20 mA.
- By means of JTAG, switch one analog channel to transparent mode, pulse it with the on-chip pulse generator and register the sampled analog positive and negative output.
- With "0" input, make acquisition of the 128 channels for pedestal registration.
- With the on-chip pulse generator, pulse sequentially each analog channel with positive and negative pulses with values of +100, +250, -100 and –250 and register the corresponding outputs.

The measurement of 87 TABed production chips provided 83 good chips and 5 bad ones including 1 with overcurrent, 1 with 24/128 dead channels 2 with 2 dead channels and 1 with 1 dead channel. Plots of the other parameters are not represented as they present a very narrow dispersion around the nominal value. The 94% yield after the wafer tests corresponds mainly to cutting, handling and TABing.

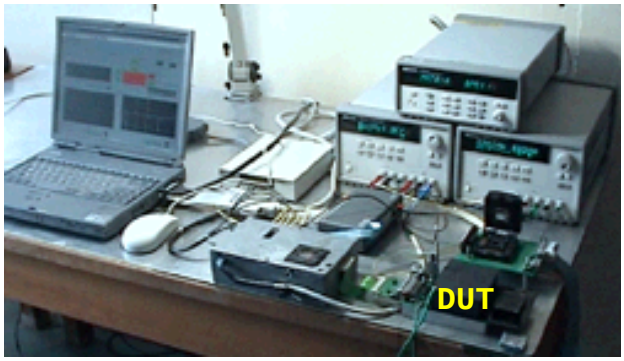

Fig. 8: ALICE128C chip automated test equipment

4. COSTAR CONTROL CHIP

The COSTAR control chip has been designed for remote JTAG monitoring and control of various analog and digital parameters [15]. Basic feature includes on-chip temperature measurement, which is especially important for air-cooling, and on-chip power supply voltage measurement. It includes also detector guard and bias current monitoring. One COSTAR is located on each STAR hybrid.

Testing of the COSTAR bare chip is performed on the probe station by means of a probe card and an automated test equipment. Calibrating of the on-chip temperature sensor is performed during the same process. Results are provided to the production data base. From 351 tested chips, 311 are "good" and 40 "rather bad".

5. THE ASSEMBLED MODULE

The test of the 400 assembled modules for STAR and 1800 for ALICE requires automation and optimizing. The basic aims are to get inside the data base, the operating parameters and location of each channel of each module. This includes an automated diagnosis of all the channels, the identification and location of each disturbed channel for any reason and the characteristics of the working channels in terms of gain and also of on-chip pulse generator calibration.

The defective channels can suffer from noise mainly related to a leaking strip, they may be shorted together with their neighbor, they may not be connected, they may be connected to a strip with a dead coupling capacitor, they correspond to a dead amplifier channel either with a dead input (blocked channel) or with a dead amplifying chain.

For diagnosis, one gets the inputs from the production data base corresponding to the measurements made on the components before assembling. One also pulses the amplifiers for testing them "in-situ" by means of the

JTAG operated on-chip programmable pulse generator. In the test equipment developed at IReS, we systematically pulse also the whole detector chain by means of a pulse light source scanning the surface of the detector to produced located calibrated charges inside the detector.

After deconvolution, the information coming from the

- components tests recovered from the data base,
- noise acquisitions,
- on-chip pulse generator acquisition and
- light pulse acquisition of the triggered detector

is cross-checked for a very accurate diagnosis of the assembled detector modules and finally, the diagnosis results are again stored into the data base. Figure 9 shows this test equipment, the Device Under Test (DUT) being inside the black box for protection against external light.

Fig. 9: The automated module test equipment.

To achieve this goal, full control and data acquisition are required for the module as well as opto-insulation of the electronics connected to the floating side and also motion control of the light source.

6. CONCLUSION

The existing TABed DS SSD modules have been previously validated for their main characteristics on various beam tests, focused on geometric resolution, signal to noise ratio [1], [9] and radiation hardness [11]. Now, for producing these modules, a set of automated test benches has been developed for the various tests at the different steps of assembling, of the components as well as sub-assemblies, complete modules and soon complete ladders supporting a number of modules. Their operation efficiency has been demonstrated. They are now applied to the STAR modules. On the ALICE detector modules, slight changes have been made. The DS SSD strip angles have been slightly changed to +7.5 and –27.7 mrad instead of ±17.5 mrad to minimize the ambiguity problem, a new HAL25 hardened FE chip has been designed and the ALICE modules have to meet the water-cooling requirements. Adapting the existing test equipments to the ALICE detector module should imply minor changes only.

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