Analogue Read-Out Chip for Si Strip Detector Modules for LHC Experiments

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Abstract

We present a 128-channel analogue front-end chip SCTA128 for readout of silicon strip detectors employed in the inner tracking detectors of LHC experiments. The architecture of the chip and critical design issues are discussed. The performance of the chip has been evaluated in detail in bench tests and is presented in the paper. The chip is used to read out prototype analogue modules compatible in size, functionality and performance with the ATLAS SCT base line modules. Several full size detector modules equipped with SCTA128 chips have been built and tested successfully in the lab with β particles as well as in beam tests.

I. INTRODUCTION

The LHC operating conditions present a great challenge to the front-end electronics of Si trackers for experiments designed for high luminosity physics. Historically most collider experiments have so far used full analogue readout front-ends for Si trackers and vertex detectors. This method allows individual treatment of data in each channel with optimised and adaptable software and thereby the most detailed control and monitoring of the whole system. Analogue readout is to a large extent immune to external electromagnetic pickup (common mode) since common mode noise can be fully eliminated with software. The price to pay for this safety is a heavier load on data transmission from the detector over optical links, both in bit rate and in the required number and quality of the links.

The ATLAS Semiconductor Tracker has adopted a binary scheme for the readout of silicon strip detectors as the baseline. The binary architecture allows a more compact design and has the advantage of a much reduced data transfer rate with more chips using a single optical link. This architecture is, however, not immune at all to common mode noise and so is very sensitive to external electromagnetic interference.

In this paper the ATLAS back-up solution, the SCTA128 chip will be presented. The SCTA128 chip is an example of analogue readout architecture for silicon strip detectors, which meets all basic requirements of the LHC experiments. It comprises five basic blocks: front-end amplifiers, analogue pipeline (ADB), control logic including derandomizing FIFO, command decoder and output multiplexer. The chip has been manufactured in the DMILL process, the same as used for the binary chip ABCD [1], [2]. The front-end is a fast transimpedance amplifier, using a bipolar input transistor and providing pulse shaping with peaking time of 25 ns.

The design and the performance of the chip will be presented. The basic chip performance has been evaluated on a test bench. An analogue prototype module consisting of two 6.4 cm x 6.3 cm ATLAS baseline detectors read out by 6 SCT128A chips has been built. The chips are mounted on a ceramic hybrid connected to the sensors in an end-tap configuration. The pitch adapter needed to match the strip pitch of 80 μm and the pitch of input pads on the chip, which is 60 μm, is integrated on the hybrid. The performance of the module, which has been tested with a Ru β-source and in a 100 GeV pion beam, will be discussed.

II. CHIP ARCHITECTURE

Figure 1 shows the block diagram of the SCTA128 chip.

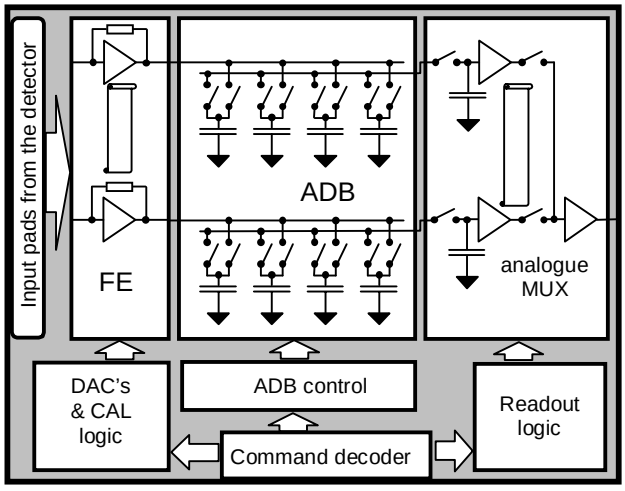

Figure 1: Block diagram of the SCTA128 chip.

The SCTA128 chip comprises the following building blocks: 128 channels with front-end amplifiers, Analogue Memory (ADB) with the capacity to store 128 analogue samples, control logic providing a derandomizing function (up to 8 events), command decoder and fast

analogue multiplexer to output serial data. In addition to the basic functional blocks, internal calibration circuitry containing an 8-bit DAC to control the calibration level has been implemented to improve the testability of the chip. Four 5-bit DAC's for the bias of the analogue part of the chip have been implemented in order to compensate the drifts after irradiation and optimise chip performance for various parameters (noise level for a given detector capacitance, required dynamic range etc.). The details of the chip architecture and basic principles as well as readout protocol may be found in previous publications [3], [4].

III. RESULTS FROM THE PROTOTYPE CHIP SCTA128HC.

In this section we briefly review results from the performance of the prototype chip SCTA128HC already presented in previous publications [3] and [4]. We present also the latest results obtained from beam tests of a full size (13cm length) ATLAS type detector modules.

The SCTA128HC chip was manufactured in the middle of 1998 – an early stage of DMILL stabilisation process at TEMIC. Looking at the noise figure obtained with this prototype chip it should be remembered that the typical value of the BJT beta was in the range of 100 (today 250) which obviously has an impact on the value of parallel noise. In addition to that the SCTA128HC chip suffers from two technological problems not fully understood at the time of submission. One was the susceptibility of the RHV type resistors (used in the front-end) to the radiation which makes a whole design non-rad-hard. The second one was the problem of the parasitic coupling through the substrate of the chip (described in [5]) limiting the phase margin and causing an oscillation. The temporary solution cancelling that effect was thinning and metallization of the chip backplane done in an extra process step outside the foundry.

A. Basic chip performance – results from a single chip evaluation board.

Basic requirements for the front-end performance are the speed, noise figure and the dynamic range. In the SCTA128HC chip there is no direct access to the output of the FE amplifier however the pulse shape can be evaluated by scanning the delay of the calibration signal with respect to the phase of the ADB sampling clock. Figure 2 shows the example of a delay scan normalised to the absolute time scale for one particular front-end channel. The injected charge was 6 fC. The obtained 25 ns peaking time matched the design value well.

Figure 3 shows the gain linearity for one particular channel of the chip. The gain is in the range of 28 mV/fC and the linearity is kept up to 12fC, which is enough for tracking applications.

The overall distribution of the gain in one SCTA128HC chip is presented in figure 4. The RMS spread of the gains is about 3%, which is acceptable for tracking applications. The spread between the on-chip calibration capacitors (100 fF in each channel) and the calibration resistors (one for calibration line) also contributes to this distribution.

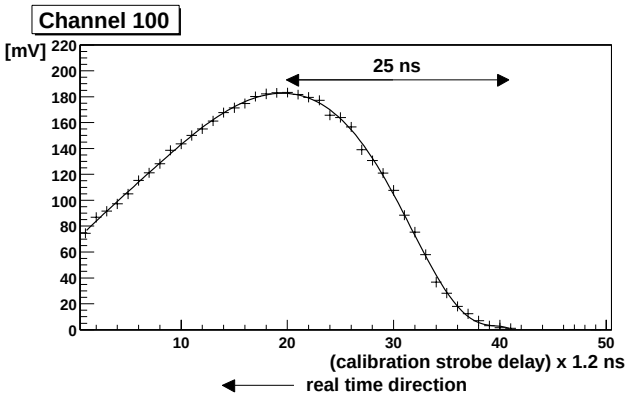

Figure 2: Pulse shape at the multiplexer output obtained from the delay scan.

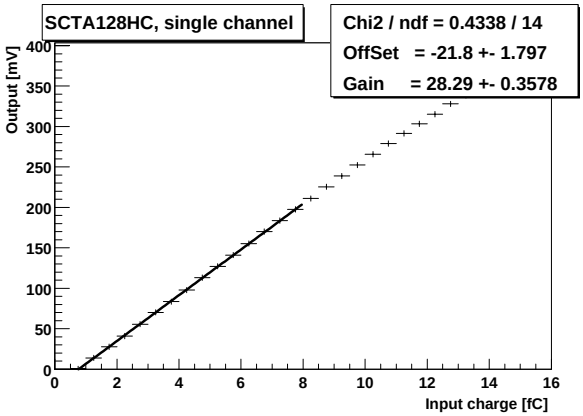

Figure 3: Gain linearity for a single channel of SCTA128HC.

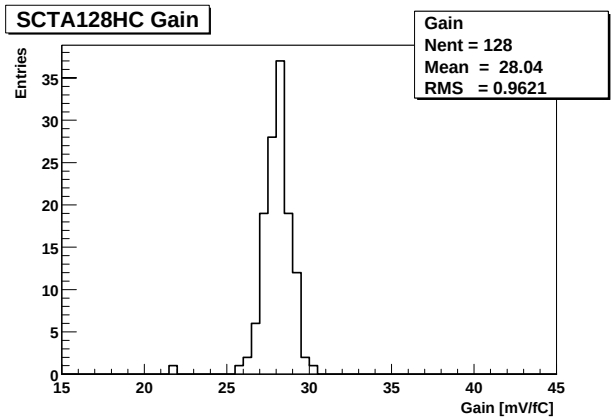

Figure 4: Distribution of the front-end gain in one SCTA128HC chip.

The noise measurements of the front-end have been performed for the whole chip running with a 40 MHz clock sampling data to the analogue memory and for random readout of the ADB cells. This way any pedestal variation between ADB cells was included in the overall noise performance. Noise slopes for different values of the input transistor bias are shown in figure 5.

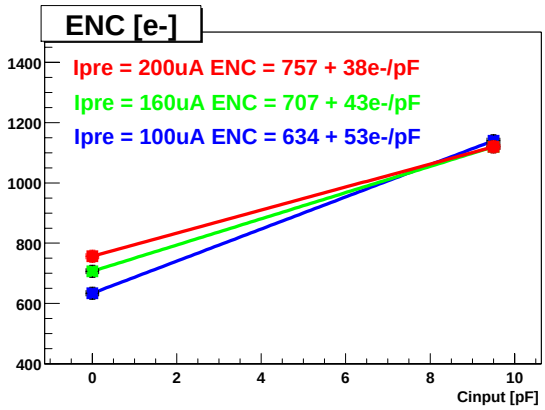

Figure 5: ENC noise slope for different bias conditions of the input transistor.

As already mentioned the ENC value for zero input capacitance is limited by relatively low beta (around 100) of BJT transistors manufactured at TEMIC in 1998.

The spread of the pedestals in the analogue memory has a direct impact on the overall noise performance of the whole chip. Since the analogue memory performs a simple voltage sampling, the pedestal spread will contribute, as an extra noise source uncorrelated with the input noise. The distribution of the pedestals in the ADB for a typical channel of the SCTA128HC is shown in figure 6.

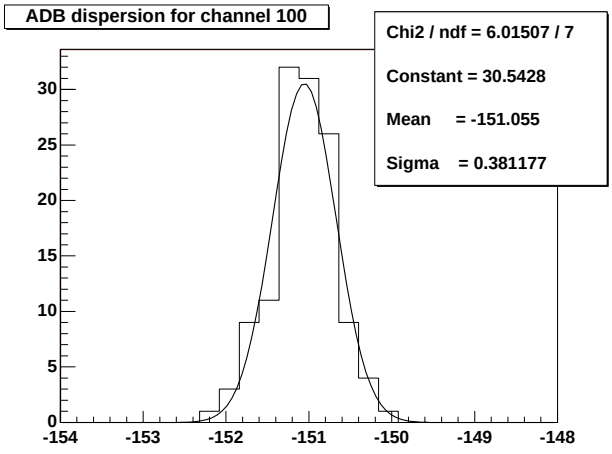

Figure 6: Pedestal distribution of 128 cells in one typical channel of SCTA128HC chip readout with 40 MHz clock.

The value of 0.4 mV has to be compared with 28 mV/fC gain, which gives additional noise contribution in the range of 100e- ENC uncorrelated with the input noise. The measurement has been done using 40 MHz readout clock for the output multiplexer, which is synchronous with the ADB sampling clock. Using slower multiplexer clock increase activity of the digital signals asynchronous to the sampling clock which couple through the chip substrate to the inputs of the front-end and increase the pedestal spread. The typical value of RMS pedestals spread in analogue memory for lower readout frequency is in the range of 1.2 mV.

B. Performance of the ATLAS type detector modules equipped with SCTA128HC chips.

To demonstrate the feasibility of using the SCTA128 chip as a backup solution for the ATLAS SCT several modules compatible with the size and number of electronic channels of the baseline binary module have been built. A 6 chip ceramic hybrid holding 2 silicon detectors of size 6.3x6.4 cm (ATLAS baseline design) in end-tap configuration is shown in figure 7.

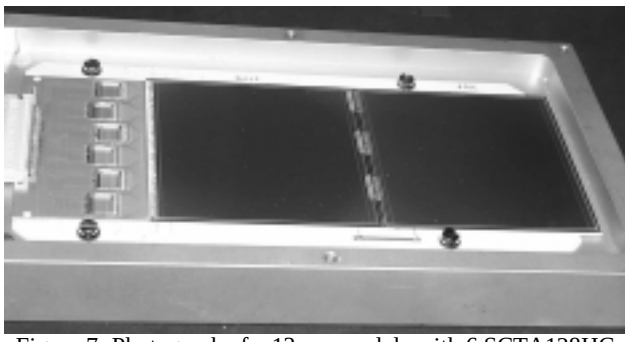

Figure 7: Photograph of a 13-cm module with 6 SCTA128HC chips.

The modules were tested in the SPS beam line, which provides 100 GeV pions. A standard procedure described in [4] was applied to extract spatial resolution, efficiency and noise occupancy for the tested modules. The signal over noise distribution of the found clusters on 13-cm strips regions is shown in figure 8. The most probable value is about 20, which is sufficient to provide high particle detection efficiency while keeping the noise occupancy well below ATLAS requirements.

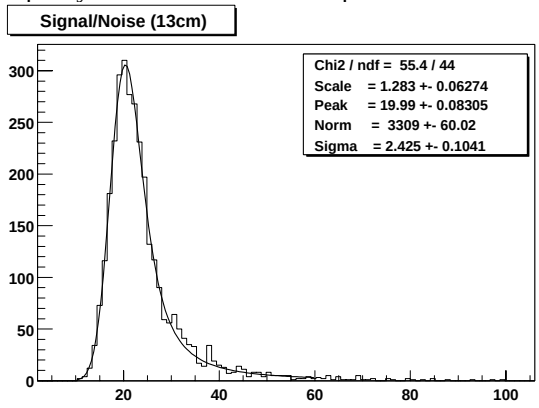

Figure 8: Signal to Noise for 13 cm Si strip detector.

Since the detectors used in the modules were optimised for binary electronics the majority of events were single strip hits. Thus the spatial resolution obtained in the beam test is as expected for binary electronics σ = 23 μm (detector pitch 80μm/$\sqrt{12}$). Selecting events with double strip clusters (~15% of total number of events) one can obtain a spatial resolution of about 3μm. The distributions of residuals separately for single and double hit clusters are shown in figure 9.

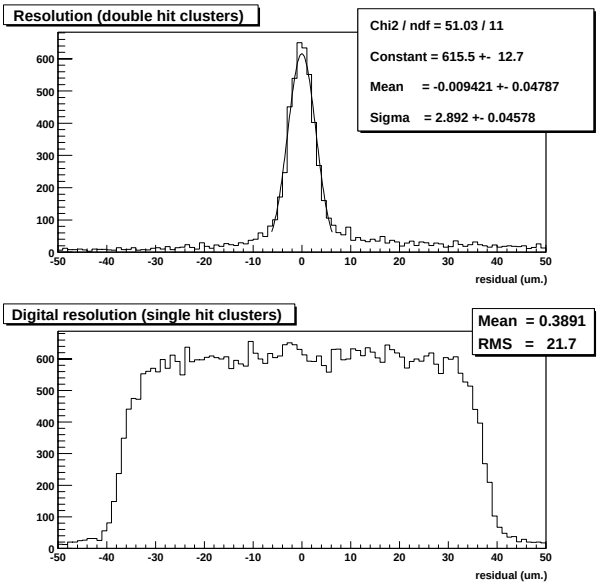

Figure 9: Resolution of the 13-cm silicon strip module equipped with the SCTA128HC chip.

An important parameter characterising overall performance of the detector module is the noise occupancy for a given tracking efficiency. The plot showing the noise occupancy versus tracking efficiency for tested modules is presented in figure 10. For the efficiency calculation only events with one well-reconstructed track were considered.

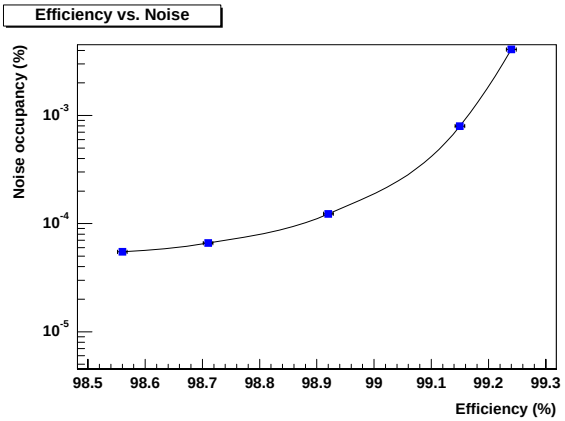

Figure 10: Noise occupancy versus efficiency for 13-cm silicon strip detector module equipped with SCTA128HC chips.

IV. SCTA128VG - A NEW VERSION OF THE ANALOGUE CHIP.

Although the SCTA128HC chip has been used successfully over the last two years to build detector modules one should not forget that this prototype has some limitations and should not be considered as a final version of the analogue chip. Development of the binary chip ABCD in the same DMILL technology has had a big impact on the planned improvements in the new version of the analogue chip. Apart from the changes implied by modified technology such as the introduction of new rad-hard resistors (RBXB type) and new structures for the input pads with a screening layer preventing parasitic coupling through the substrate, several improvements in front-end part have been done. In April 2000 a new version of the analogue chip SCTA128VG was submitted to the TEMIC foundry. The first stage of the preamplifier is identical to the ABCD3T design (the noise performance and radiation hardness is already proved).

In the new design of the shaper stage we focused on the improvements of PSRR, immunity to spread of the process parameters, temperature and drifts during irradiation. The overall gain of the front-end stage was tuned to 50 mV/fC to be completely safe against the ADB pedestal spread and possible excess noise at the level of data transmission outside the chip. The stability of the front-end parameters with respect to temperature is improved by using a new band-gap reference for the bias DAC's. Several changes in structure of the biasing and grounding of the front-end stage both on schematic and at the layout level have been applied to improve the stability of the chip working in detector system with millions of channels.

The schematic of one channel of the front-end amplifier is shown in figure 11. The input stage formed by the bipolar transistor loaded with a PMOS current source is followed by a common collector buffer and enclosed with the transresistance loop. A DC coupled booster amplifier provides extra amplification before the shaper stage. A booster amplifier is a two-stage BiCMOS amplifier with negative feedback defined by a resistive network. It provides good stabilisation of the gain with respect to the technological parameters, temperature and power supply as well as high bandwidth for relatively small power consumption (0.25 mW for nominal bias). The same structure is replicated in the shaper stage, which is AC coupled to the preamplifier in order to prevent propagation of DC offsets implied by the spread of process parameters and drifts after radiation. An extra AC coupling is used in the front of the output buffer in order to provide a well-defined DC level at the output of the chip before the optical link. One can notice the separation between grounds and supplies lines, especially the extra connection for the emitter of the input transistor – the most sensitive node of the circuit – to avoid parasitic coupling via the common inductances of the bond wires. The bias lines used in various part of the amplifier are separated and filtered to avoid parasitic coupling of the high dynamic range signals to the more sensitive front part of the circuit.

During the optimisation of the circuit we have placed special emphasis on the reduction of possible variations in the circuit parameters with operating conditions (temperature and power supply) and the variations of process parameters from run to run. In order to illustrate possible effects we show in figure 12 and 13 simulation results for gain and peaking time respectively for various combinations of power supply (±10%), operating temperatures (0 and 80°C) and corner parameters defined by the technology vendor.

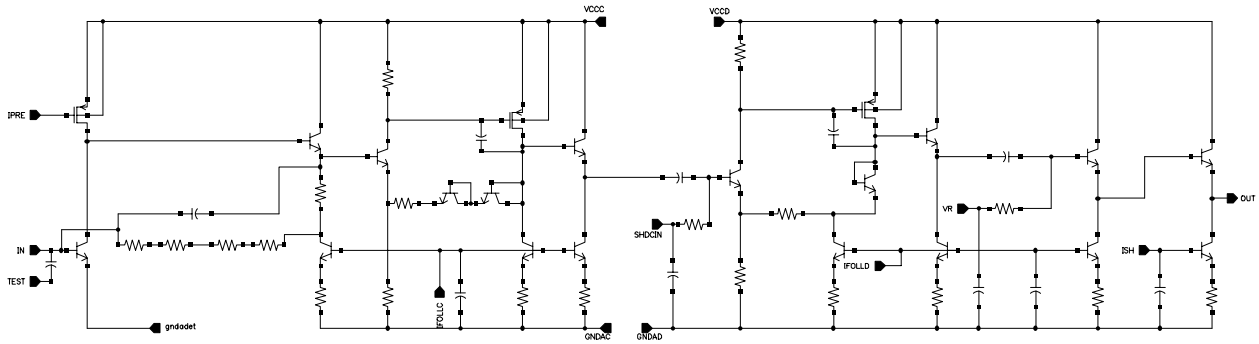

Figure 11: Schematic of one channel of the SCTA128VG front-end amplifier.

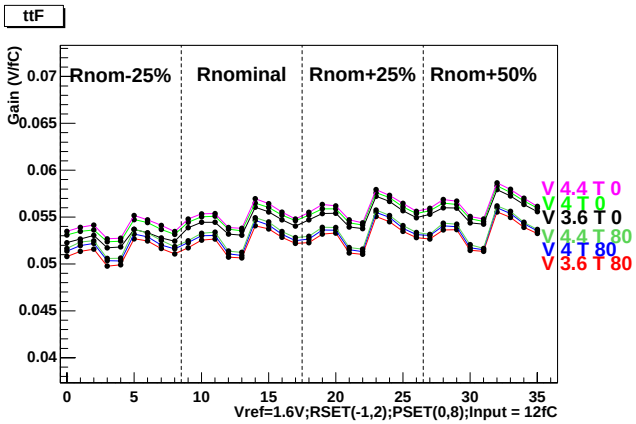

Figure 12: Evolution of gain [V/fC] with variation of the process parameters (resistors –25% - +50%, CMOS corner parameters, temperature from 0 to 80°C, power supply ±10%). The variation of the parameters are from batch to batch. For a given batch the matching of the device parameters on chip/wafer is much better.

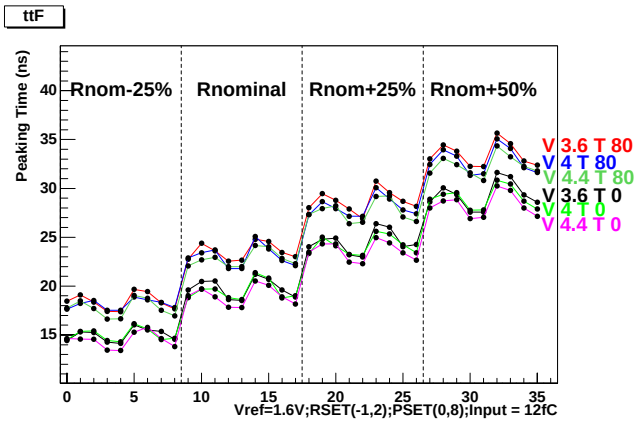

Figure 13: Evolution of the peaking time [ns] with variation of the process parameters (resistors –25% - +50%, CMOS corner parameters, temperature from 0 to 80°C, power supply ±10%)

The corner parameters include also worst case combinations of initial parameters and expected radiation effects after a total dose of 10 Mrad. The performance of the circuit for 50% higher values of the resistances is only shown as an example of the robustness of the circuit since the maximum expected deviation is 25%.

V. Conclusions

The SCTA chip is an implementation of full analogue readout architecture compatible with the requirements for readout of silicon strip detectors at LHC experiments. Using prototype SCTA128HC chips a number of silicon detector modules matching ATLAS specification has been built and successfully tested in the SPS beam. A new version of the analogue chip – the SCTA128VG is expected soon back from the foundry.

VI. References

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