

# The APVD Readout Circuit for DC-Coupled Silicon Detectors

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## Abstract

The APVD[1,2], an integrated circuit for the front-end electronics of DC-coupled silicon detectors has been developed and produced in the radiation-hard process DMILL for the CMS experiment. This paper reports very briefly on the final test results, more details will be published elsewhere.

## I. SUMMARY

The APVD\_DC contains, like other members of the APV[3] family 128 identical analogue channels, each composed of a low noise preamplifier, a CR-RC shaper, an analogue pipeline of 160 cells and a signal processing stage[1,2]. A current compensation circuit is added in every preamplifier to sink the leakage current coming from a DC coupled silicon detector.

The circuit has been tested and measured in the presence of significant DC-currents up to 11 microampere, without deterioration of the analogue performance of the circuit like pulse shape or dynamic range. The noise increases by about 300 ENC as is shown in figure 1, small compared to the additional shot-noise.

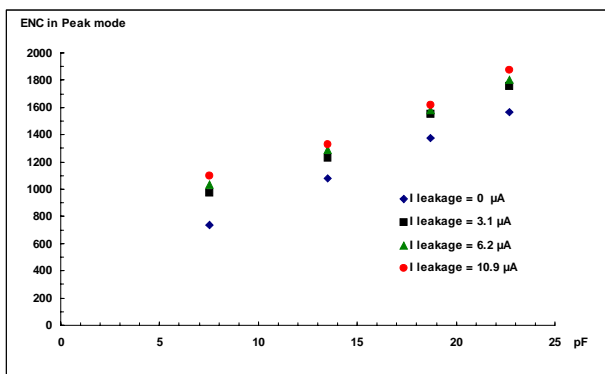


Figure 1: The measured noise in the presence of different external currents.

Previous APVD circuits suffered from an instability problem in the analogue stage of the circuit occurring at nominal bias values. The analogue baseline of the new

modified circuit is absolutely stable also under extreme operation conditions, like twice as high bias currents, demonstrating that the implemented solution stops indeed the oscillation of the circuit as we previously claimed based on extensive simulations of the circuit[4].

The linearity and pulse shape are well within the specifications as previous versions of the circuit. More details on the performance will be available in[5].

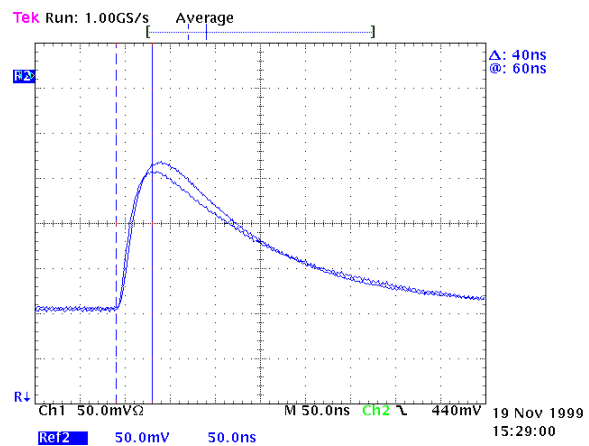


Figure 2: Pulse shape at nominal and increased bias conditions.

## II. REFERENCES

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- 5 to be published