Front-End electronics for ATLAS Pixel detector.

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Abstract

Large advances have been made over the last years in the development of rad-soft readout chip prototypes, closing the first phase of the ATLAS pixel [2] demonstrator programme. The next step of this programme is aimed at realizing a full scale pixel front-end chip using two rad-hard technologies. The DMILL chip has been received in Oct. 99 and the deep submicron design is currently under development. Measurements on the DMILL ATLAS pixel Front-end chip are presented.

I. INTRODUCTION

The electronics subgroup of the ATLAS pixel detector has pursued an iterative programme of design development over the last 3 years. The initial phase of this demonstrator programme was aimed at realizing ATLAS specification front-end chips using radiation-soft technologies, the designs of which could then easily be adapted for fabrication at rad-hard foundries. First realistic prototypes were designed in 2 parallel efforts (Europe and US) in 97/98, producing a rad-soft AMS prototype (FE-A/FE-C) and a rad-soft HP prototype (FE-B). Throughout 98/99, more than 60 single chip assemblies and 10 electrically functional modules were produced and have been studied extensively in lab and during 7 testbeam periods at SPS. All of the ATLAS requirement issues (except for the radiation hardness) were addressed in detail such as noise, threshold dispersion, timewalk, digital/analog crosstalk, power supply rejection... with very encouraging results [3]. A unified design approach has been adopted for rad-hard front-end chips, i.e. all working on the same design to be implemented in 2 rad-hard processes. The DMILL (FE-D) and the deep submicron rad-hard designs maintain the spirit of the demonstrator programme (i.e. pin compatibility, same pixel pitches...) and combine features of both FE-A/C and FE-B. FE-D has been received in Oct. 99 and the deep submicron design is currently under development.

II. THE MODULE INTEGRATION

A. *The Module concept*

The ATLAS pixel module consists of a n+ on n-type silicon sensor attached to 16 Front End (FE) chips. The sensor substrate contains approximately 47000 pixels sized at 50µm*400µm, leading to a total active area of 16.4 × 60.8 mm². An additional module controller chip (MCC) is used for control of the FE chips and eventbuilding. The MCC collects the data of all 16 FE chips, builds complete module events and sends them through a pair of serial links to the data acquisition (DAQ). It also provides control of the FE chips, i.e. slow control signals used to reset the chip and to write the configuration data into the FE registers.

The event data transmission between the module and the data acquisition system, along with the reception of trigger, timing and chip configuration, use optical fibers. For this purpose, the reception is carried out by the DORIC chip along with a pin diode and the emission is performed by the VDC chip driving a VCSEL laser diode [4].

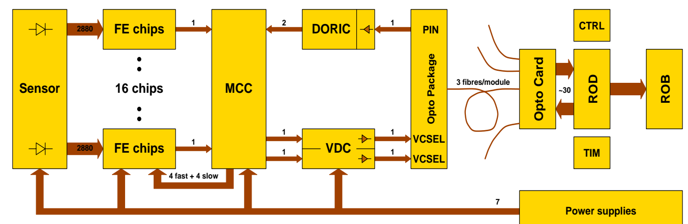

Figure 1: From the sensor to the data acquisition system...

B. *The Flex hybridization ("chip-down" approach)*

This is the baseline choice for the inner, outer layers and forward disk. As shown in Figure 2, Front-end (FE) backplanes are in direct thermal contact with the support structures.

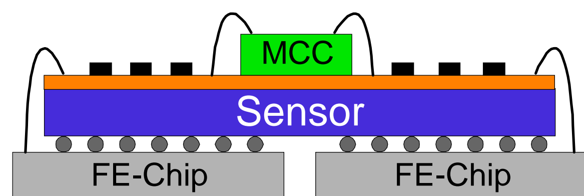

Figure 2: cross-section of the flex module

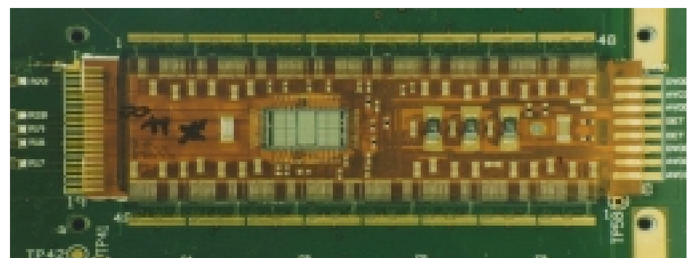

Figure 3: photograph of the flex module

The sensor (which is bump-bonded to the FE-chips) has the Kapton bussing piece glued to its backplane. The FE chips protrude along the long edges of the sensor thus facilitating

wire-bond connections up to the kapton hybrid. The Kapton layer has the role of supporting the Module Controller Chip (MCC), optical transmission, reception devices, local decoupling and the distribution of clocks/data between the MCC and FEs.

C. *MCM-D hybridization ("chip-up" approach)*

This is the baseline choise for the B-layer. Bussing structures and individual pixel via are actually fabricated on the surface of the sensor itself in up to 5-layers of Cu/BCB (post-production lithographic process). As shown in Figure 4, MCC and other surface-mount components are bump-bonded to the detector surface along with the FE chips thus eliminating wire-bonds.

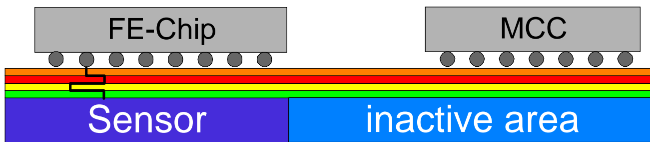

Figure 4: cross-section of the MCM-D module

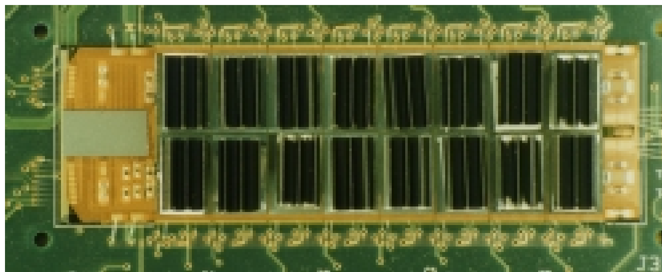

Figure 5: photograph of the MCM-D module

This technique also allows more flexible mapping of the pixel electronics channels to the sensor implants. A unique pixel implant length and pitch can be used everywhere instead of the ganged pixels and stretched pixels used in the standard layout to cover the regions between FE chips. This reduces hit ambiguities and improves the point resolution in these regions.

III. THE FRONT-END CHIPS

A. *Introduction*

First realistic prototypes were designed in 2 parallel efforts (Europe and US) in 97/98, producing a rad-soft AMS prototype (FE-A/FE-C) and a rad-soft HP prototype (FE-B). The final chip, in its rad-hard version, is a common design between LBL, CPPM and Bonn with the analog part of FE-A/C and the readout architecture of FE-B. The goal is to provide two radhard options using two different technologies. The DMILL chip, submitted to a rad-hard foundry (Atmel) has been received on Oct. 99, tested and re-submitted. The second design, using a deep submicron technology, is currently in preparation.

The FE chips have a size of 7.4 mm * 11 mm and include close to 700,000 transistors. The active area is divided into 18 columns of 160 rows of pixels sized at 50µm * 400µm. Pairs of columns are grouped together for readout sharing purpose. Each pixel contains a control section providing injection, masking and threshold adjust features. The column-pair data is stored in 24 End-of-Columns buffers located below the active area until the arrival of a level 1 trigger. The trigger managment, serializer, digital control, global analog blocks, along with the protocoll circuitry for communication with the MCC are implemented at the bottom of the chip [4].

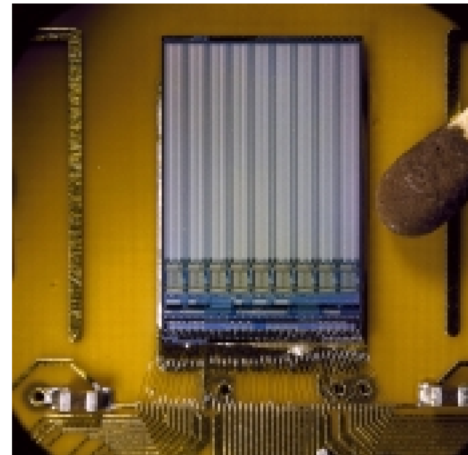

Figure 6: photograph of the FE chip

B. *Measurements on FE-D*

1. <u>The analog part</u>

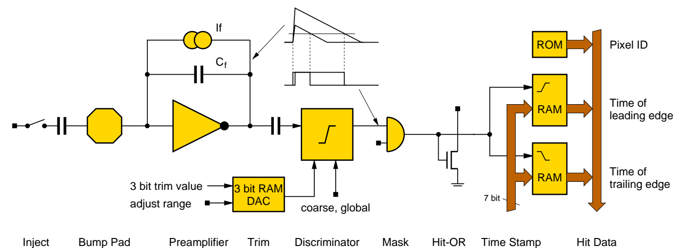

Figure 7: The analog part

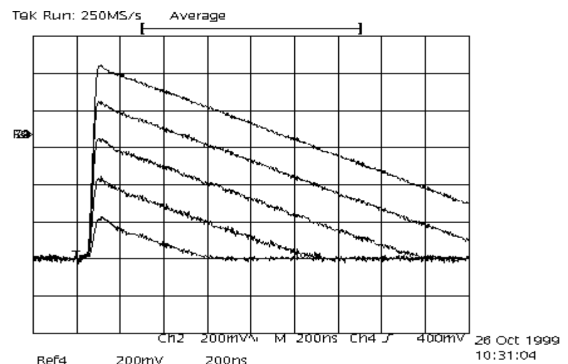

Figure 8: Analog output signal of the preamp (step of 5000e-)

The analog part (see Figure 7) contains a charge sensitive preamplifier AC-coupled to a fast discriminator. The feedback

capacitor of 3.5fF is discharged by a constant current, making the output pulse shape proportional to the input charge as shown in Figure 8.

The pulse width of the discriminator is therefore a measure of the analog pulseheight by using the Time Over Threshold (TOT) technique. This information is recorded by the readout system which performs the subtraction between the leading and the trailing edge of the discriminator pulse. The TOT information is sampled at the bunch crossing rate, providing a 4 (5) bit analog resolution. As shown in figure 9, the feedback current can be varied by means of a global DAC, so that the trade-off between analog resolution and pixel occupancy can be easily found.

Figure 9: Effect of various feedback current on the preamp shape

The global threshold of the discriminator is externally set whereas an individual threshold adjust is locally stored (3bit trim DAC with adjustable range) in order to achieve a good threshold uniformity (see figure 10).

Figure 10: Threshold scan with different DAC values

A known charge can be injected in every pixel by means of a 12 fF injection capacitance so that threshold, noise and crosstalk measurement are easily performed. In parallel, each pixel can be masked so that a single channel can be isolated for measurement or noisy channels can be turned off in normal operation.

An analog test chip has been implemented beside FE-D aiming at investigating more precisely the analog performance. This chip contains all basic analog blocks required to work properly the analog front-end. Several additional features have been added in order to simulate the sensor behavior before and after irradiation. For example, the tunable capacitance network at the preamp input and the leakage current injection capability help us to predict the evolution of threshold, noise, timewalk and crosstalk before attaching the sensor. Figure 11 depicts the evolution of the ENC against the input capacitance. The noise without capacitive load is well below 100e and the slope is 40-60 e/100fF. The typical noise expected for a detector capacitance of 300fF is 180-230 electrons.

Figure 11: ENC as a function of input capacitance

2. The digital readout

Figure 12: Principle of the time stamp readout

The hit information must be stored on the FE chip for 100 to 120 clock cycles until a trigger signal generated by other

subdetectors of ATLAS selects interesting events for readout. The time of a hit is therefore recorded using the time stamp mechanism illustrated schematically in Figure 12. Several tasks are active simultaneously:

- A 7 bit wide time stamp counter (using gray coding) operated at the 40 MHz bunch crossing rate generates the time reference which is distributed to all pixels in the chip. When a pixel is hit, the times of the rising and of the falling edge of the discriminator output signal are stored in latches in the pixel. A hit is flagged in the pixel as soon as the falling edge has arrived.

- All hit flags in a column are connected by a fast asynchronous priority scan which indicates to an arbitration unit that a hit is present in the column. This initiates a cycle to transfer the two time stamps and the address of the uppermost hit pixel into one of 24 end of column (EoC) buffers at the bottom of the column pair. The speed of this transfer can be programmed for best performance after irradiation. Once the transfer is complete, the hit flag in the active pixel is cleared and the priority scan searches for the next hit in the column. The left and the right halves of the column pair share the time stamp and readout busses and are served alternately.

- The (programmable) latency value is subtracted from the time stamp and compared continuously to the rising edge information stored in every EoC buffers. The hit is cleared if the values coincide and no trigger signal is present. If a trigger selects the event, it is flagged with a 4 bit trigger number and kept in the buffer for readout. The trigger is recorded in a FIFO.

- Pending triggers in the FIFO initiates a readout cycle. The 9 EoC buffer blocks are scanned for valid hits with the correct trigger number. Every matching hit is retrieved, serialized and sent to the MCC through the serial link. It is then cleared from the EoC buffer. The event is terminated with an end of event sequence if no more hits are available for the processed trigger number.

3. Additional blocks

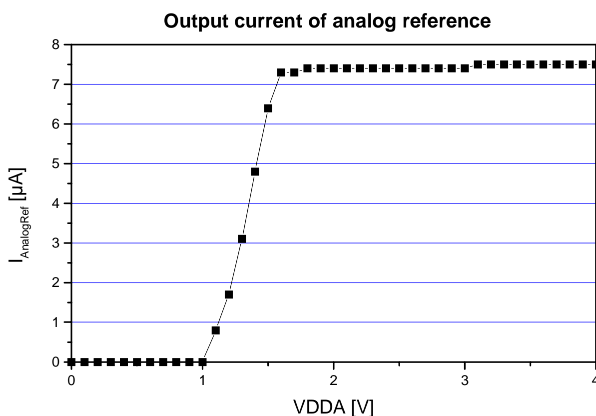

Figure 13: Output current versus voltage supply

A current reference is used to supply a constant current to all internal DACs and LVDS input and output circuits.

As depicted in Figure 13, measurement of the output current versus (analog) supply voltage shows that the current reference reaches operation point at only 1.6V and its saturation value is approximately 7.5µA, which is sufficiently close to the design goal of 8.0µA.

Several current mode DACs are used to supply the bias currents for the analog part, the threshold setting trim and the injection chopper. Measurements show perfect linear characteristics and successful operation at low supply voltages providing a large safety margin.

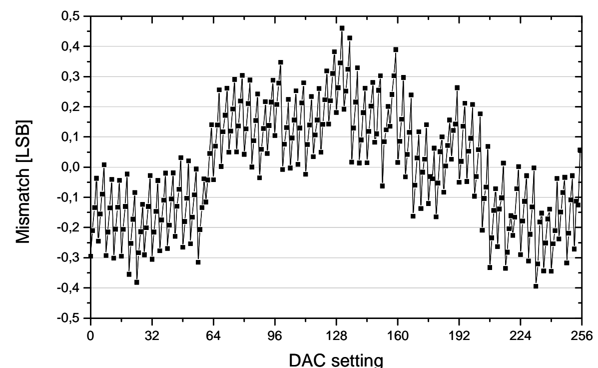

Figure 14: Integral non-linearity of the current mode DAC

As shown in Figure 14, the integral non-linearity, expressed in LSB, is well below ±0.5LSB which proves good linearity. So far, the largest mismatch observed in DACs is 0.6LSB.

An internal injection chopper provides a voltage step which can be programmed with 8 bit resolution. The chopper can be operated in a 'low' mode where charges up to 6000 electrons can be generated with high resolution for precise threshold setting. Larger charges of up to 60,000 electrons can be generated in 'high' mode to measure, for example, the time response. The chopper along with the reference and the DAC are designed such that it should remain unaffected by changes in the process parameters after irradiation.

4. FE-D status

All analog and digital blocks work except:

- A short in the Vth amplifier which has not been detected by the verification tools. The trace between the block and the array is cut for the tested chips and the voltage is externally supplied.

- There are missing or under-sized buffers at 3 locations.

All these errors have been easily fixed in the second DMILL generation (FE-D2) which is currently processed.

Nethertheless, serious yield problems have been observed in 2 locations using dynamic circuitry (the pixel shift register and the pixel readout). All other locations using dynamic logic don’t exhibit this problem and have correct yield. According to the high density in these regions, the main hypothesis is a certain configuration of several rules set at the minimum.

After few months of investigation with extensive lab tests and simulations, the best candidate to explain the behavior of the non-working parts has been found to be a leakage path between drain and source of one given transistor. This hint has been confirmed after the test of several chips sent to the Focussed Ion Beam (FIB) surgery (see Figures 15 and 16).

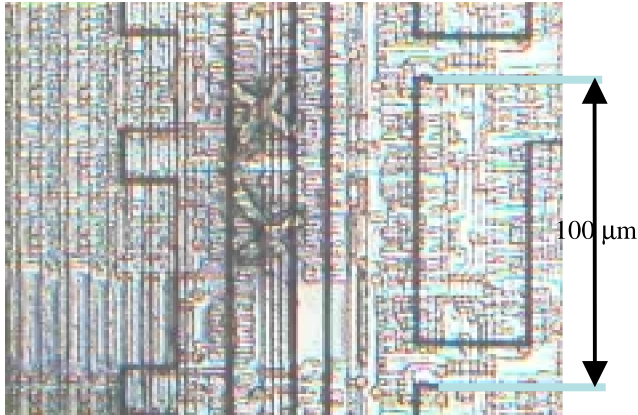

Figure 15: photograph of FE-D after FIB surgery

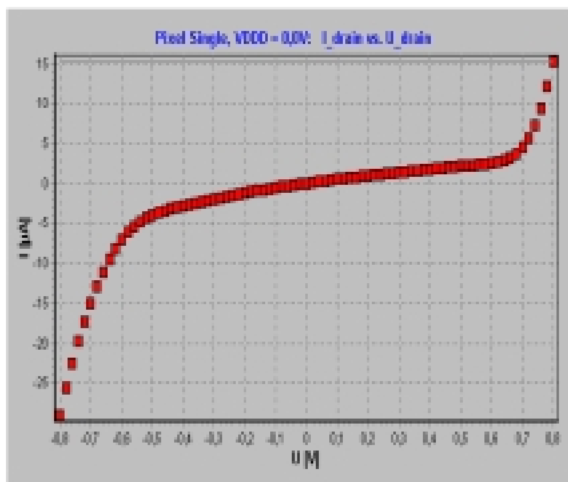

Figure 16: Resistive behavior of the faulty transistor

IV. Conclusion

All of the ATLAS-requirement issues have been addressed with very encouraging results. Tests on FE-D show up a peculiar low yield in 2 locations of the chip. Extensive lab measurements have enabled to isolate faulty transistors and to get more insight into the failure mechanism. A close study between ATMEL and labs is being pursued. A new DMILL engineering run has been submitted, and should return in Oct. 2000. This run contains 2 front-end versions (the previous front-end used for process comparison & process monitoring and a full static version) along with the DMILL version of the Module Controler Chip, the DORIC & VDC chips, Process Monitor chips and analog test chips.

In addition to the DMILL standard engineering run, a second experimental run has been launched. In this run, three different variations of the standard processing will be made, on 9 sub-groups of wafers, in order to isolate the sources of poor yield observed in the initial FE-D run.

We had also prepared a submission of a complete pixel FE chip for the Honeywell SOI4 process, but this work was abandoned after very substantial cost increases from the foundry made access to this process unaffordable for anyone besides military contractors.

We are presently transfering all of our designs to 0.25u deep-submicron process using radiation-tolerant layout techniques in order to have a second vendor in case our low yield problems with DMILL cannot be resolved quickly.

V. References

[1] Member institutes of the ATLAS pixel collaboration: State University of New York, Albany, USA; LBNL and University of California, Berkeley, USA; Physikalisches Institut Universitat Bonn, Germany; Experimentelle Physik IV, Universitat Dortmund, Germany; Dipartimento di Fisica e INFN Genova, Italy; University of California, Irvine, USA; Centre de Physique des Particules de Marseille, France; CERN, Geneva, Switzerland; Dipartimento di Fisica e INFN Milano, Italy; NIKHEF, Amsterdam, Holland; University of New Mexico, Albuquerque, USA; University of Wisconsin, Madison, USA; Max Planck Institut, Munchen, Germany; University of Oklahoma, Norman, USA; Academy of Sciences of the Czech Republic, Institute of Physics, Prague, Czech Republic; Charles University, Faculty of Mathematics and Physics, Prague, Czech Republic; Czech Technical University, Faculty of Mechanical Engineering, Prague, Czech Republic; University of California, Santa Cruz, USA; Fachbereich Physik, University of Siegen, Germany; University of Toronto, Canada; Dipartimento di Fisica e INFN Udine, Italy; Fachbereich Physik, Bergische Universitat, Wuppertal, Germany.

[2] Technical Design Report of the ATLAS Inner Detector, CERN/LHCC 97-16 (1997).

[3] J. Richardson for the ATLAS pixel collaboration, The ATLAS pixel on-detector electronics, workshop on electronics for LHC experiments, Snowmass 1999.

[4] P. Fischer for the ATLAS pixel collaboration, Pixel electronics for the ATLAS experiment, PIXEL 2000 workshop, Genoa 2000.