Design of a Readout Chip for LHCb

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Abstract

This paper details design and simulation of a prototype of a 128 channel readout chip for the LHCb experiment.

The chip named *Beetle* fulfills the requirements of the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detector[1] of LHCb.

Section 1 summarizes the requirements on a LHCb frontend chip. Section 2 presents an overview of the chip's architecture and features. Section 3 describes the various components and shows simulation results. Section 4 gives an outlook on future plans.

I. Introduction

The requirements on a LHCb frontend chip are mainly determined by the use in the silicon vertex detector (table 1). The signal of a minimum ionizing particle (MIP) in 150 μm silicon corresponds to 11,000 electrons. This input signal has to be shaped with a peaking time of less than 25 ns. The peak voltage is sampled at 40 MHz. The L0 triggers occur at an average rate of 1 MHz, whereas consecutive triggers are possible. The readout of a triggered event has to be performed in less than 900 ns.

For the frontend chips a dose rate of more than 2 Mrad per year is expected, which leads to a total accumulated dose of more than 10 Mrad in 5 years of operation [1].

Table 1: Requirements on a LHCb vertex detector readout chip [1].

readout pitch	40-60 μm
detector capacity	10 pF
required S/N	> 14
irradiation dose	> 10 Mrad
max. power consumption	< 4 mW/channel
peaking time	≤ 25 ns
pulse spill-over	$\ll 30\%$ after 25 ns
dynamic range	$\pm$ 110,000 electrons ($\pm$ 10 MIP in 150 μm silicon)
required linearity	$\leq 5\%$ up to 10 MIPs
L0 trigger rate	1 MHz
consecutive L0 triggers	yes
multi event buffers	16
max. latency	4 μs (160 $\times$ 25 ns)
readout time	≤ 900 ns/event

II. Chip Architecture

The *Beetle* chip (fig. 1) is an analogue or binary pipelined readout chip. It implements the RD20 frontend electronics architecture [2] and provides binary signals for a trigger decision.

The chip integrates 128 channels. Each channel consists of a low-noise charge-sensitive preamplifier and an active RC-CR pulse shaper. The risetime of the shaped pulse is 25 ns with a 30% remainder of the peak voltage after 25 ns. A comparator per channel provides a binary signal. It features a configurable polarity and an individual threshold level. Four neighbouring comparator channels are ORed together, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signal (LVDS) ports at 80 MHz. Either the shaper or comparator output is sampled with the LHC bunch-crossing frequency of 40 MHz into an analogue pipeline with a programmable maximum latency of 160 sampling intervals and an inte-

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[1] In case multianode photomultipliers are used.

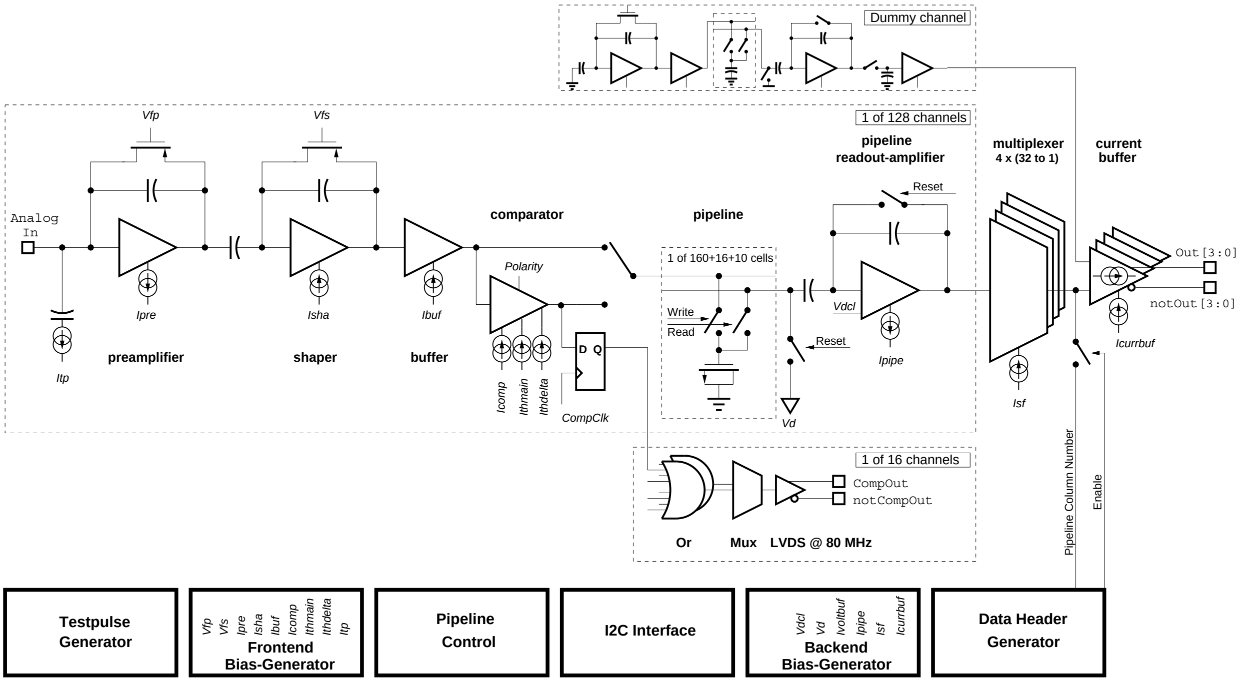

Figure 1: Schematic block diagram of the *Beetle* readout chip.

grated derandomizing buffer of 16 stages. The pipeline cells are realized as NMOS gate-capacitances. The stored charge is transfered to the multiplexer via a resetable charge-sensitive amplifier. Different readout modes have been implemented. Analogue data can be multiplexed with up to 40 MHz onto 1 port or 4 ports. In binary readout mode multiplexing runs at up to 80 MHz on two ports. The output of a dummy channel (fig. 1) is subtracted from the analogue data to compensate common mode effects. Current drivers bring the serialized data off chip. The chip performs deadtimeless readout in 900 ns at an average trigger rate of 1 MHz. All amplifier stages are biased by forced currents. On-chip digital to analogue converters (DACs) with resolutions of 10 bits generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height has been implemented for each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard $\mathrm{I^2C}$-interface. All digital control and data signals (except for the $\mathrm{I^2C}$-ports) are routed via LVDS ports.

The chip is fabricated in a 0.25 μm standard CMOS process. The die size is 6.1×5.5 mm^2. The analogue input pads have a pitch of 41.2 μm. If no comparator outputs are required, pads on the top and bottom side of the chip need not to be bonded. This allows an overall pitch of 50 μm putting the chips side by side. Fig. 1 shows a schematic block diagram of the chip. The layout of the *Beetle1.0* version is depicted in fig.2.

Fig. 3 shows the simulation result of the complete

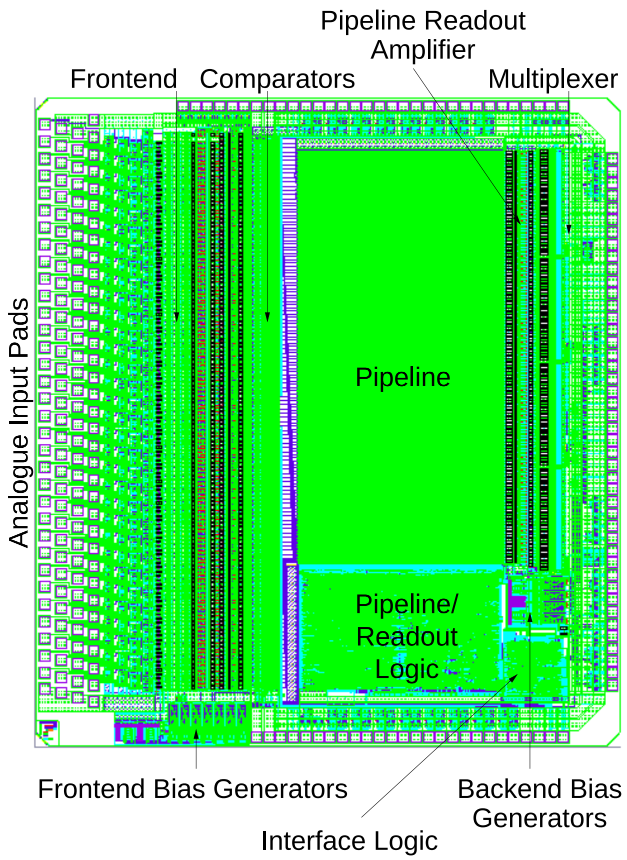

Figure 2: Layout of the *Beetle1.0* chip version. The die size is $(6.1 \times 5.5)\,\mathrm{mm}^2$.

analogue chain. The total gain is 54 μA/MIP at 10 pF load.

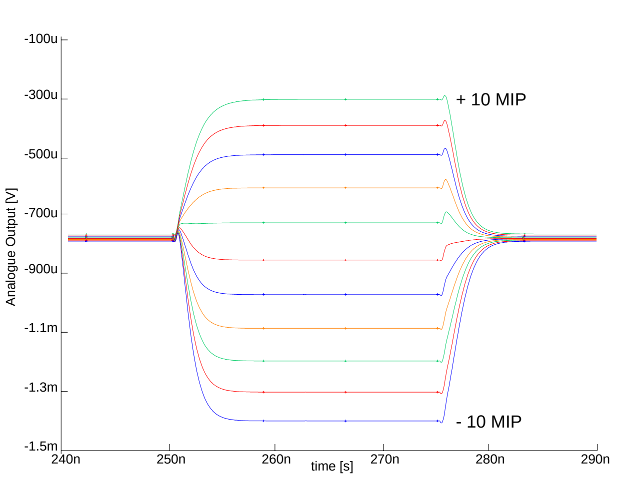

Figure 3: Simulation result of the complete analogue chain. Only one polarity of the differential output is shown. The total gain is 54 μA/MIP at 10 pF load.

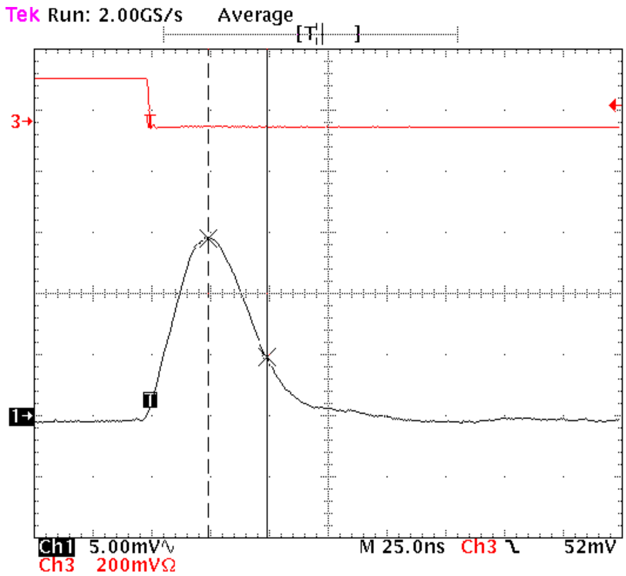

Figure 4: Measured transient response on a delta-shaped signal of 1 MIP (11,000 e$^-$) at a capacitive load of 10 pF.

Several design measures have been taken to withstand the radiation level [3]. The integration in a 0.25 μm process with a gate oxide thickness of 60 Å reduces the threshold voltage shift under irradiation. Enclosed gate structures for NMOS transistors have been used to suppress an increase in leakage current under irradiation. A consistent use of guardrings should minimize the rate of single event effects [4]. Forced bias currents are used in all analogue stages instead of fixed node voltages.

III. Components

A. *Frontend Amplifier*

The frontend amplifier circuit consists of a low-noise, low-power charge-sensitive amplifier, an active CR-RC shaper and a source follower as output stage (see fig. 1).

This frontend has already been submitted and tested on an earlier prototype chip [5]. Fig. 4 shows the measured transient response on a delta-shaped signal of 1 MIP (11,000 e$^-$). The risetime is 26 ns with a 30 % remainder of the peak voltage after 25 ns, achieving a gain of 17.25 mV/MIP.

The equivalent noise charge (ENC) has been measured to be 303 e$^-$ + 33.6 e$^-$/pF at a bias current of 600 μA. The total power consumption of the frontend is 1.88 W/channel.

B. *Comparator*

The comparator circuit consists of an integrator, a threshold generator and a discriminator (fig. 5). The integrator extracts the DC-offset of the shaped pulse with a time constant of 5 μs. This offset varies from channel to channel and is added to the threshold voltage. The threshold level is adjustable per channel with a resolution of 3 bits. The discriminator itself consists of 2 differential amplifiers. With a polarity signal the comparator output can be inverted.

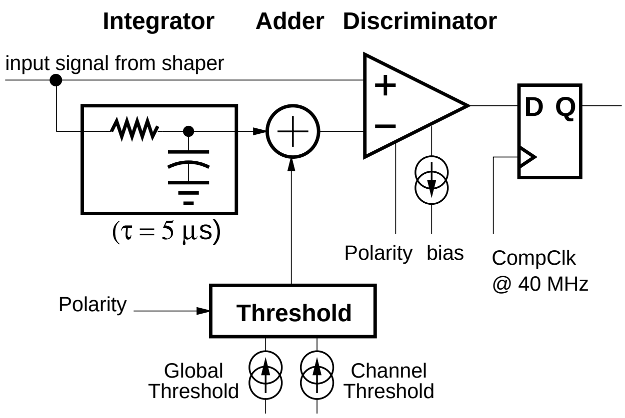

Figure 5: Schematic block diagram of the comparator.

C. Analogue Pipeline and Pipeline-Readout-Amplifier

The pipeline is an array of (129×186) analogue memory cells. The sampled voltage is stored on the gate-capacitance of an edgless NMOS transistor of 1 pF.

In case of a trigger signal the stored charge is transfered to the multiplexer's hold capacitance via a resetable charge-sensitive amplifier.

D. Multiplexer

The multiplexer is a simple sample- and hold-stage with a source follower. It is structured into four (32:1)-multiplexers, which can be grouped in order to realize three different readout modes:

1. Analogue readout in 900 ns on 4 ports
2. Binary readout in 900 ns on 2 ports
3. Analogue readout on 1 port (for applications with less demanding readout speed requirements).

E. Control Logic

The control logic has been functionally described in *Verilog HDL*, synthesized with *Synopsys*, and placed and routed with *Silicon Ensemble* using 3 metal layers.

The logic controlling the readout is essentially identical to that of *Helix128-3.1* [2] [6].

The chip's slow control interface is a standard mode I^2C-slave device performing a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I^2C-bus, is assigned in a self-programming procedure on power-up. Therefore the chips sharing one I^2C bus line are in addition connected in a daisy chain. All 33 registers are readable via this interface.

The total number of flip-flops in the control circuitry is 683 (readout part: 500, interface part: 183).

F. Bias Generators

The bias generators are divided into a frontend and a backend bias block. All digital to analogue converters (DACs) have resolutions of 10 bits. The voltage DACs use an R-2R resistor-ladder. The current DACs use PMOS transistors as current sources. A current source consisting of cascoded transistors with a 20 kΩ reference resistor provides a reference current.

The bias circuitry has been already submitted and tested on an earlier prototype chip [5]. The current sources on 20 tested prototype chips show a variation of less than 5%.

[2] *Helix128-3.1* is the latest member of the Helix readout chip family used in the experiments HERA-B, ZEUS and HERMES at HERA.

IV. Future plans

It is planned to do single event upset (SEU) measurements with the *Beetle1.0* chip version at the tandem accelerator of MPI for Nuclear Physics in Heidelberg.

At the beginning of 2001 it is intended to submit a version 1.1 of the readout chip which will additionally feature

- a JTAG boundary scan architecture
- SEU detection and correction mechanisms
- the programmability via the trigger line
- mask registers for testpulse and comparator
- a fail safe token scheme for the daisy chain readout.

Status reports and further test results will be available under [7].

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