

Radiation Tolerance Evaluation of the ATLAS RPC Coincidence Matrix Submicron Technology

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Abstract

The Coincidence Matrix ASIC is the central part of the ATLAS level-1 muon trigger in the barrel region; it performs the trigger algorithm and data read-out. The ASIC will be mounted on dedicated boards on the Resistive Plate Chamber detectors. The chosen technology has to guarantee complete functionality in the ATLAS RPC radiation environment. Radiation tests have to satisfy the radiation tolerance criteria proposed by the ATLAS Policy on Radiation Tolerant Electronics. The ATLAS standard test methods has to be followed in order to guarantee both total dose and single event effects tolerance.

A frequency multiplier ASIC was used for technology evaluation and radiation tests. The chip is a low jitter programmable clock multiplier, realised in 0.25 μm CMOS technology. This frequency multiplier is intended to be used in the Coincidence Matrix ASIC as a macro, to perform the internal clock frequency multiplication. Radiation test results will be presented.

I. INTRODUCTION

The Coincidence Matrix ASIC (CMA) performs the ATLAS barrel level-1 muon trigger algorithm and Resistive Plate Chambers data read-out. ~ 4000 CMA will be mounted on dedicated boards on the RPC detectors. The CMA chip executes the timing and digital shaping of the signals coming from the RPC doublets, the high P_T and low P_T trigger algorithm, the data storage during level-1 latency, the trigger and data read-out generation, the storage of read-out data in derandomizing memory and the serialisation of read-out data [1] [2]. Figure 1 shows the trigger algorithm basic scheme.

The CMA is required to tag incoming hits with a time resolution greater than the bunch crossing period, and has an internal pipeline working at 320 MHz for this purpose. An internal clock multiplier is so required to perform frequency multiplication of the external 40 MHz clock.

The Fujitsu ULPM2 is a low jitter programmable clock multiplier, realised in 0.25 μm CMOS technology with triple well. A delay locked loop (DLL) provides the chip clock output, within a range between 40 MHz and 400 MHz. The multiplying factor is programmable between 2 and 32. Power supply is 2.5 V. The ULPM2 chip has been chosen as a

candidate for the CMA internal clock multiplier, and it is intended to be used as a macro in the CMA chip, to perform the 8x40 MHz internal frequency multiplication.

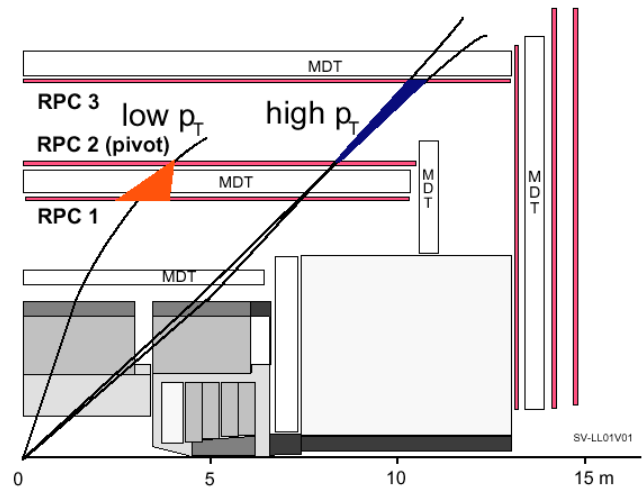


Figure 1: The high P_T and low P_T trigger scheme

Fujitsu released the macro for testing in a 120-pin QFP plastic package. The tests were intended to be useful for evaluating the Fujitsu technology, the radiation tolerance of the process, and the ULPM2 frequency multiplier functionality, so as to decide if the Fujitsu technology and the ULPM2 could both be used for the CMA chip. In order to test radiation tolerance of this deep submicron process, tests were repeated after gamma and proton irradiation. The technology has to guarantee complete functionality in the ATLAS RPC radiation environment.

II. ULPM2 TEST

A test board for the ULPM2 chip has been developed in Rome INFN lab. The ULPM2 input clock can be connected to an external generator or to a on board oscillator. A few switches select the macro control signals and initialisation registers. A special output signal is provided in the chip to monitor the status of the ULPM2 DLL lock.

A. Functionality test

The macro clock input has been connected to an external pulse generator, in order to monitor the output clock as a function of the input one. Clock functional range has been

first tested. The output clock working range, for all possible multiplying factors, has been verified. In order to monitor the DLL lock status, the ULPM2 lock signal has been connected to a transformer/shaper and then to a pulse counter. The chip has shown a correct functionality, in accord with the Fujitsu ULPM2 datasheet values [3]. Maximum measured output clock jitter is 25 ps RMS, 170 ps P-P.

In order to evaluate the frequency multiplier linearity, output clock has been monitored for different values of the input clock, in steps of 2 MHz, for a fixed multiplication factor equal to 8. The measured integral and differential non-linearity is less than 6%. ULPM2 output frequency standard deviation has been measured. RMS output frequency standard deviation is less than 5% the input frequency. No appreciable difference has been observed between different tested chips.

B. Total Ionising Dose test

For this test the ATLAS TID standard test method has been followed [4]. Two chips have been tested. The ULPM2 chip has been irradiated with a Cobalt 60 γ source. The Gammacell 220 High Dose Rate Research Irradiator has been used (facility from Istituto Superiore di Sanità, Rome). Dose rate during irradiation has been 481 Rad/minute.

The ULPM2 chip has been irradiated up to a total dose of ~ 300 kRad. Chip functionality, output clock jitter, frequency and amplitude has remained unchanged during irradiation. Differential and integral non-linearity has been measured after irradiation. Figure 2 and Figure 3 show differential and integral non-linearity before and after irradiation. DNL and INL measured values has not changed appreciably after irradiation. Power consumption has been monitored during irradiation, showing a final increase of $\sim 25\%$, as can be seen in Figure 4. Annealing measurements have been done, for simulating low dose effects. Measurements were done during ten days at room temperature, and then during ten days at 80°C . During annealing, the macro showed a correct functionality. After ten days at room temperature, power consumption was still 14% more than the one before irradiation (see Figure 5). Then, after ten days at 80°C , power consumption decreased down to 8% the original value (ten weeks at 80°C are requested for coming back at original values).

The radiation tolerance criteria proposed in the ATLAS TID test method for the RPC is

$$RTC_{\text{tid}} = SRL_{\text{tid}} \cdot SF_{\text{sim}} \cdot SF_{\text{ldr}} \cdot SF_{\text{lot}} \cdot 10y$$

where:

$SRL_{\text{tid}} = 3.0 \cdot 10^{-1}$ Gy/y (RPC worst location);

$SF_{\text{sim}} = 3.5$ (safety factor for simulation inaccuracies);

$SF_{\text{ldr}} = 1$ (safety factor for low dose rate effects);

$SF_{\text{lot}} = 4$ (safety factor for different lot);

10y = ten years of LHC working operation.

Using these values we obtain $RTC_{\text{tid}} = 4.2$ kRad, which is ~ 70 times less than the maximum total dose taken by the chip

during TID test. The calculated RTC_{tid} clearly shows that TID is not a problem in the RPC radiation environment.

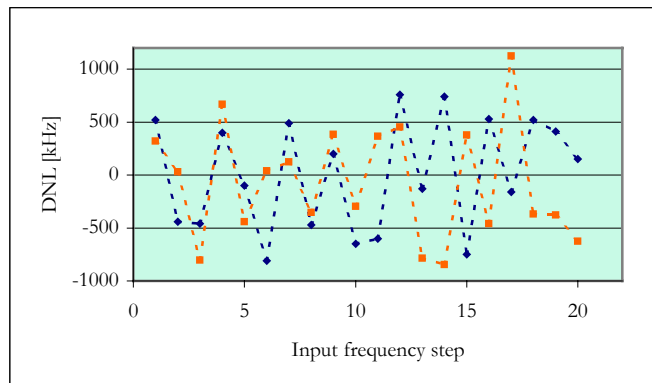


Figure 2: Differential non-linearity before and after irradiation

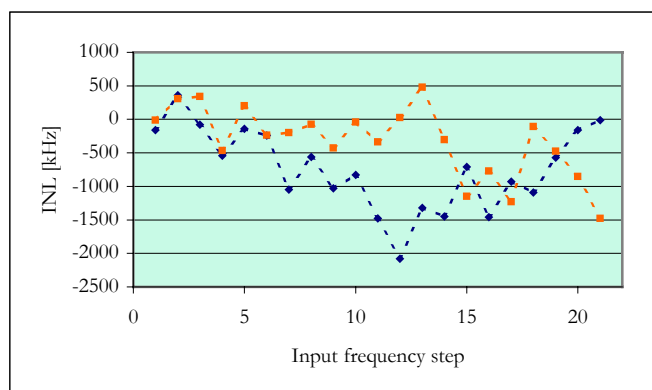


Figure 3: Integral non-linearity before and after irradiation

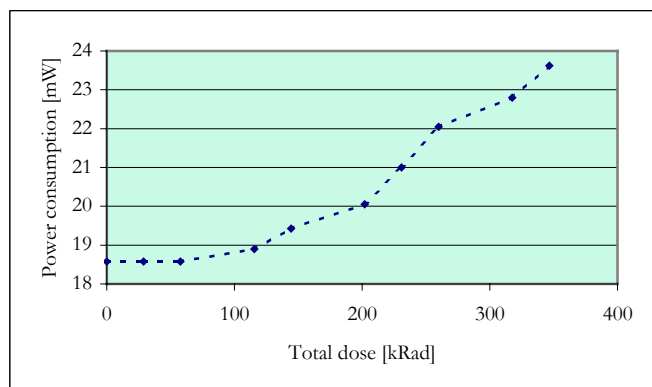


Figure 4: ULPM2 power consumption during irradiation

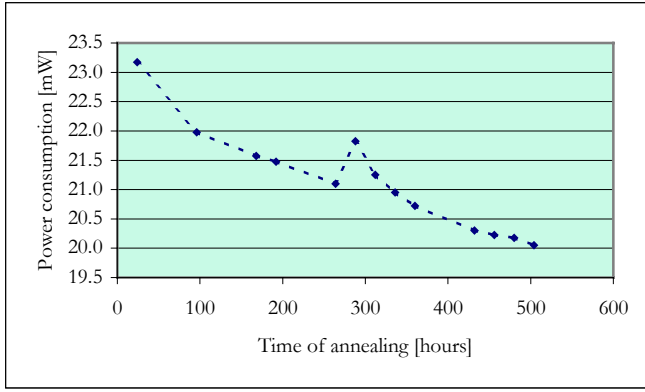


Figure 5: ULPM2 power consumption during annealing

C. Single Event Effects test

For this kind of test the ATLAS SEE standard test method was followed.

Irrad1 proton facility at CERN Proton Synchrotron (PS) was used. The proton beam forms a spot of (2×2) cm², and has an energy equal to 24 GeV. The proton flux at the centre of the beam is $(2 \div 9) \cdot 10^9$ cm⁻²s⁻¹. In order to have a reduced particle flux on the electronics to be tested, it is possible to place the test board outside the beam centre. In this case the total particle flux contribution comes from back-scattering particles and from the 24 GeV proton beam halo. Figure 6 shows Irrad1 back-scattering energy spectrum (values from FLUKA simulation). As can be seen from the histogram, the energy of the back-scattered particles is high enough to generate SEE in the irradiated chip.

The ULPM2 chip has been placed 10 cm far from beam centre, in order to have on the chip $\sim 1\%$ of the maximum flux during irradiation. With this reduced error rate a more easy error monitor and control is possible. Total irradiation time has been 6 hours, obtaining a total fluency on the ASIC equal to $1.38 \cdot 10^{12}$ h/cm² ($1.68 \cdot 10^{14}$ h/cm² at beam centre). No hard or destructive errors have been detected. Only soft SEU have been detected, coming from ULPM2 DLL loss of lock. The DLL has been able to recover the lock within 4 clock periods (100 ns), and so no reset has been necessary during irradiation. Figure 7 shows the measured error time distribution histogram.

Assuming that the effective cross-section for protons is constant up to 24 GeV [5], the number of foreseen errors in the ATLAS RPC radiation environment can be calculated with the following formula:

$$\text{soft SEU}_f = (\text{soft SEU}_m / \text{ARL}) \cdot (\text{SRL}_{\text{sec}} / 5 \cdot 10^7 \text{s}) \cdot \text{SF}_{\text{sim}}$$

where:

- soft SEU_f: foreseen rate of soft SEU in a given ATLAS location [soft SEU/s];
- soft SEU_m: total number of soft SEU measured during proton irradiation;
- ARL: Applied Radiation Level (integrated flux of 60÷200 MeV proton applied) [h/cm²];

- SRL_{sec}: integrated flux of hadrons with energy > 20 MeV in 10 years [h/cm²];
- $5 \cdot 10^7$ s: integrated beam time expected in 10 years of LHC operation;
- SF_{sim}: safety factor representing SRL_{sec} inaccuracies.

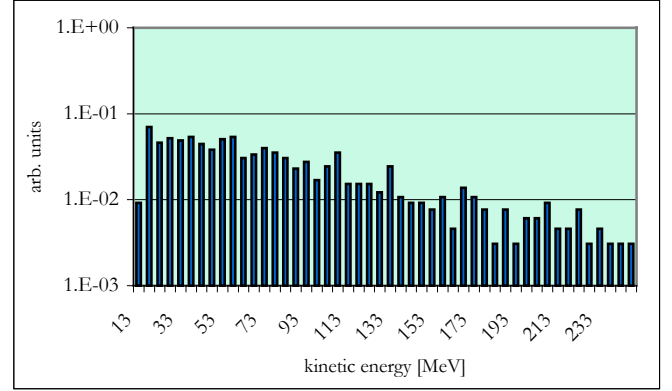


Figure 6: Irrad1 proton back-scattering energy spectrum

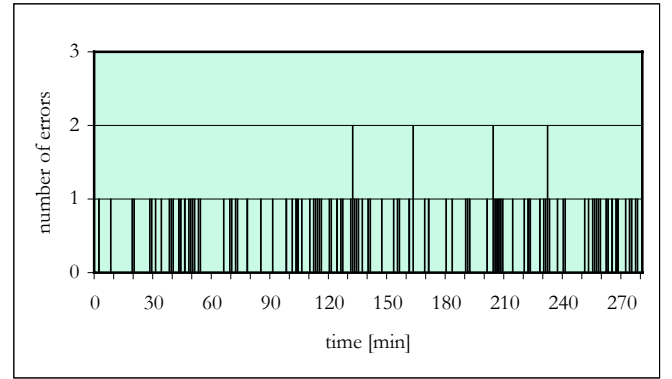


Figure 7: Number of measured SEU during 280 min. of irradiation

Using the formula we obtain:

$$\text{soft SEU}_f = 5.6 \cdot 10^{-8} \text{ soft SEU/s} = 4.8 \cdot 10^{-3} \text{ soft SEU/day.}$$

With this value we can calculate the foreseen dead time induced in the Coincidence Matrix ASIC by the ULPM2 soft SEU errors. Assuming to perform a CMA reset every fixed reset period, we define CMA dead time as the time interval between a soft SEU occur in the ULPM2 and the next CMA reset (see Figure 8). Assuming an exponential distribution for the time between two soft errors, the induced CMA dead time will be:

$$T_D = T_R / \lambda \cdot (1 - e^{-\lambda T_R})$$

where:

T_D = dead time;

T_R = trigger reset period;

λ = soft SEU rate = $5.6 \cdot 10^{-8}$ s⁻¹.

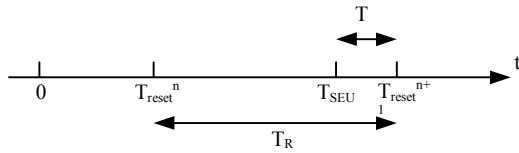


Figure 8: CMA dead time

We are so able to calculate the CMA dead time percentage as a function of the reset time. Figure 9 shows that dead time percentage values are acceptable for our purposes.

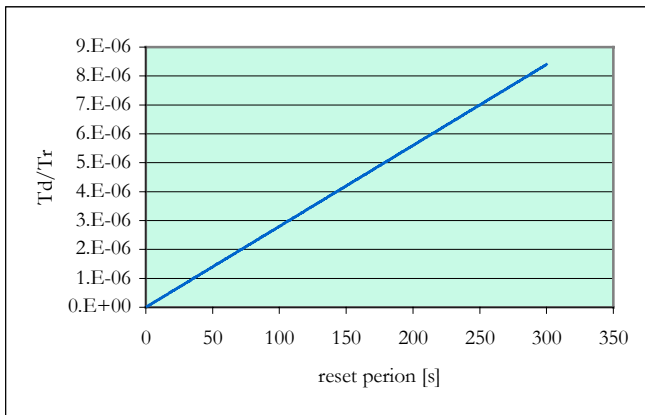


Figure 9: Dead time percentage vs. reset period

III. CONCLUSIONS

Fujitsu technology evaluation, using the ULPM2 clock multiplier has been successful.

Total Ionising Dose test, following the ATLAS standard test method, has shown that the 0.25 μm CMOS technology is radiation tolerant enough for our purposes. Power consumption increase, due to the total dose, is negligible for the foreseen radiation values in the RPC region.

Single Event Effect test has shown that this technology is not sensitive to destructive SEE, such as Single Event Latchup or Single Event Burnout. Only soft SEU were detected, coming from the ULPM2 DLL loss of lock. The dead time introduced in the CMA from this kind of errors is acceptable. Anyway, in order to keep low the CMA error rate, redundancy to SEU will be introduced in the CMA main control logic.

IV. REFERENCES

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