Low Noise Amplifier for Capacitive Detectors.

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Abstract

As a design study for the LHC experiments a 'Low Noise Amplifier Shaper' for capacitive detectors is developed. This amplifier is designed in 0.6 um CMOS technology from AMS.

The goal was to design an amplifier with a noise contribution of 250 electrons, and 12 electrons per pF contribution from the input capacitor and a relative high gain.

A test chip with two versions of the amplifier, a 'radiation tolerant' (gate-around FET's) and a 'rectangular' version has been fabricated and is now under test.

These designs, and there characteristics, simulated and measured, will be compared and discussed.

I. INTRODUCTION

A other goal of this project was to get more experience with the design- tools, methods and technologies in analogue IC design.

The pre-amplifier should have, besides the noise constraints, a relative high gain and low power consumption.

The amplifier should be able to withstand a certain radiation level. To study the influence of radiation, two versions of the amplifier are designed. The versions are a ‘rectangular’ and a ‘gate around’ (radiation tolerant) version. The basic difference in layout between these two versions is shown in figure 1.

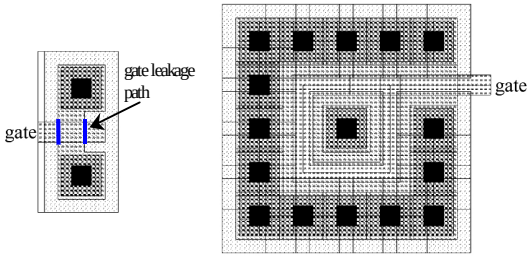

Figure 1: A ‘rectangular’ FET and a ‘gate-around’ FET

The left FET in figure 1 is the 'rectangular' version, the right FET the ‘gate-around’ version. Radiation damages especially the N-type FET. It causes a leakage current around the end of the gate. The gate of a ‘gate-around’ FET has no end, so no leakage current can occur. On the test chip 4 channels of each version are realized.

This document describes the behavior of the circuits when they are “biased for speed”. This means short time constants for the preamp and shaper, which results in undershoot at the shaper outputs.

II. THE PREAMPLIFIER

The amplifier is based on a single FET amplifier.

In this circuit the gate of the FET M0 is the input and the drain the output.

Optimising the circuit for noise makes the input FET wide. Optimising for bandwidth however subscribes a small FET, to reduce the Miller capacitance.

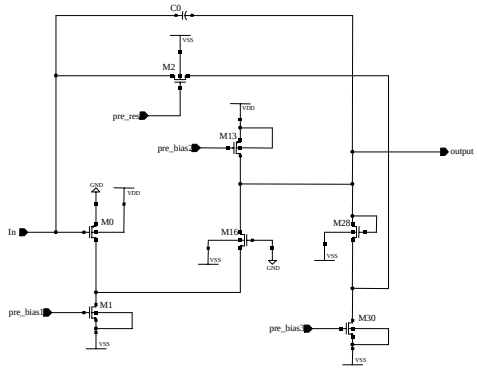

Figure 2: The schematic diagram of the rectangular version.

To optimise the circuit for gain and power a cascode circuit is used. In this circuit the amplifying steps are separated. In a single FET amplifier the conversions ‘input voltage to drain current’, and ‘drain current to output voltage’ are realized in just one FET. In a cascode schematic diagram both conversions have their own FET, which can be optimized for its purpose.

Optimising the circuit for noise requires a wide-channel input FET. A narrow channel is better to reduce the Miller capacitance (larger bandwidth).

A cascode circuit is the optimum for both requirements. A folded cascode is used to implement this configuration within the power supply limits.

A. ‘Rectangular’ amplifier

The amplifier is a charge amplifier, so the main feedback is a capacitor.

In figure 2 the schematic diagram of the pre-amplifier in the ‘rectangular version’ is drawn. The feedback resistor (FET M2) in parallel with the feedback capacitor is

required to control the DC operating point of the amplifier. The output level of the amplifier will stabilize without any precautions on about –1 Volt. This would give an asymmetrical dynamic range. To make this symmetrical, the output level should stabilize at 0 Volt. To realize this, one gate-source voltage is subtracted from the output of the amplifier.

The resistor is needed for DC and low frequency feedback. The resistance is adjustable by an external voltage (pre_res) to control the trailing edge of the amplifier signal. To operate the circuit, 3 DC bias currents must be applied:

1. input FET bias (pre_bias_1),
2. cascode FET bias (pre_bias_2),
3. subtraction network bias (pre_bias_3).

B. *'Gate around' amplifier*

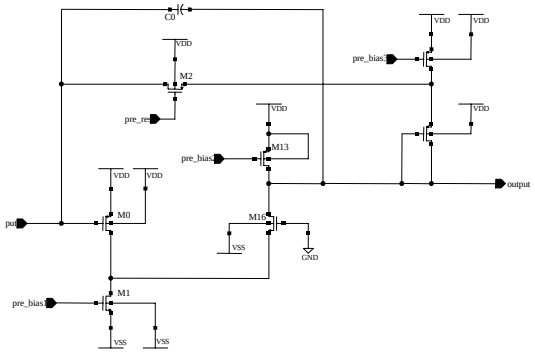

Figure 3: Schematic diagram of the gate around version.

The circuit is quite similar to the previous version. The major change is due to the fact that we cannot use a N-FET as a feedback (in ‘gate around’ it is not possible to make a FET longer then wide), so a P-FET is used instead.

The operating voltage on the gate of the feedback FET, when changed from the N-type to the P-type, is below –2 Volt, which is unacceptable. To get this voltage between the power supplies we have to change two things (see figure 2):

1. Connect the source of M0 to VDD (+2 Volt). This lifts the gate of FET M0 to +1 Volt.
2. The level subtraction at the output must become level adder. This makes the output again about 0 Volt.

III. THE SHAPER

This circuit has the same configuration as the circuit of the pre-amplifier. The differences between the circuits are the input capacitor and the dimensions of the used components.

A. *'Rectangular' shaper*

The shaper is an active band-pass filter. The components that control the bandwidth of this filter are the input capacitor, the feedback capacitor and the feedback resistor. The feedback capacitor and resistor determine the high roll off point, while the input capacitor and the feedback resistor control the low roll off point.

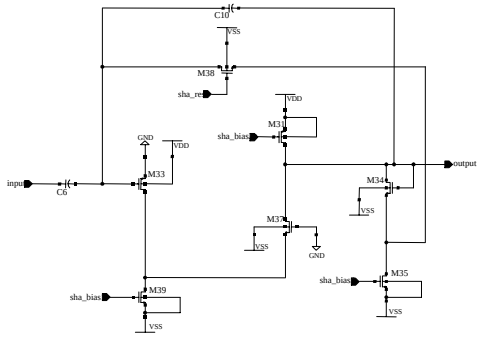

Figure 4: The schematic diagram of the shaper, ‘normal’ version.

B. *'Gate around' shaper.*

The differences between the ‘rectangular’ and the ‘gate around’ versions are similar as with the pre-amplifier versions.

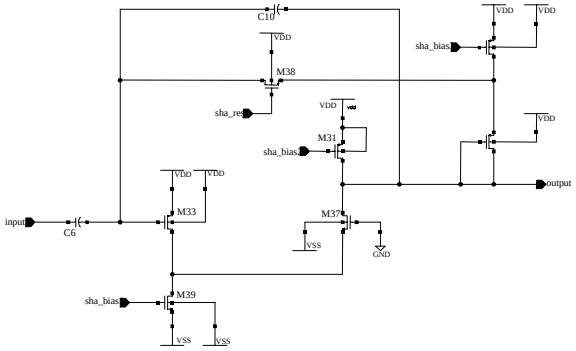

Figure 5: The schematic diagram of the shaper, 'Gate Around' version.

IV. THE OUTPUT BUFFER

The shaper signals are measured in the test set-up with an oscilloscope. The oscilloscope has high impedance inputs (1M•), with a capacitive load of 10 pF. Because the shaper output is does not have the capability to drive a capacitive load, the signals need to be buffered.

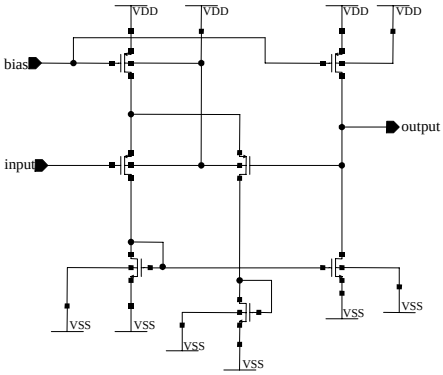

Figure 6: The schematic diagram of the output buffer.

The buffer circuit is equal for both versions. The circuit consists of a differential amplifier with a high current output stage. The differential amplifier is designed to create a buffer with a gain of 1.

V. THE CIRCUIT SIMULATIONS

The schematic diagrams above are the result of extensive list of simulations, in which we looked for the best combination of parameters.

During the simulations, and also later during the measurement, we used an input charge of 1 MIP, which corresponds to ~12000 electrons in 150µm silicon. The charge is injected via a capacitor of 1.5pF. The applied voltage step is:

$$U = \frac{Q}{C} = \frac{n_{el} \cdot Q_{el}}{C} = \frac{12000 \cdot 1{,}6021 \cdot 10^{-19}}{1p5} = 1{,}28mV$$

In figure 7 shows the simulated step response of the amplifier. The upper line is the response of the 'rectangular' version and the lower line of the 'gate around' version. A capacitor of 20pF was connected at the input to simulate the detector capacitance.

The gain of both versions differs due to the differences in the point of operation of the input FET (M0) in both versions. The source is connected to GND or to VDD.

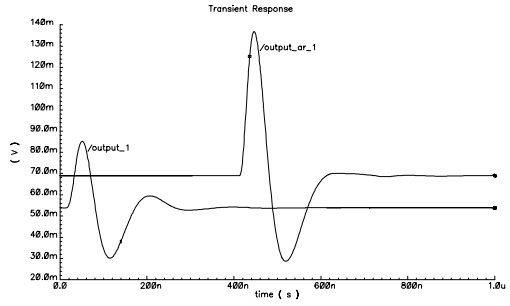

Figure 7: The step response of the circuits.

This simulation is done with a relatively fast settling time for the pre-amplifier. This results in a fast falling edge of the output pulse on the pre-amplifier and 60% overshoot after the shaper. In case the amplifier is biased for a time constant, much longer than of the shaper, no undershoot will occur.

The circuit is optimised for gain, speed and noise. For figure 7 a detector capacitance of 20pF was used.

Figure 8 and 9 show the dependency of the gain and S/N in relation with the input capacitance (detector) of the amplifier and shaper.

Also simulated is the dynamic range of the circuits. The result is plotted in figure 10 and 11, for an input range of –10 to +10 MIP.

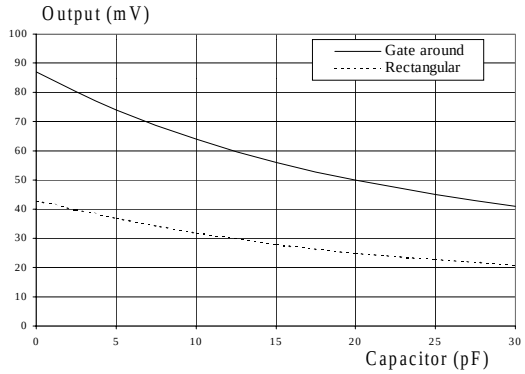

Figure 8: Gain plot, simulated

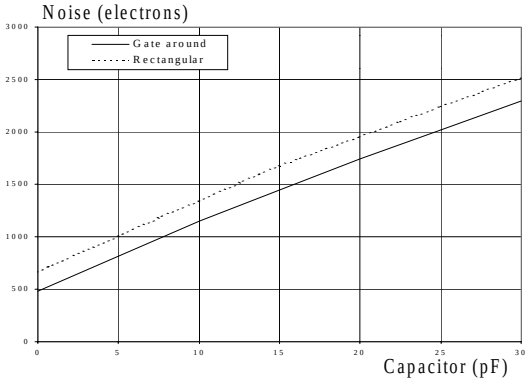

Figure 9: Noise plot, simulated.

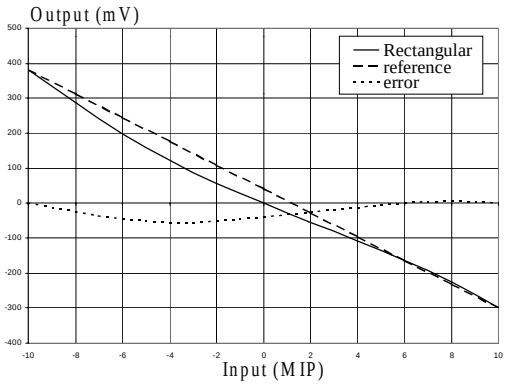

Figure 10: The dynamic range of the 'rectangular' version.

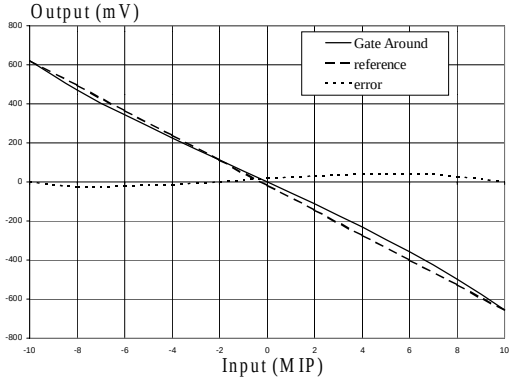

Figure 11: The dynamic range of the 'gate around' version.

All simulations are done with the bias settings from table 1. In the measurements the same bias settings are used, to allow a good comparison between both results.

Table 1: Settings used with the simulation

Circuit	Signal	net	rect	GA	
Pre-amplifier	Ibias input FET	Ipre_bias1	500	500	uA
	Ibias cascode FET	Ipre_bias2	-10	-50	uA
	Ibias level shifter	Ipre_bias2	1	-1	uA
	V feedback resistor	Vpre_res	500	-500	mV
Shaper	Ibias input FET	Isha_bias1	10	20	uA
	Ibias cascode FET	Isha_bias2	-2	-4	uA
	Ibias level shifter	Isha_bias3	500	-1	nA
	V feedback resistor	Vsha_res	500	-500	mV
	Vdd			+2	V
	Vss			-2	V

VI. MEASUREMENTS

Three measurements are made with the chip, gain, dynamic range and noise.

For the gain test the set-up in figure 12 is used. With a digital oscilloscope a large number of measurements are gathered and the mean of peak values gives the size of the output signal for 1 MIP.

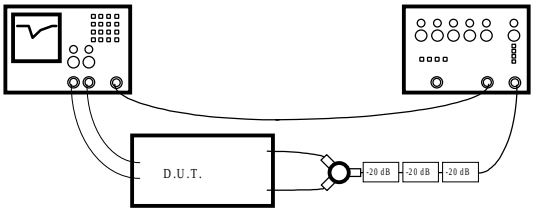

Figure 12: The test set-up.

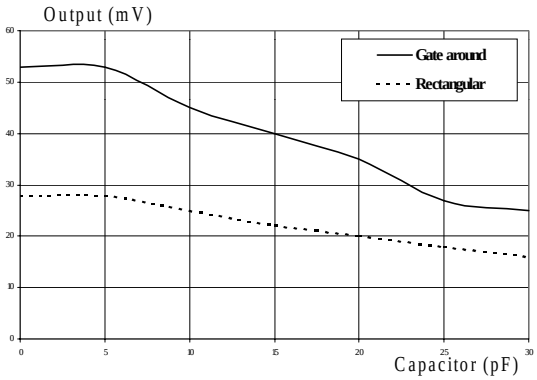

Figure 13: Gain plot, measured.

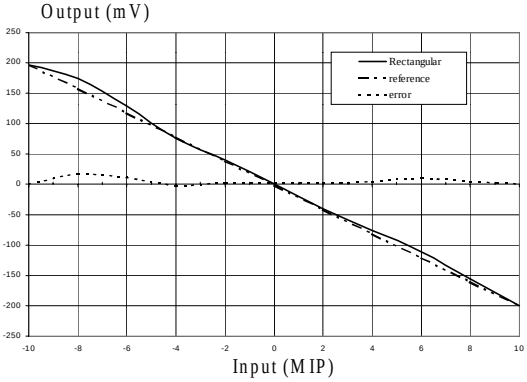

Figure 14: The measured dynamic range, 'rectangular' version.

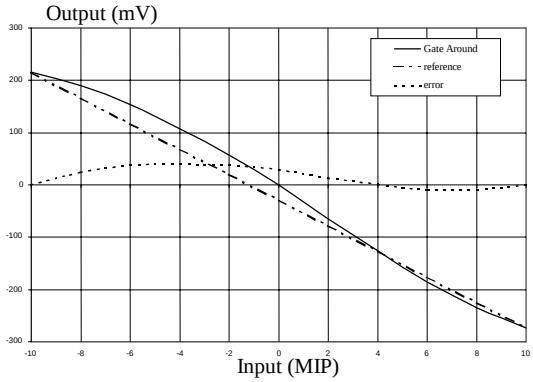

Figure 15: The measured dynamic range, 'gate around' version.

In the figures 15 and 16 the plots of the measured output signal is plotted over –10 to +10 MIP. Due to the low gain bias setting, the full dynamic output range is not reached.

For the noise test the input of the amplifier is left open, besides the detector capacitance. The oscilloscope calculates the RMS value of the AC signal at the output (Figure: 12). Similar to the simulations, the test is done with 7 values for the detector capacitance.

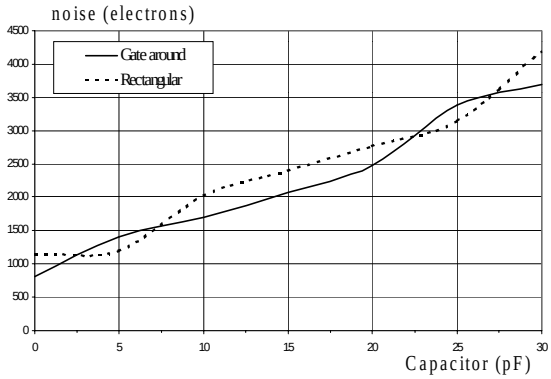

Figure 16: The noise plot, measured.

Table 2: Comparing simulation and tests.

	Measured	Simulation	Delta
	20	20	
	(pF)	(pF)	
Gate around:			
Output 1MIP [mV]	35	50	0.7
Noise [mV]	7.2	7.3	1.0
Noise [el]	2469	1741	1.4
S/N	4.9	6.9	1.4
Rectangular:			
Output 1MIP [mV]	20	28	0.7
Noise [mV]	4.6	4.6	1.0
Noise [el]	2760	1956	1.4
S/N	4.3	6.1	1.4

The measured bias currents and voltages show less then 8% deviation from the expected simulated values.

Other differences are:

Rectangular version:

- The actual gain is less than simulated.
- The value of the noise is the same, but due to lower gain is the S/N ratio lower than expected.
- The linearity is acceptable between +/- 4MIP. Outside that the deviation goes up to 10%.

Gate around version:

- The actual gain is less than simulated.
- The value of the noise is the same, but due to lower gain is the S/N ratio lower than expected.
- The non-linearity shows the same behaviour, but the deviation is worse.

1. CONCLUSIONS

Since the preamp shows a slower 1st slope, the shaper output is less then expected. This also results in a worse S/N ratio than expected.

The feedback FET's has been designed to short, this in combination with a small Cfb (~25fF) results in an instable operation point for the rectangular version for longer (>1us) time constants. These small components could be the cause of the differences between simulation and measurement.

In case the circuit is biased as presented (with short time constants) there is no instability but the S/N ratio is poor.

Measurements show a poor linearity, this also is a drawback of a short feedback transistor since the linear range is rather small.

VII. WORK TO BE DONE

For better understanding of the differences between simulation and measurements, more measurements will be done. Longer time constant of the preamplifier will be used to investigate the noise contributions. First measurements show a drastic increase in S/N at peaking times > 50ns, at a gain of more than 120mV/12000e.

In order to study the influence of radiation on both versions, a number of chips will be irradiated and compared with the not irradiated devices.

VIII. REFERENCES

1. A CMOS Mixed-Signal Readout Chip for the Micro strip Detectors of HERA-B. W. Fallot-Burghardt.
2. Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies. Zhong Yuan Chang, W. M. C. Sansen.