High-density low-mass hybrid and associated technologies

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Abstract

Industry is more and more using "build-up" Cu/Polyimide high-density hybrid circuits for civil commercial products which are small, thin, light-weight, and yet highly functional. High-energy physics can benefit from this technology in implementing frontend electronics in the area near the interaction point where the space is valuable and the material needs to be as transparent as possible. The build-up circuit and associated technologies are reviewed in this presentation with an example of application in the ATLAS SCT silicon microstrip tracking system.

I. INTRODUCTION

The terms "hybrid and associated technology" as used in the field of high energy physics are generally classified as "Packaging" technology in industry. Packaging technology includes (1) Assembling electronics parts mechanically and electronically on a wiring board, (2) Extracting the heat generated by active components, thus, solving the heat problem and (3) Protecting the packages from environment of daily usage. The latter (2) and (3) are not trivial issues. The solutions are, however, strongly associated with the design of the products, thus being critical to making the products successful in the market, e.g., as with mobile phones and laptop computers. Much development has occurred in the area of (1) which is rather generic and fundamental to technology, therefore often being classified as "packaging" in a narrow sense. This paper mostly reviews the area (1), with an example application in an LHC experiment.

II. PACKAGING TECHNOLOGY OVERVIEW

In order to get an overview of the packaging technology, three summary tables are given: History of electronics packaging (Table 1), High density packaging of IC/LSI's (Table 2), and Development of printed wiring board (Table 3) [1].

A. History of electronics packaging

In the history of electronics packaging, the building blocks of active devices, IC packages, electrical parts, printed wiring boards (PWB), and packaging methods are listed in the time sequence in Table 1. A clear trend in all areas is toward smaller packages and higher densities. In active devices, from the vacuum tubes in the 1950's, through transistors in the 1960's, integrated circuits (IC) in the 1970's, large scale IC's (LSI) in the 1980's and to very- and ultra-large scale IC's (VLSI, ULSI) in the 1990's and 2000's. In wiring boards, from metal chassis in the 1950's, single-side PWB's in the 1960's, double-sided PWB's in the 1970's, multi-layer PWB's in the 1980's, then emerging and maturing in the 1990's, the "Build-up PWB" technology.

The term wiring board is often associated with the word "printed", abbreviated as PWB, used to mean "duplicated". Photo-etching is one such duplicating method, and wiring boards made with this technology are also known as "printed" WB's.

B. High density packaging of IC/LSI's

The aim of IC/LSI packaging is to maximize the ratio of silicon area to the wiring board. Historically, IC's were first packaged in carriers which themselves had no internal circuitry, such as the DIP (Dual In-line Package) and SMT (Surface Mount Technology) packages. Soon, more functional forms followed with IC's or LSI's packaged in circuit carriers, COX/COB (Chip on X-substrate, or Chip on Board, where X means a type of PWB), or multiple IC's or LSI's in modular carriers, MCM (Multi Chip Module). MCM's have been used in main frame super-computers. Most recently, multiple IC's or LSI's have been processed on a wafer (silicon PWB), WSI (Wafer Scale Integration) technology. Advantages and disadvantages of different IC packaging are summarized in Table 2.

It is also possible to use COX/COB within MCM packages, so that there are three substrate categories of PWB in use: MCM-C, using ceramic thick-film PWB's; MCM-L using organic material PWB's (laminated); and MCM-D using thin-film deposited PWB's. All deal with bare IC's and associated technologies. When dealing with bare IC's, it is critical to use good working chips, so called KGD (Known Good Die), and to work in a clean room environment, at least class 10,000 or so.

An even higher density packaging is to integrate multiple LSI's on one wafer, WSI (Wafer-Scale Integration): either processed on a single wafer, WSI-Monolithic, the ideal of a "system on wafter", or individual LSI's mounted onto a silicon PWB, WSI-Hybrid. WSI-Hybrid provides more freedom than WSI-Monolithic but requires extra connection technologies. The cost of WSI packaging depends critically on the yield of the wafer.

Packaging efficiencies, the ratio of silicon to package areas, of different IC packages are summarized in Figure 1, together with the line/gap width of the technologies. The efficiencies are approximately: DIP ~ 6%, SMT 5~30%, COX/COB 20 ~ 70%, MCM 30 ~ 70%, WSI 50~100%, and 3D packaging > 100%. The character of the efficiency has two aspects: on the one hand, when the line width is large, e.g., 300 μm, for DIP and SMT packages, it is governed by the overall packaging, i.e., the "System" side; on the other hand, when the line width is 10 to 1.0 μm, it is governed by the LSI, i.e., "Device" side.

COX/COB by definition covers a wide range of line widths from 10 μm to 200 μm, overlapping the narrow MCM line widths of 10 ~ 80 μm and the thin-film of 50 ~ 100 μm, and also

Table 1: History of Electronics Packaging [1]

<table>
<tr><td></td><td>1950</td><td>1960</td><td>1970</td><td>1980</td><td>1990</td><td>2000</td></tr>
<tr><td rowspan="3">Active devices</td><td rowspan="3">Vacuum tubes</td><td rowspan="3">Transistors</td><td rowspan="3">IC</td><td rowspan="3">LSI</td><td rowspan="3">VLSI</td><td>ULSI</td></tr>
<tr><td>Stacked LSI</td></tr>
<tr><td>Ball IC</td></tr>
<tr><td>IC packages</td><td>Socket</td><td>TO</td><td>DIP/PGA</td><td>QFP/TSOP</td><td>BGA/CSP</td><td>CSP/LGA</td></tr>
<tr><td rowspan="2">Electrical parts</td><td rowspan="2">Long-lead parts</td><td rowspan="2">Axial-lead</td><td rowspan="2">Radial-lead</td><td colspan="2" rowspan="2">SMT, Chip parts</td><td>SMT, Chip</td></tr>
<tr><td>Embedded</td></tr>
<tr><td rowspan="2">Wiring board</td><td rowspan="2">Metal chassis</td><td rowspan="2">Single-side PWB</td><td rowspan="2">Double-side PWB</td><td>Multilayer PWB</td><td colspan="2">Build-up PWB</td></tr>
<tr><td colspan="3">Ceramics, Glass-ceramics multilayer WB</td></tr>
<tr><td rowspan="3">Packaging method</td><td rowspan="3">Wire, terminal, solder</td><td colspan="2" rowspan="3">Leads into through-holes, solder</td><td colspan="3">Attach SMT parts, solder, solder re-flow</td></tr>
<tr><td colspan="2" rowspan="2">ACF/ACP, simultaneous attach & connect</td><td>ACF/ACP</td></tr>
<tr><td>Direct Ball IC's</td></tr>
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the wide line widths, 100 ~ 300 μm of the thick-film ceramic hybrids or SMT PWB's. An exotic class with efficiency more than 100% is 3D packaging, e.g., stacking multiple LSI's.

C. Development of printed wiring board

Printed wiring board (PWB) technologies can be categorized into four types: Through-hole (TH) technology, Surface mount technology (SMT), Ceramic substrate technology, and Build-up technology. Critical breakthroughs in each PWB technologies are listed in Table 3.

Multi-layer TH-PWB matured in the 1960's and is still being used in industry for low-cost applications where space is not the primary concern. SMT-PWB is a development of TH-PWB which incorporates fine pitch traces optimized for SMT devices and has dominated PWB's after the 1970's.

There are two methods of TH-plating and patterning in TH- or SMT-PWB's: subtractive and additive. In the subtractive method, TH-plating is done without photo-resist masking on the top and bottom conductor planes, thus making the conductor thicker by the TH-plating thickness in addition to the base thickness, e.g., 20 μm TH-plating to 12 μm base thickness. Pattern masking includes the TH lands and etching is done afterward. In the additive method, photo-resist masking is done before TH-plating. After TH-plating, the photo-resist and the base metal are etched out. One type of the additive method removes the TH plating thickness on the traces when the base metal (of non-trace area) is etched out.

The ceramic substrate PWB's are as old as the TH/SMT-PWB's. After the development of "green sheet" and "thick-film pasting" technology, ceramic PWB's became established in applications such as thick-film hybrid IC packages.

Because of the demand for finer traces and higher density packaging, the latest PWB technology is the "build-up" PWB, first introduced by IBM as SLC (Surface Laminar Circuit) in 1985, and which from 1995 has matured into numerous variations. In Japan, companies producing build-up circuits (and their proprietary varieties) include Nippon CMK(SPM-P), Fujitsu (FDLL), Nippon AIC (ADDIVIA), Hitachi Kasei (HITA-VIA), Ibiden (IBSS), Matsushita (ALIVH), Meiko (M-VIA), NEC (DV multi), Oki (Via post) Sharp (Flexible), Toshiba (B2it), and Nippon Victor (VIL). The build-up technology is also known as "High Density Interconnection" in the US.

III. BUILD-UP PWB'S

The build-up technology is the latest and is dominating high density PWB's. In Japan, in 1998 it shared about15% of all the multilayer PWB's, and in 2000 it is expected to be about 30%. The major application is small, thin, light-weight, and yet highly functional commercial products, such as mobile phones, digital cameras etc.

One difference between TH-PWB's and build-up PWB's is in the interconnection between layers. An example of the two technologies is shown in Figure 2 applied in the Cu/Polyimide hybrid of ATLAS SCT barrel modules which uses both technologies. In the TH-PWB technology, the diameter of the TH is limited to the physical dimension of drills, i.e., 300 μm diameter, thus the land diameter is 500 μm. The TH's are penetrating all layers and the interconnection of a layer is inclusive to all layers, thus requiring larger total area for the interconnection and less freedom in trace patterns. In the build-up PWB technology, insulator/conductor layers are laminated one-by-one while making "micro-vias" between layers, layer-by-layer. The diameter of the via is 150 ~ 50 μm, and the diameter of the land is 300 ~ 100 μm. The area required for the interconnection of layers is greatly reduced not only because of the size of the land but also because of the non-inclusive nature of the via, thus leading to higher density and more freedom in patterning traces.

Table 2: IC packages [1]

	Packaging on PWB	Advantages	Disadvantages
DIP	leads: attach, insert TH	Easy pre-check	Single-side PWB Space inefficient
SMT	SMT package attach	Dense packing on double-side	
COX/COB	bare ICs on "X" substrate	High density	Multilayer PWB, CTE mismatch, Clean-room work, Known good die (KGD)
MCM -C, -L, -D	Multi LSI's on a substrate Ceramic, PWB, Thin-film deposition	High density, Modular	same as COX, No substrate for fine pitch yet
WSI	Multi LSI's on one wafer	Ultimate high density, short connection, smaller fab. step	Cost depends on wafer yield
-Monolithic	Multi LSI processing on one wafer	System on wafer	
-Hybrid	Separate LSI's on one wafer	Same CTE, separate LSI processes, LSI locations in cooling	

A. Micro-via formation

The key technology of the build-up PWB is the formation of the micro-via. There are a number of technologies, including photo via, drilled via, laser via, laser via with conformal masking, and plasma via. These technologies are summarized in Table 4, associated with product names. A commonly used technology today is the laser via with conformal masking. The micro-via is formed in three steps in the resin coated Cu foil laminated to the completed layer underneath: etching out the via hole in the metal, drilling resin with a laser using the metal hole as a mask, and then plating. Use of etching technology allows much smaller via diameters, 50 ~ 150 μm, than mechanical drilling, 300 μm.

IV. Ceramic PWB's

Although ceramic PWB technology is more massive than organic PWB technologies with epoxy and polyimide, the technology is briefly reviewed for comparison. Multilayer ceramic PWB's have been developed using thick-film and thin-film methods.

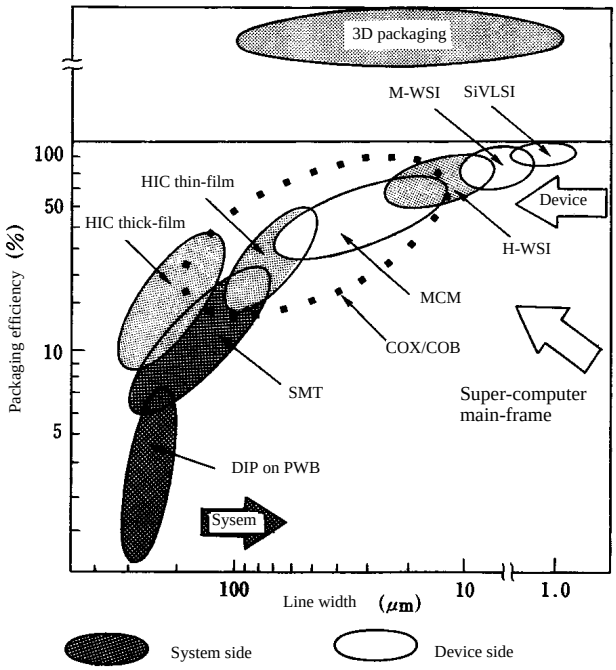


Figure 1 Packaging efficiency of various technologies as a function of line width [2] (referenced in [1])

A. Thick-film method

This is the technology commonly used in the ceramic PWB, introduced in 1960, together with the "green sheet" technology in 1959. In the method, conductor patterns are screen-printed with a thick-film paste, possibly together with resistors, and then fired at 1000 °C or so. This is possible because of the high heat tolerance of ceramics.

The thick-film paste is made of 1 to 5 μm diameter "metal powders" mixed with a few wt% of "flit" and a binder material. When fired, the metal powders melt to form a conductor, e.g., 8 μm Au thickness, which is controlled by the printing thickness of the thick-film paste. Metal powders of Ag, Au, and Cu are commonly used. In the case of Ag, because of the migration problem, a small amount of Pd or Pt is added forming Ag/Pd or Ag/Pt.

The "flit" is used to interface the ceramic and conductor for mechanical or chemical bonding. Glass flit is used for a glass interface for mechanical bonding, and copper oxide and bismuth oxide flit for chemical bonding.

A flow diagram of one method, Thick-film Tape Casting Method, is shown in Figure 3. Although the screen-printing method is cost-effective, the line width and gap are limited in this technology.

Table 3: Development of printed wiring board [1]

	TH-PWB	SMT-PWB	Ceramic substrate	Build-up PWB
1938			Tele-funken-Siemens: Alumina metalliza-tion	
1953	Motorola: double-side plat-ing TH			
1959			RCA: Ceramic “green sheet”	
1960			IBM: Alu-mina multi-layer board Thick-film past-ing	
1961	Hazel-tine: Mul-tiplaner plating TH			
1968	Polyim-ide PWB			
1970~	Prepreg,...	TH-plat-ing meth-ods (Subtrac-tive, Addi-tive)	Thick-film hybrid IC	
1985				IBM: SLC (surface laminar circuit)
1996~				Build-up PWB’s in Japan

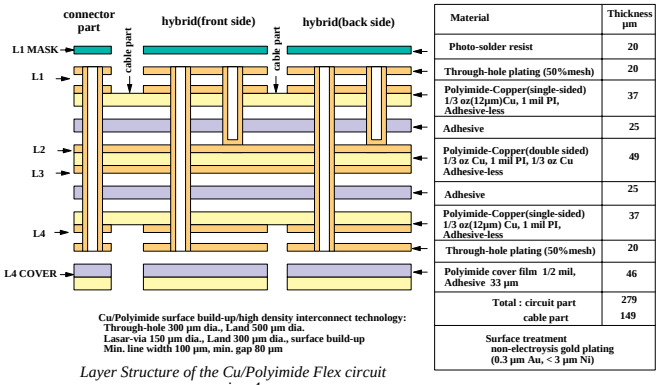
B. Thin-film method

One way of overcoming the line width limitation of thick-film screen-printing is to deposit metals with a vacuum evapo-ration or a sputtering method, where a thin film of 10 to 200 nm can be deposited. Fine patterns with line width much less than 100 µm and a via diameter of 50 µm with laser drilling are achievable. Deposited thin-film, such as with the IVa family - Ti, Zr - and VIa family - Cr, Mo, W - is not the actual conductor but forms an interface between ceramic and conductor. A thick-er conductor of Cu, Au, or Ag of 5 to 20 µm is plated additively afterward. Since the thin-film technology does not involve high temperature, the technology is not limited to ceramic PWB’s and is finding application in other organic material PWB’s.

V. Low Mass

A. Battle of Weight

In industry, “low mass” means “small and light-weight”. A typical example of weight competition has been seen in mobile phones as shown in Figure 4. This competition can be remem-bered as the battle of the “gram”. The weight of mobile phones was about 200 g in 1995. The weight reduction rate was sudden-ly changed in 1995 by the introduction of Matsushita’s (ALIVH) build-up PWB, reducing the size of mobile phones, together with other reductions such as the battery casing with aluminium. In 1996-97, the weight was about 100 g, and in 1999-2000, the weight will be in the range of 50 g. The least heavy model of the day has been the winner in market share.



Layer Structure of the Cu/Polyimide Flex circuit version-4

Figure 2 Layer structure and interconnection between layers in the hybrid of the ATLAS SCT barrel modules

Table 4: Micro-via formation technology [1]

	Process	Products
Photo via	Photo imagiable insulating material and Photo-lithog-raphy	IBM (SLC)
Laser via	Thermosetting resin and laser-drilling	
Drilled via	Drill via in resin coated copper and laminate on core substrate	Hitachi-Kasei (HITAVIA)
Laser via with confor-mal mask-ing	Etch out the via hole in copper, laser-drill via in resin by using the etched-out copper as mask	Most common
Plasma via	Etch out the via hole in copper, plasma-drill via in resin by using the etched-out copper as mask	Dyconex (DYCOstrate)

B. ATLAS SCT barrel module

An example of an application of build-up technology is the

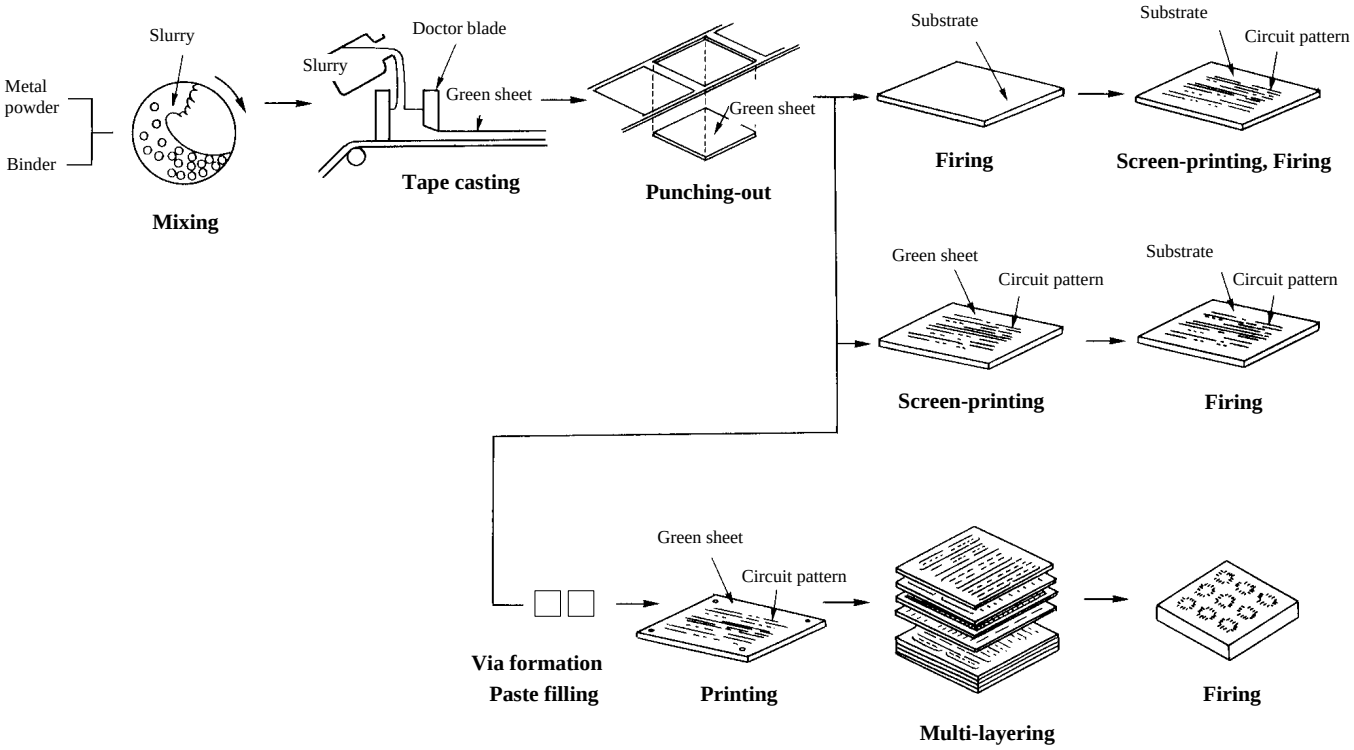


Figure 3 Thick-film tape casting method [1]

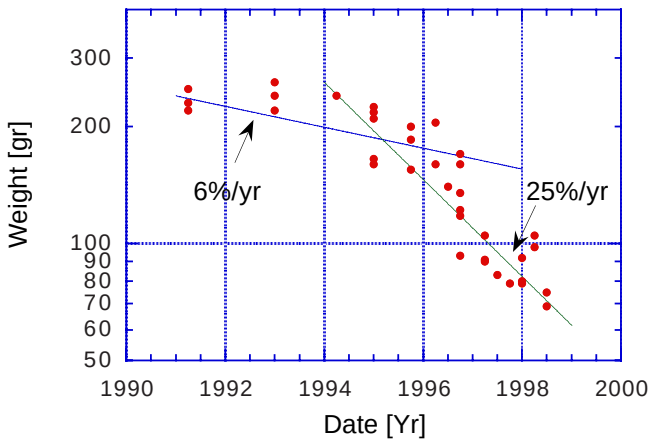


Figure 4 Reduction of weight of mobile phones [3]

hybrids of the ATLAS SCT (Semiconductor Tracker) modules [4]. The hybrid carrying the frontend electronic ASICs is integrated with silicon microstrip sensors to form a modular detector unit, as depicted in the case of a module for the barrel section in Figure 5.

The large, wide silver-coloured area is the silicon microstrip sensors. The hybrid, made from build-up PWB of Cu conductor and polyimide insulator, is placed near the centre of the module and carries 6 ASIC's on the front side. The module is double-sided and the hybrid extends to the backside with 6 more chips, wrapping around the module. An advantage of the Cu and polyimide technology is that the cable and electronics sections are fabricated in one piece, thus improving the electrical performance and the reliability of the mechanical and electrical connections.

1) Hybrids in the ATLAS SCT

In ATLAS SCT modules, the packaging efficiency requirement is modest in the hybrid, being determined by the size of silicon microstrip sensors which is wider than the sum of the ASIC's. The tightest requirement is at the backend of the chips where the minimum pad pitch is 180 µm. Thus, the minimum line width and gap is each 90 µm on the PWB. These lines are to be connected to the bus lines running along the hybrid. The bus line pitch is determined by the land diameter of the via's which connect the lines from the chips traversing across the bus lines. With the build-up technology, a land diameter of 300 µm with a via diameter of 150 µm is modest, matching the bus line pitch of 300 µm which then determines the line width and gap of 150 µm.

The layer structure of the hybrid is shown in Figure 2. The ground and power planes are the third and fourth layers, respectively. Fully penetrating TH technology is used to bring the

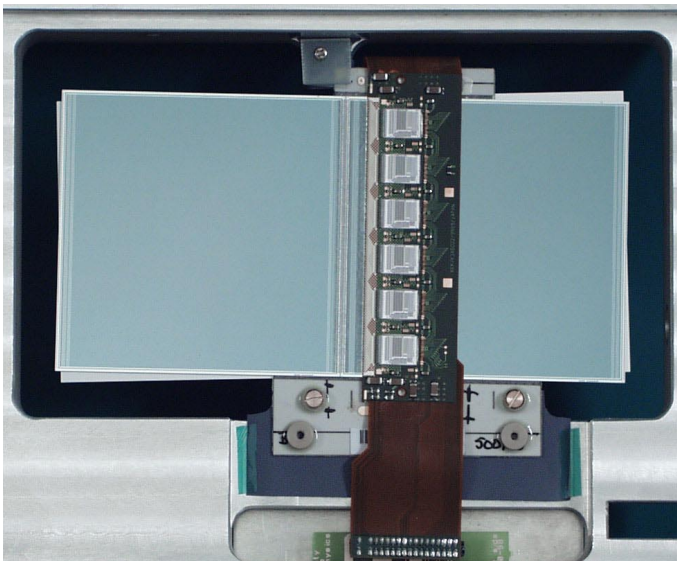


Figure 5 An example application: ATLAS SCT barrel module

power connections to the surface layer, and to bring the ground to the surface and bottom layers. Since the Cu and polyimide PWB is flexible, a carbon material (substrate) reinforces the electronics sections mechanically, thermally and electrically, the ground being reinforced by connection to the conductive carbon material.

A critical aspect of the packaging technology used for the SCT modules is a solution to the cooling problem presented by the high power consumption of the ASIC's, about 5 W for the 12 chips in the module, and by the possible thermal runaway of the silicon microstrip sensor leakage current because of radiation damage in LHC. A highly thermally conductive material is required both for the baseboard to which the sensors and the hybrid are glued, and for the hybrid substrate itself.

Table 5: Summary of the ATLAS SCT barrel hybrid

LSI	ABCD, 12 chips, BiCMOS, Amp-shaper-discri + FIFO buffers
Power consumption	5 W nominal, 7 W maximum
PWB	Build-up Cu/Polyimide PWB
Substrate	Carbon-carbon Uni-directional fibre material, 700 W/m/K (x), 35 W/m/K (yz)
Cables	Integrated, one-piece construction, better reliability

C. Radiation length comparison

"Low mass" in High Energy Physics means low radiation length. Properties of candidate materials are listed in Table 6: radiation length (Xo), thermal conductivity, and electrical resistivity.

For the hybrid substrate, for which the primary concerns are radiation length and thermal conductivity, a carbon material is superior to others, e.g., the so-called "carbon-carbon" with fibres running in one direction. The carbon is electrically conductive and can reinforce the electrical conductivity of the hybrid circuitry. It is often necessary to coat the surface of the carbon material in order to prevent carbon dust coming off. A material used for such coating is Parylene which can be grown uniformly on the surface in a fashion similar to chemical vapour deposition (CVD). Beryllia (BeO) comes second with respect to radiation length and thermal conductivity, however, toxicity may restrict its use.

For the insulator of the multi-layer structure, organic materials such as polyimide are available, as well as ceramics and glass. Organic material is far superior with respect to the radiation length.

For the conductor, there are four candidates: Cu, Au, Al, and Ag. From the radiation length aspect, Al is the leading choice. However, the industry's choice is Cu because of advantages in processing such as plating and etching, in electrical resistivity, in cost, etc. which override the low mass concern.

Table 6: Properties of candidate materials for low mass hybrid

	Xo [cm]	Thermal conductivity [W/m/K]	Resistivity [μΩcm]
Substrate			
Carbon-carbon/UD	19	700(x), 35(yz)	250
Beryllia (BeO)	14.4	280	
AlumiNitride (AlN)	8.38	165	
Alumina ceramics(Al2O3)	7.55	26	
Insulator			
Polyimide	28.6	0.12	
Pb glass	8		
Conductor			
Copper (Cu)	1.43		1.67
Gold (Au)	0.335		2.22
Aluminium (Al)	8.9		2.65

VI. Die Attaching

Bare semiconductor dice are glued to substrates using or-

ganic based adhesives. There are basically three different types used in the microelectronics industry: epoxies, cyanate esters and polyimides. Epoxies are widely used for low temperature applications (<175 °C), and cyanate esters and polyimide for high temperature (300 °C, >400 °C respectively). Epoxies are characterized by relatively low cure temperatures (room temperature to 175 °C) and moderate T(g)'s (Glass transition temperature, 50-155 °C typical). Epoxy provides a strong adhesive bond and can be easily reworked. Epoxies are relatively low cost and there is a large supplier base with many different products from which to choose.

Epoxy meets the requirements established by the military and NASA for high reliability applications. Strict controls have been established to limit the amount of permissible ionic contamination. Other controls have been put in place to assure the user community that the epoxy would have the same basic material properties from lot to lot. Table 7 summaries the supplier requirements of Test Method 5011 [5]. The carrier material is typically an epoxy resin. The carrier provides the adhesion and mechanical strength in the bond line. The carrier is filled with metal particles, such as Ag, Au, and Cu, in the event electrical and thermal conductivity is required (Type 1) or non metallic particles, such as silica and alumina, if the final bond must act as an insulator (Type 2). To enhance thermal performance aluminium nitride and diamond particles can be added.

Stress on the die is a critical parameter that affects the reliability of MCM/COX/COB's. Fortunately, most epoxies, if properly attached, can relieve and dissipate some of the stress built up due to CTE mismatch between the die and the substrate.

A. Ionic Contamination

It is known that hydrolyzable ions such as chlorine, fluorine, sodium and NH4 in the presence of moisture can lead to corrosion of aluminium metal on an IC and can be the source of electrical problems within a device. Test Method 5011 limits the amount of ionic contaminants and overall PH (ref. Table 7). Only trace amounts of the ionic contaminant is needed to start a corrosion process as shown in Figure 6. The ion is not consumed and is available to continue the corrosion process.

$$4Al + 3O_2 \rightarrow 2Al_2O_3$$

$$Al_2O_3 + 3HOH \rightarrow 2Al(OH)_3$$

$$Al(OH)_3 + Cl^- \rightarrow Al(OH)_2Cl + OH^-$$

$$Al + 4Cl^- \rightarrow AlCl_4^- + 3e^-$$

$$AlCl_4^- + 3H_2O \rightarrow Al(OH)_3 + 3H^- + 4Cl^-$$

Figure 6 The corrosion mechanism for aluminium [1]

B. Application methods

Automatic syringe-dispensing, screen printing, and stamping paste adhesives are the popular production methods for attaching ICs and other components. In application, control of the epoxy flow is an important consideration. Excessive flow-out will contaminate adjacent bonding sites and require additional cleaning steps. Uniform bond line thickness is important. Wire bond yields may also be affected if the large dice are not sufficiently level.

Table 7: MIL-STD-883 TM 5011 Supplier Requirements

Test Method 5011	Requirement
Materials	Uniform Consistency: free of lumps and foreign material, report filler type
Viscosity	Report
Pot Life	Minimum 1 hour
Shelf Life	12 months @ 25 C for a two component system 12 months @-40 C for a one component system
Infrared Spectrum	Supply
Adhesive Cure	Report, identical for all tests
Thermal Stability	less 1% weight loss at 300 C
Filler Content	+/- 2% of certified lot
Ionic Impurities: Total el conductance Hydrogen Chloride Sodium Potassium Fluoride	 less 4.50 mS/meter 4.0 < pH < 9.0 less 200 PPM less 50 PPM less 50 PPM less 50 PPM
Bond Strength	greater than 2.5Kg at room temp
Coef of Linear Thermal Expansion	65.0 micron/meter C below Tg
Thermal Conductivity	Type 1 greater than 1.5 W/meter K Type 2 greater than 0.2 W/meter K
Volume Resistivity	spec
Dielectric Constant	less 6.0 @ 1kHz and 1MHz
Dissipation Factor	less 0.03 @ 1 kHz less 0.05 @ 1 MHz

C. Cure

The cure schedule (i.e. oven time and temperature) determines the final properties of the adhesive. The optimum cure is determined by the user. Once an epoxy is fully cured it is advisable not to exceed the cure temperature for extended periods of time because the epoxy will begin to break down and lose strength.

D. Reworkability

An important consideration in MCM/COX/COB manufacturing is the ability to rework a chip if it fails during acceptance testing. Chips typically have to be removed and replaced because of defective die, ESD zaps, wire bonding problems etc. The epoxy selected has to have a glass transition temperature T(g) which will allow rework at temperatures that will not damage adjacent chips or the PWB structure. The glass transition temperature is the softening temperature of the epoxy, below which the thermal expansion coefficient is low and nearly constant, and above which is very high. For most die attach epoxies these values range from 50 to 150 °C. In a typical rework operation the chip is locally heated up to 200 °C. How much heat is required is dependent on the T(g) and thermal mass.

VII. Chip Interconnection

In industry, more than 95% of semiconductor chips are wire-bonded ultrasonically. Gold-ball thermosonic bonding forms the majority of interconnections in microelectronics today. The most advanced alternative to wire-bonding is the flip-chip process (called C4 - Controlled Collapse Chip Connection - or FC), first invented in mid the 1960s at IBM.

Comparing the two technologies, wire bonding is the most flexible. The minimum bond pad pitches are ~70 µm in Gold-ball bonds and as low as ~40 µm in Aluminium-wedge bonds. On the other hand, FC has advantages in handling high current, in low inductance and in low cross-talk capability. One expert opinion is that if the entire industry were to move toward FC, planning should be made to change in an ordinary fashion, not ahead of the wave, but along with the majority, so that mature chips and equipment, as well as experienced personnel would be available for a reasonable price.

Multi chip module rework is a costly and time consuming process which can often create additional damage due to increased handling. Therefore, high first pass yield at wire bonding is essential from a cost and schedule standpoint. In order to achieve very high yields of <100 ppm, there are numerous design and manufacturing considerations: e.g., chip bonding pads, bonding pads on polymer substrate, and wire bonding technology.

A. Wire bonding technology

Three wire bonding technologies are widely used in industry: Ultrasonic aluminium wire wedge bonding (US), Thermosonic gold ball bonding (TS), and Thermocompression gold ball bonding (TC). Advantages and disadvantages of the technologies are:

US -- Advantages: Least susceptible to contamination (example in Figure 7), Al bonds at room temperature, Finest pitch (<60 µm e.g.), Highest yield (<20 ppm e.g.). Disadvantages: Slower bonding, X-Y wire-pad orientation required (slows bonding), Three-parameter machine setup.

TS -- Advantages: all directions, fast, reliable Au-Au bonds, medium interface temperature. Disadvantage: susceptible to contamination, large pads, four-parameter machine setup, forms plague with Al chip pads.

TC -- Advantages: all directions, fast, reliable Au-Au bonds. Disadvantages: high interface temperature (>300 °C), very susceptible to contamination, large pads, forms plague with Al chip pads.

In the US process, stitch bonds are formed at both ends of the interconnect by a combination of pressure and ultrasonic energy (60~120kHz at the tool). As the wire softens freshly exposed metal in the wire comes in contact with the freshly exposed metal on the pad and a metallurgical bond is formed. Aluminium wire is typically doped with 1% silicon to more closely match the hardness of the wire with the bond pad material.

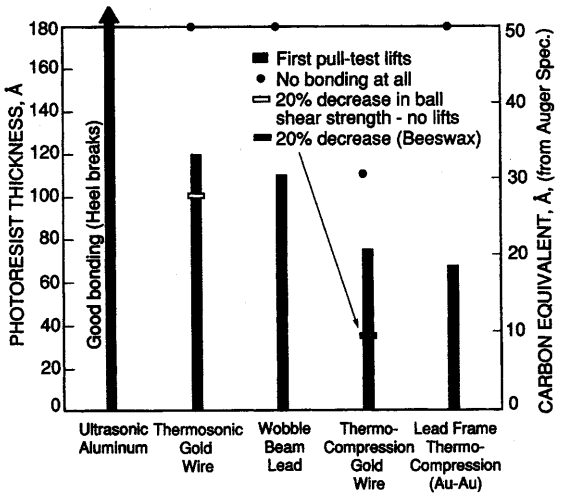


Figure 7 Sensitivity of various bonding methods to organic surface contamination [7]

B. Chip bonding pads

The first requirement for high-yield bonding is that the metallizatin on both the chip and the package be bondable. Unfortunately, the characteristics of chip metallization are often determined by other considerations. One solution being practised is capping (or coating) the doped bond pad metallization with ~0.3 µm of aluminium. Capping would allow for freedom in metallization design and processing and still result in the highest wire bond yield. The additional metal thickness also reduces the possibility of cratering, again increasing the yield.

The pad surface must be clean. Several significant contaminants may be left by the wafer-processing steps: sulphur, fluorine, fluoropolymers, glass, and carbonaceous materials. The wafer manufacturer should plasma clean the wafers in oxygen (or oxygen-argon) before shipment or storage.

C. Bonding pads on polymer substrate

Soft substrates often require a hard metal layer underneath

the wire bondable layer to obtain sufficient yields. A generic multi-layer structure of the bonding pads on polymer substrate is shown in Figure 8. Hard under layers such as Ti, Cr or nickel platings can be used to stiffen the bond pads and prevent "cupping" or "pad deformation".

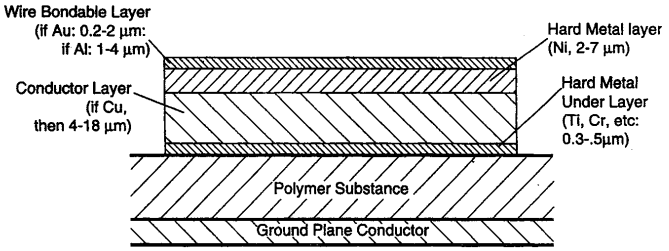


Figure 8 Structure of a generic, stiffened-metal bond pad and polymer substrate for wire bonding to MCMs [7]

D. Shelf-life aging of bonding wires

Aging properties of various 25-μm diameter bonding wires stored on 5-cm spools at 23 °C for two years were tested periodically [6]. In general, the breaking load of hard, as-drawn wire decreased rapidly (from 5 to15%) within six weeks after manufacture (thus, hard-wire is seldom recommended for volume production). All stress-relieved and annealed wires remained within their breaking-load specification for the entire two-year test period. The wire must be stored at approximately constant room temperature, and avoid exposure to direct sunlight, drafts from an open door, or possible heat sources.

E. Wire-bond pull test

Wire-bond quality is evaluated by visual inspection. Signs of cracked heels, tearing at the wedge, misplaced wires, inconsistent wire placement, excessive neck down etc. are indications that the wire bonding process is not properly controlled. Sample wire bond pulls are routinely used to verify supplied parts, production set-ups, check out new wire lots, or when the bonding process is changed. Averages and ranges are typically charted on traditional SPC (Statistical Process Control) Xbar -R, together with failure modes, for example, wire breaks, lifts etc. for statistical process monitoring.

In the destructive pull test, a small hook is placed in the centre of the wire span between the substrate and the lead frame and pulled up in a direction normal to the bonding plane as shown in Figure 9. If both bonds are on the same level (H=0), then the familiar equation is

$$f_{wt}=f_{wd}=F/(2\sin\theta) \quad (1)$$

with $2\sin\theta=1$ for $\theta=30°$. The f_{wt} or f_{wd} is typically about 60 to 75% of the manufacturer specified breaking load (due to heel deformation and metallurgical overworking). The hook being closer to one bond or the other results in a lower pull force.

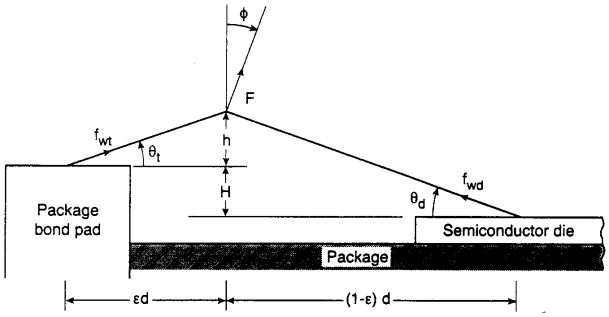


Figure 9 Wire bond pull test Set up [7]

F. Common failure modes and past problems

Over the past thirty years or so many wire bonding failure mechanisms have been identified and changes made to the design, process and materials used in wire bonding to eliminate or minimize the problem.

2) Purple plague

The purple plague and associated Kirkendall voiding are well known to occur at the bond pad in the gold (Au)/aluminum (Al) system. Purple plague is an Au-Al intermetallic compound which is brittle and made at high temperatures such as 600 °C as shown in Figure 10. Below 175°C, intermetallic growth in the gold-aluminium system is not primarily dependent on steady-state temperature but rather on the defect density. The failures are usually caused by the Kirkendall voids where the higher diffusivity of gold leads to voiding on the gold side of the interface. Au-Al related failures are more properly referred to as impurity-driven or corrosion reactions.

In well bonded systems, an intermetallic-related decrease in bond strength is not observed in use at temperatures less than 125°C. Thinner metallization also limits Kirkendall voiding by restricting the availability of gold. Al wire bonds on 0.25 μm plated Au films have been shown to be reliable.

3) Cratering

Cratering is a general term used to describe mechanical damage to the bond pad or underlying material. The damage may be a minor defect that surfaces during electrical testing or a gross divot of semiconductor material which appears on the underside of a wire bond after bond pull or shear testing. Wire hardness, bond pad thickness, bonder set up parameters, in particular high ultrasonic energies, have all been identified as causes or contributing to the cratering problem. Serious "overbonding" conditions which result in cratering can be identified visually or by SEM inspection. A wire bonding material system that is prone to cratering should be optimized via DOE (design of experiment) techniques and made robust to the conditions that lead to cratering.

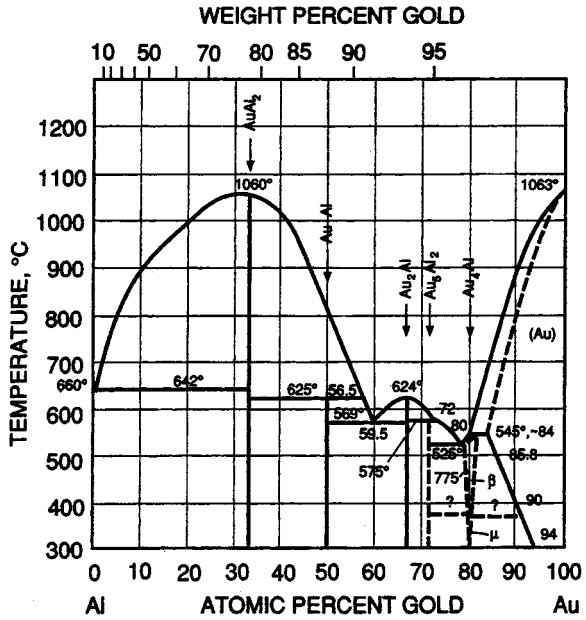


Figure 10 Aluminium-gold phase diagram (after Hansen) with the five Au-AI intermetallic compounds indicated [7]

4) Cracked heel

A common problem in aluminium ultrasonic wedge bonding is cracks which will sometimes appear at the heel of the wedge, an example being shown in Figure 11. These type of cracks are frequently caused by the motion of the bond head after the wedge bond is formed. The tool may rise too high or come off at an angle that overworks the wire and causes a crack to form. Larger cracks can pose a reliability problem especially if the wire is coated with a polymeric material and later temperature cycled.

5) Contamination

Contamination by plating impurities or thin layers of organic contamination on the bonded surface have both been the cause for reduced bondability (low yields), as well as causing premature failure during subsequent thermal stressing and downstream reliability problems. Gross contamination can sometimes be seen visually or with the help of a 15X microscope. For example, epoxy bleed out, residual stains from solvent cleaning or badly oxidized surfaces can generally be seen this way. In the event much higher magnifications are needed, other techniques are available. Scanning electron microscopy (SEM) and associated EDX (energy dispersive x-ray analysis) or Auger microscopy are two such techniques.

Carbonacesous contaminants, which cause the majority of bondability problems, can be cleaned with Oxygen, Ar, and other plasma cleaning, as well as UV-ozone cleaning methods. It is important to minimise contamination of bonding surfaces rather than to rely on cleaning afterwards. Protection of the bonding surfaces can be made with proper masking.

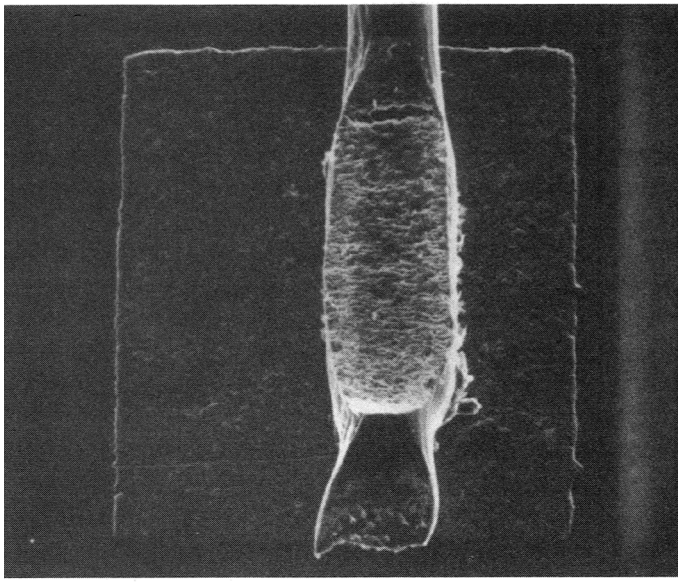


Figure 11 A wedge bond which shows a small crack at the heel [7]

VIII. SUMMARY

High density, low mass hybrid and associated technologies have been reviewed from the viewpoint of packaging technology in industry. Demands for small, light-weight, thin, and highly functional devices are driving industry to develop cost-competitive packaging components and technologies. In the area of printed wiring boards, the build-up PWB is growing rapidly in popularity. ATLAS SCT has benefited from the build-up flexible PWB with a compact one-piece-construction hybrid with low radiation length materials.

Wire bonding is the most cost effective technology for chip interconnection, yet. Ultrasonic Al wire wedge bonding has higher bondability on contaminated surfaces and higher reliability against Kirkendall voids. There are numerous design and manufacturing issues which must be addressed in order to achieve high wire bonding yields at the level of <100 ppm.

Packaging optimization is a non-trivial task which requires much work: understanding of the device and the system aspects, fundamentals and practicalities, etc. The effort is well worth it to produce good, reliable products and to extract the best performance of the device and the system.

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