ATLAS Electronics System Overview

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Abstract

A short overview of the ATLAS readout and level-1 trigger electronics is presented, as well as a few system issues that ATLAS is willing to address in a coordinated way.

ATLAS readout system overview

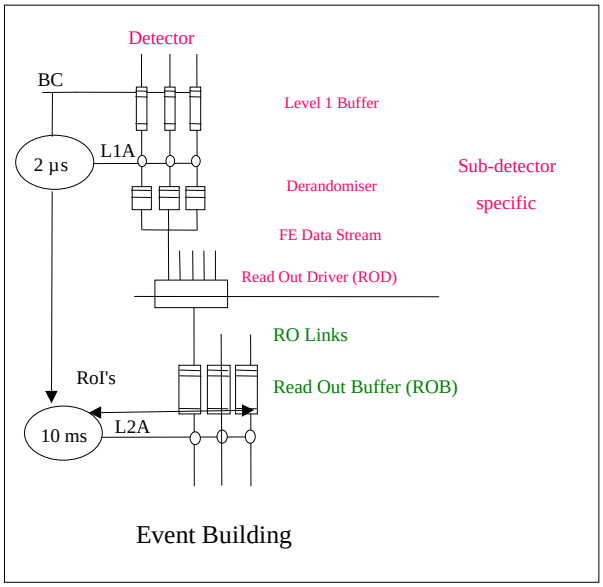

Figure 1. System Overview

Figure 1 shows a very schematic view of the ATLAS readout and triggering system.
Each sub-detector front-end electronics system contains a level-1 buffer or level-1 pipeline, either analogue or digital, in which information is stored at every bunch crossing and maintained during the level-1 trigger latency which is 2 µs. When a level-1 accept signal (L1A) occurs, data is transferred in a so-called derandomiser and sent to the first back-end electronics module, the Readout Driver (ROD) through front-end links. The derandomiser buffer must be able to contain several events in order to accommodate the maximum instantaneous L1A rate without introducing dead time. The ROD gathers several front-end links, processes the data, format them and send them through Gigabit links to the Readout Buffer (ROB) which is the data source for the level-2 trigger system, the event filter and the data acquisition.

The trigger has three levels:

1. The level-1 [1], based on fast hardware processing of coarse data. After 2 µs of latency the 40 MHz input rate is reduced to 75 kHz.
2. The level-2, based on high level processors. It processes part of the data on the basis of geographical region of interest (ROI of 0.1 x 0.1 $\eta\varphi$) provided by the level-1 system. After a few ms of latency, it reduces the event rate to a few kHz.
3. The event filter, based also on high level processors, processes the full event. After about one second of latency the event rate is of the order of 100 Hz.

The level-1 trigger system

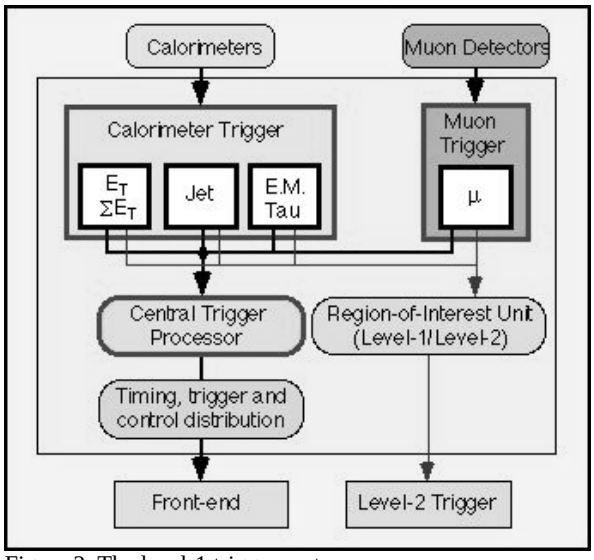

Figure 2. The level-1 trigger system.

This system is based on four main components (figure 2): the calorimeter trigger system, the muon trigger system, the central trigger processor (CTP) and the timing, trigger and control (TTC) distribution system. The latency of the level-1 trigger system is 2 µs, of which 600 ns are due to transit time in cables and to which an additional 500 ns latency has to be added in order to accommodate possible cable routing changes. It uses specialised hardware processors handling 8000 calorimeter trigger cells (analogue) and 208 muon sectors each containing up to 2 muon candidates classified in 6 P_T thresholds.

The inner tracker

The inner tracker [2] consists of three sub-detectors (figure 3): the pixel detector, the semiconductor tracker (SCT) and the transition radiation tracker (TRT).

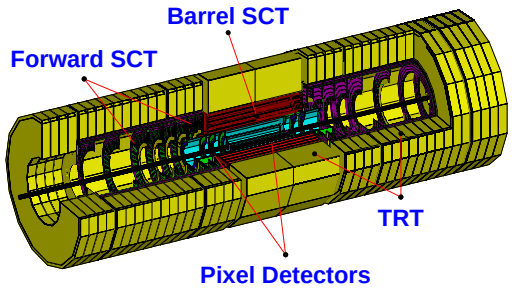

Figure 3. The inner tracker

The pixel detector

The pixel detector consists of 2500 modules and about 100 10^6 pixels and gives a spatial resolution of 15 μm in rφ and 100 μm in z. It is exposed to a very high radiation dose (35 Mrad and 6 10^{14} N.cm^{-2} for 10 years of operation). The read-out is based on two chips: a front-end chip (FED) and a module controller chip (MCC). A module consists of 16 FED chips bump bounded on the detector (Figure 4).

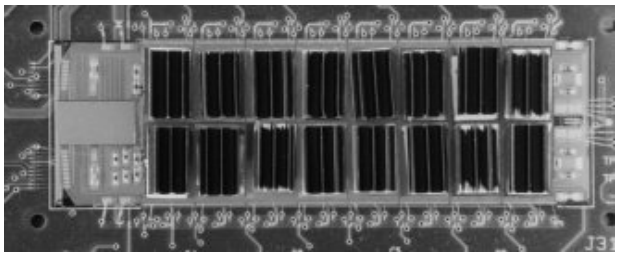

Figure 4. A pixel module

Both FED and MCC have been prototyped in DMILL. There are severe problems with the FED and some work is being done with TEMIC in order to understand them. If it is necessary to change technology the schedule will have to be revised.

The SCT detector

The SCT consists of 6 10^6 silicon strips and should provide a spatial resolution of 20 μm. The read-out is based on the so-called binary solution: the analog signal is amplified and discriminated and only one bit of information per channel is kept in the level-1 pipeline for later readout. As the average occupancy of the detector is small, the data are zero-suppressed before being put in the derandomiser. When a L1A occurs, the data corresponding to three consecutive bunch crossings are read-out. Up to 8 events can be stored in order to accommodate a dead-time smaller than 1% when the L1A rate is 75 kHz.

A single 128-channel BiCMOS chip in DMILL technology, ABCD, will be used. This chips is now in preproduction and some work is going on with TEMIC in order to optimise the yield.

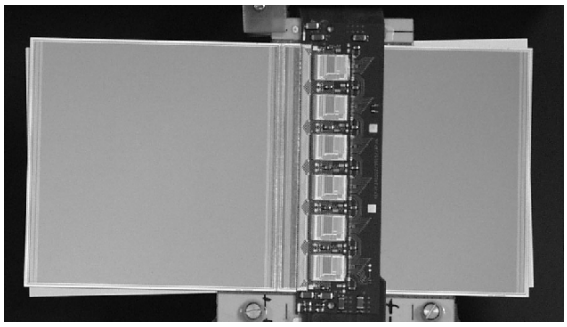

Figure 5. An SCT module

The detector is organised in modules (figure 5), which consists of two hybrids housing 6 128-channel read-out electronics. One module is read-out through two optical links and receives timing, trigger and control through one optical link.

The data transmission runs at 40 Mbits/s and the off-detector ROD receives up to 32 data links.

The optical elements of the links are LEDs for the emission and Pin diode for the TTC reception. A special chip (LDC) drives the LEDs. The TTC is using a bi-phased mark code, which is decoded by another chip (DORIC). Two VCSELs and one Pin diode are housed in an opto-package.

The TRT detector

The TRT is a gaseous detector, which has two functions: continuous tracking with a spatial resolution better than 200 μm and electron identification using the transition radiation effect. It is formed of 420000 straws of about 50 cm length and 4 mm diameter embedded in foam.

Due to the size of the detecting element, the occupancy is quite high; to avoid pile-up, the front-end analog stage has to cancel the tail of the signal caused by ion drift in the straw.
The front-end system consists of two chips: an amplifier shaper discriminator (ASDBLR) followed by a digital read-out chip (DTMROC).
The 8-channel bipolar ASDBLR chip includes a pre-amplifier, a shaper, an ion tail cancellation circuitry, a base line restorer and two discriminators. One discriminator has a high threshold and is used to detect transition radiation X-rays and hence electron candidates. The other one has a low threshold to detect minimum ionising particles for tracking.
The 16-channel CMOS DTMROC chip receives the two discriminator signals per channel. The high threshold signal is simply stored in the pipeline while the low threshold signal is digitised every 3.125 ns. This allows the drift time of the ionising electrons in the straws to be measured and hence to obtain a very good spatial resolution.
There are 9 bits of information stored in the pipeline per straw and per bunch crossing. When a level-1 trigger occurs, three consecutive time slices are read-out to take into account the total drift time in the straw (about 40 ns). This leads to a fairly large amount of data per event and it is necessary to have one 40 Mbits/s link per 16 channels, ie. a total number of 27000, to transmit the data to the off-detector RODs. For reasons of economy these links are copper shielded twisted pairs using the Low Voltage Differential Signal (LVDS) standard.
Both chips have been prototyped in DMILL and are working within the specifications. There are still two concerns: the dispersion of the thresholds in the ASDBLR and the yield of the DTMROC which is a large chip (71 mm^2). The production of these chips should start in 2001.

The ATLAS calorimeters

The ATLAS calorimetry [3,4] is based on two technologies. Liquid Argon is used for the electro-magnetic calorimetry and the end-cap hadronic calorimetry. Scintillating tiles are used for the barrel and extended barrel hadronic calorimetry. There are 200000 channels in the Liquid Argon part and 10000 channels in the tiles part.

The Liquid Argon calorimeter

The read-out of the Liquid Argon calorimeter is based on a multi-gain shaper and a 144-cell analogue pipeline (SCA). In parallel to the read-out part, analogue summation electronics forms the trigger towers and transmits them to the level-1 calorimeter trigger system. When a L1A signal occurs, five consecutive time slices are digitised by an ADC (12 bits, 10 MHz) and the digital data are sent to the ROD through Gigabit optical links (G-Link from HP). Eight channels share a common ADC.
The front-end system is housed in 60 crates, each of which handles about 3000 channels, located inside the detector. These crates contain four types of module (figure 6):

- 128-channel front-end board containing the read-out electronics and one gigabit link driver.
- The tower builder board.
- The timing and control interface.
- The calibration electronics.

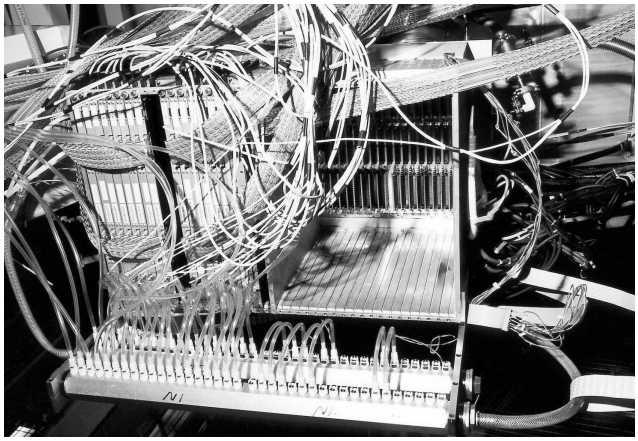
Figure 6. Liquid Argon front-end crate with its cooling tubes

A complete radiation tolerant system (two crates) will be available in the course of 2001. In order to meet this milestone, several ASICs are being designed in a radiation hard technology (DMILL).

The Tile calorimeter

The read-out is based on a bi-gain shaper followed by two 12-bit, 40 MHz ADCs and a digital pipeline (figure 7). The electronics is housed inside the detector and has been qualified against radiation. It is currently being produced.

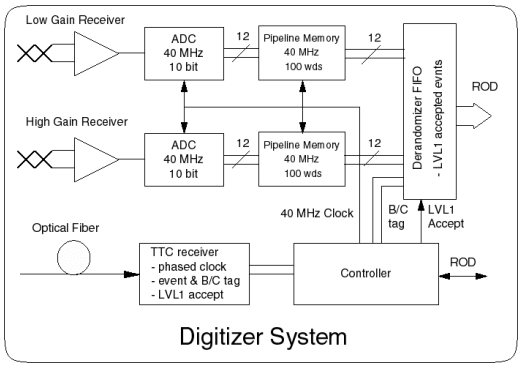

Figure 7. Tiles calorimeter read-out electronics

The Muon Spectrometer

The muon spectrometer [5] is based on four types of chambers: the Monitored Drift Tube (MDT) and the Cathode Strip Chambers (CSC) to obtain precise coordinates and the Resistive Plate Chambers (RPC) and Thin Gap Chambers (TGC) for the trigger.
There is a total of 1.3 10^6 electronics channels.

The MDT Chambers

The MDT chambers are drift time chambers giving a 80 μm spatial resolution.
The read-out electronics is based on an amplifier-shaper-discriminator (ASD) followed by a TDC (figure 8). Each channel of the ASD consists of a differential input stage, a tail cancellation circuitry, two discriminators and a gated integrator.

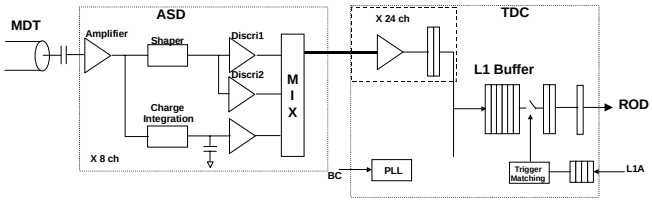

Figure 8. The MDT read-out electronics

The TDC is a 24-channel chip and the timing measurement is done by dividing the 40 MHz clock into 32 intervals, providing 800 ps bins. The hits are stored in a level-1 buffer and when a L1A occurs, a matching function allows to retrieve data belonging to the appropriate time window. The read-out is then done serially and up to 4 TDCs can share the same link.
Both ASD and TDC chips are CMOS and their production will start in 2001.

The Trigger Chambers

The two types of trigger chambers are read-out in a very similar way (figure 9 shows the RPC read-out).

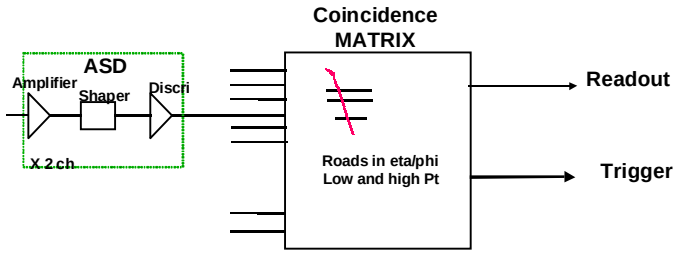

Figure 9. The RPC read-out electronics

The amplifier-shaper-discriminator (ASD, using GaAs technology for the RPC and bipolar technology for the TGC) provides data to the coincidence matrix chip (CMOS in both cases) which looks for tracks at different Pt and includes the read-out part. Two additional stages are necessary before a full sector information is sent to the level-1 trigger system.
The ASD chips of both TGCs and RPCs are now being produced together with the front-end boards which house them.

Common ATLAS issues

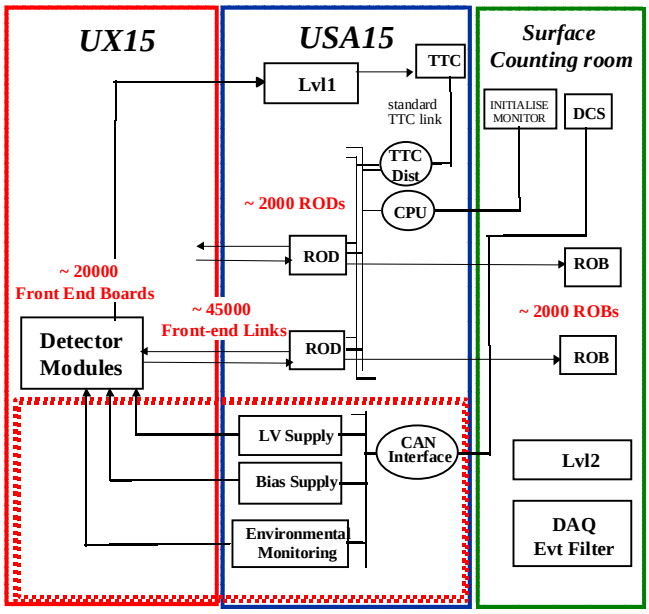

Figure 10. System overview

The system overview shown in figure 18, helps to identify common system issues:

- There are about 20000 front-end boards or modules which have to be radiation hard or radiation tolerant.
- Grounding and power distribution have to be done in a coherent way if the required noise performance at system level level is to be obtained.
- The location of the power supplies is of importance as substantial power is involved and it influences the quantity of copper necessary to bring the power in the detector and the in-line losses.
- The front-end links connecting the on-detector electronics to the RODs deserve special attention if one wants to save development costs and harmonise the system.
- The timing of the experiment and the dead-time control has to be worked out at the experiment level and in a coherent fashion.
- The slow control system has to be uniform across the experiment.
- Reliable electronics must be produced, tested, installed and maintained for a number of years. A comprehensive quality assurance system should help to meet this goal.

Design Reviews

Production Readiness Reviews (PRR) are ATLAS wide mandatory reviews which are made prior to the commitment of major funds. During these reviews, the production documents and QA plans are checked. For the electronics, design reviews are held before the PRR in order to have enough time to look at the design. This has proven to be necessary and useful. For instance, several reviews have been necessary before the fabrication of most of the ASICs deigned. The scope of the reviews and the points to be addressed have been documented for chips and systems [6].
These reviews require the participation of all institutes as 2 to 4 reviewers per design and much preparatory work are necessary.

Radiation hard electronics

Table 1 gives the list of chips which are being designed or produced for ATLAS. As can be seen most of them are using the DMILL BiCMOS technology but back-up solutions in other rad-hard technologies exist in most of the cases (as requested by the approved ATLAS policy on radiation hard electronics).
The main problems with radiation hard technologies are the low volume production leading to low yield and high cost. The read-out chip for the pixels is currently a very critical item as a first DMILL prototype was produced a year ago and sstill does not work as expected. There is a on-going work with ATMEL in order to try and understand the problems. In case this is not solved rapidly a change of technology will be necessary and there will be a significant impact on the schedule.
Another concern is the fact that the design teams are linked to the sub-detector collaborations. It often leads to scattered teams. For instance the TRT DTMROC chip has been designed by people from Lund, Philadelphia, Cracow, Geneva, Michigan and CERN. This is very good for telecom companies but not optimal for the project...
The availability of frame contracts with ATMEL for the TEMIC technology and with IBM for the CMOS 0.25 μm technology is a great help as it simplifies the ordering process and allows a good cost evaluation.

System	Chip	Techno	Size mm^2	Status
Pixels				
	FE-D	DMILL	80	Prototyped
	FE-D	H. SOI		
	Control	DMILL		Prototyped
SCT				
	ABCD	DMILL	51	Pre-production
	DORIC	AMS	5	Reviewed
	VDC	AMS	4	Reviewed
TRT				
	ASDBLR	DMILL	12	Prototyped
	DTMROC	DMILL	71	Prototyped
LARG				
	SCA	DMILL	30	Reviewed
	SCA Controller	DMILL	100	
	Gain Selector	DMILL	21	Reviewed
	BiMUX	DMILL	5	Prototyped
	DAC	DMILL	6	Reviewed
	SPAC slave	DMILL	27	Reviewed
	OpAmp	DMILL	2	Reviewed
	Config. Controller	DMILL	20	Reviewed
	MUX	DMILL	18	
	Calibration Logic	DMILL	16	Reviewed
Services				
	TTCrx	DMILL	27	Prototyped
	PHOS4	DMILL	6	Prototyped

Table 1. Radiation hard chips

Radiation tolerant electronics

We realised early on that radiation would be a major issue as the first “ATLAS policy for radiation tolerant electronics” was published at the end of 1996. The last two years have shown that it was a very serious problem. Take two examples:

- During the design review of the Tile calorimeter high voltage distribution, additional radiation tests were requested. These tests showed that the design

was too much sensitive to neutrons. It took about 10 months to fix the design and to validate it.

- For the Liquid argon front-end boards a lot of high performance components are needed. Some preliminary tests on COTS were not satisfactory. It was then decided to design 9 chips in rad-hard technology.

In all cases it costed time and money.

An updated “Atlas policy on radiation tolerant electronics” [7] has been set-up during the last two years. It defines the strategy for component procurement, the radiation tolerance criteria (including safety factors) and the standard test methods (ionising dose, displacement damages, SEU) to be used. A WEB repository [8] has been created in order to make available the results of the tests done in ATLAS.
This policy has been defined by an ad-hoc working group and its acceptance in ATLAS allows us to be sure that every sub-system speaks the same language and that the tests and radiation constraint estimations are done in the same way.
The existence of RD49 [9] (Radtol) project is a great help.

Grounding

ATLAS has defined an overall grounding policy [10]. Each sub-detector must be isolated with respect to the others and there must be no ground connection from the on-detector system to the off-detector. The power supplies must be floating and signal transmission must use either optical links or shielded twisted pairs. Every system has produced a grounding plan and a detailed implementation has been done by some of them. Figure 11 shows the TRT implementation [11]. This aspect needs to be addressed during the reviews and will generate a non-negligible follow-up work as it is very easy to achieve an implementation completely different from the intended design.

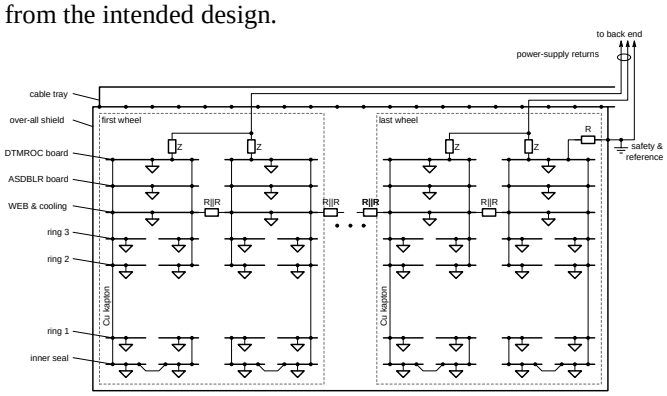

Figure 11. TRT grounding scheme

Power supplies

There is a strong wish to have the power supplies in the cavern. The radiation level and the stray magnetic field must be properly taken into account and may require some special developments.
Measurements have been done at BNL and CERN (with ESS group and CMS) showing that the feedback opto-couplers of DC-DC converters are sensitive to neutrons and that special devices must be used. Another critical point is the sensitivity to single event burn-out of their MOSFET transistors. This was clearly identified during tests done by BNL.
Measurements have shown that magnetic fields below 200 gauss do not pose problem and measurements at CERN have shown that reasonable shielding allows power supplies to work in magnetic fields of up to 1kGauss.
A joint program of work and a common approach to technical and commercial issues is being set-up in ATLAS. Its goal is to provide some common "bricks” which could be used by several sub-systems to cover their needs (Table 2).

System	No. of modules	Power/module (W)	No. of voltages
Pixels	1000	48	7
SCT	4088	9	7
TRT	1500	50	3
LARG	58	3300	7
	8	200	6
Tiles	32	2200	7
Muons			
MDT	1200	40	2/3
CSC	64	40	2/3
RPC	550	60	2/3
TGC	600	60	2/3

Table 2. Power supply requirements

Front-end links

An ATLAS front-end links working group [12] has produced a lot of very valuable work, such as a links specification document, the coordination of radiation testing program and a safety document which has been and reviewed by the CERN safety division.
All ATLAS front-end links are digital and can be classified into two categories:

- Rad-hard 40 MHz;
- Rad-tolerant 1.28 Gbits/s.

All optical links use VCSEL devices and multimode fibres. 40 MHz over 100 m copper links have been demonstrated (see Figure 12).

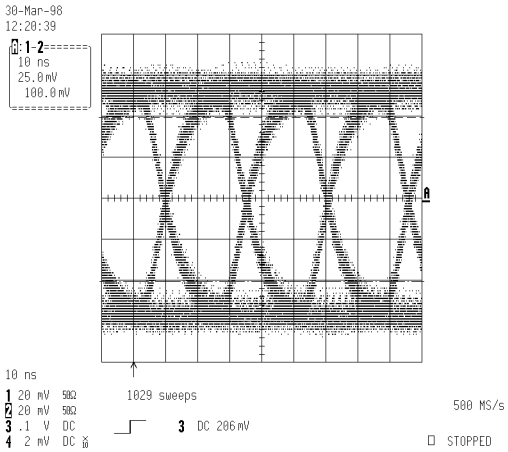

Figure 12. Eye pattern of a 100m 40MHz LVDS copper link after cable compensation.

Two packages are being developed for the 40 MHz rad-hard optical links to be used in the inner tracker. They both contain two emitters and one receiver. A GEC opto-package is available in small quantity and their tests and assembly procedures are being improved. Prototypes are also available from Academia SINICA (Taipei). Measurements have shown that single event effects in PIN diode increase the bit error rate and will produce some synchronisation errors.
The radiation tolerant 1.28 Gbits/s links (mainly used by the liquid argon calorimeter and the muon trigger system) are based on the G-link chip-set. Single event upsets in the serialiser have been seen. The impact on the system is being analysed and some solutions such as the use of a double serialiser are being envisaged.

Back end electronics

It consists in the Read-out drivers (ROD) and the Read-out Buffers (ROB) as shown in Figure 1.
The RODs gather front-end elements in trigger region of interest. They process the data (data compression, zero suppression), format them according to the ATLAS event format and transmit them to the ROBs which are data sources for high level triggers and data acquisition system.
The RODs are sub-detector specific but some common features have been agreed, such as:

- Link to ROBs;
- Crate backplane: VME64x;
- Data format;
- Dead-time handling.

Some other common features are still under discussion:

- Interface to crate processor;
- VME interface capability;
- Error recovery.

The RODs have to deal with different types of errors. They could be front-end data corruption, synchronisation errors (false bunch crossing identifier [BCID] or event number [L1ID]) caused by single event upsets in the front-end readout chips or electromagnetic interferences, ... The RODs are able to detect the errors and to flag their occurrence. The data acquisition system should not be stopped when an error is found. Persistent errors need to be cured. For instance synchronisation errors are cured by appropriate resets (BCID is reset every LHC turn, L1ID is reset periodically).

Timing of the experiment

The timing (BC clock) and trigger are distributed from the central trigger logic to the read-out elements through the RD12 optical fan-out system [13]. This system either stops at the ROD level where a protocol conversion is performed (as is done in the inner tracker) or goes up to the front-end level.
There must be a partitioning between sub-system and within each sub-system to allow independent commissioning, debugging and calibration. A partition consists of an interface module (TTCvi) which selects the timing and trigger signal source (either from the experiment or sub-detector specific) and feeds the encoder and electrical-to-optical converter (TTCex, TTCtx). It is planned to have up to four independent partitions per sub-system.
There is a need for a strategy to adjust the timing of the experiment. It is based on the structure of the LHC cycle, the availability of a BCID in the front-end electronics and the knowledge of the length of certain fibres or cables [1].

Dead-time control

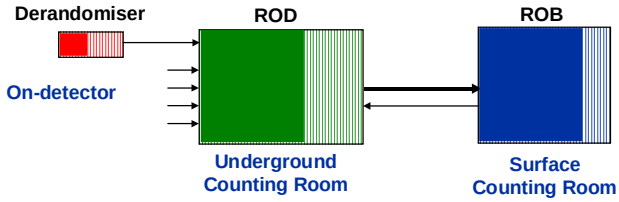

Figure 13. Buffer control

There are buffers at different levels (figure 13) which can be filled and hence introduce dead-time. The handling of the dead-time depends on which buffer is concerned.

Derandomiser
After each L1A a 4 BC dead-time is introduced by the Central Trigger Processor. To handle the filling of the front-end derandomisers, a limited number of L1A within a given time window is allowed (leaky bucket algorithm). Currently, the baseline is to have less than 8 L1A within 80 µs. The deadtime introduced by this algorithm is very small as can be seen in figure 14 and in [14].

ROD
If the ROD buffers, a BUSY signal is generated and hierarchically propagated to the CTP to throttle the L1A rate [1].

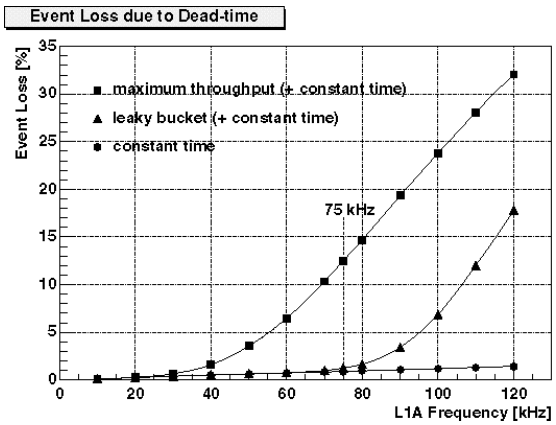

Figure 14. Event loss due to dead-time

ROB
The BUSY mechanism at the ROB level is neither efficient nor practical isnce before introducing dead-time it is necessary to know the status of the previous buffers. An XOFF mechanism is implemented on the readout link to apply back-pressure on the RODs. When applied, the ROD buffers fill and a BUSY signal can be generated if necessary.

Racks and cables
There will be electronics racks in the cavern (UX15) and in two underground counting rooms (USA15 [Figure 15] and US15). There will be cables from the detector to these racks.
An inventory work has started in ATLAS in order to allocate the racks to different sub-systems and to prepare the cabling work.
Two databases are made available for this purpose [15], [16].

Crates
It has been decided to have common crates in ATLAS for the back-end electronics. It will be 6U or 9U (Figure 16) VME64x crates. The following points are considered to be important for ATLAS:
- The crate must be low cost;
- Its maintenance must be easy;
- It should use standard elements;
- It must be integrated in the cooling and control systems of ATLAS.

The specifications are being finalised [16]. Another database [17] allows sub-system requirements (quantity and date of availability) to be stored.

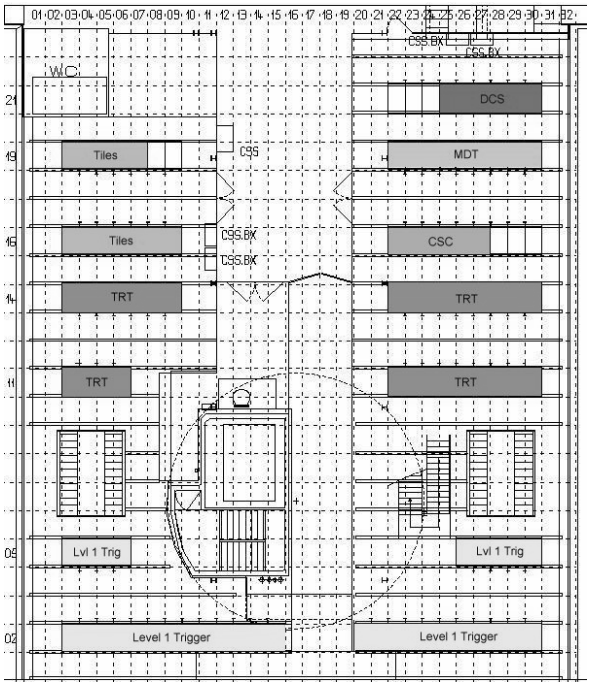

Figure 15. USA15 Niveau-1

Production
There will be several tens of thousands of chips and boards to be produced, mainly by industry. The tests will often be done by the institutes and this may be a very long process if testing has not been foreseen at the design phase and/or if the quality of the industrial work is not good enough. Hence it is very important that testing facilities and quality assurance plans are reviewed before the production starts.
Production databases must be developed to store some information for traceability purpose and for future

calibration work. The electronics should benefit a lot from similar work done for the detectors construction.

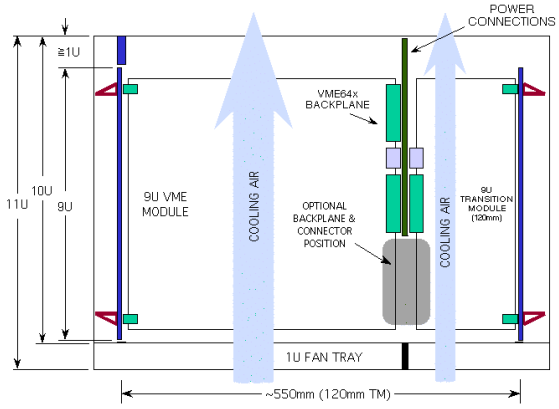

Figure 16. Possible crate lay-out

Maintenance

The electronics inside the detector has to be as much reliable as possible because the maintenance scenarios are extremely discouraging…

The maintenance of the industrially supported electronics (backend, most of the power supplies,…) has to be foreseen during the design phase in order to simplify procedures and to ensure adequate funding. We can benefit from the LEP experiments which have had to maintain electronics during ten years and from which we can extract valuable data. For instance, the failure rate of the Fastbus power supplies in DELPHI[1] has been monitored during the last ten years. Figure 17 shows the yearly failure rate and the expected failure rate assuming a 65000 hours MTBF (constructor data). One can see that it is reasonably predictable.

The maintenance of the electronics designed and built in the institutes is, in general, properly done. The main problem consists in maintaining the documentation of the different systems. We can now make use of EDMS and of its interface to the CAE tools (mainly CADENCE) [19].

[1] Thanks to Philippe Gavillet

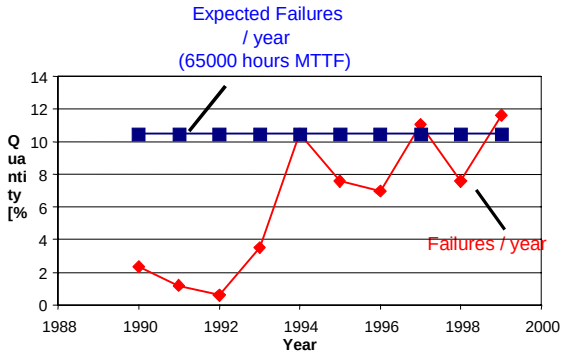

Figure 17. Failure rate of the DELPHI Fastbus power supplies

Summary

The designs of rad-hard ASICs are close to completion but there are still some worries for the production.

Concerning the radiation tolerant electronics, a huge effort has been made in order to obtain coherent and consistent measurements across the experiment. There are evidences of SEE problems which may be very troublesome in certain cases and whose impact on the experiment need to be analysed.

The review procedures are now well established and the reviews have been proven to be very useful.

The grounding and shielding study is in good progress. Its implementation will require a substantial amount of follow-up work.

Several common activities are going on. They concern the power supplies, the links, the racks and crates and the cables.

Despite the enormous work produced so far and the progresses that have been made, there is still an important point missing: large scale system tests have not yet been done in most of the sub-detectors.

Disclaimer

The time available to write this article has been extremely short. As a consequence, it has not been possible to circulate it in the ATLAS community and hence it may happen that some information is incomplete or out-of-date. The author apologises for any such event.

References

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