Status of the 80Mbit/s Receiver for the CMS digital optical link

F. Faccio, C. Azevedo, K. Gill, P. Moreira, A. Marchioro, F. Vasey

CERN, CH-1211 Geneva 23, Switzerland
(e-mail: Federico.Faccio@cern.ch)

Abstract

The first prototype of the 80Mbit/s optical receiver ASIC for the CMS digital optical link has been manufactured in a 0.25µm commercial CMOS process. The circuit design has been made using radiation tolerant layout techniques. Its performance satisfies the low power, wide dynamic range, sensitivity and speed specifications. The radiation hardness of the receiver has been verified irradiating the diode with 6MeV neutrons (up to $6.5 \cdot 10^{14}$ n/cm^2) and the receiver circuit with 10KeV X-rays (up to 20 Mrad). A second prototype has been submitted for fabrication in the same commercial CMOS process.

I. INTRODUCTION

The CMS tracker control system will use approximately 1000 digital optical links for the transmission of timing, trigger and control signals [1]. These digital signals, transmitted serially at a bitrate of 40 Mbit/s (80 Mbit/s for the clock signal), will be converted into electrical signals by an optical receiver. One of the transmission channel ends will sit inside the detector, in the radiation environment of the tracker: its components need therefore to be radiation hard.

The envisaged solution is the use of a selected commercial PIN photodiode able to stand the high particle fluence expected, coupled to a radiation-tolerant ASIC. The exigency of developing an ASIC comes from the lack of a commercial radiation-tolerant circuit satisfying the specifications in terms of low-power, speed and sensitivity.

An extensive irradiation work has been performed to select commercial photodiodes for the radiation environment of the CMS tracker [2]. The principal candidate for the time being is the Fermionics FD80S-8F, an InGaAs/InP detector with 80µm diameter and approximately 2µm active InGaAs layer thickness on an InP substrate. The radiation hardness of this photodiode type has been demonstrated up to a neutron fluence in excess of $6.5 \cdot 10^{14}$ n/cm^2 [2].

The ASIC has been developed in a commercial quarter micron process using radiation tolerant layout techniques to achieve the required radiation hardness of 10 Mrad. This design approach is now attractive because of the decreasing thickness of the gate oxide in present day submicron CMOS technologies. Since the eary 80's, it has been demonstrated that radiation effects decrease dramatically for oxides thinner than about 10 nm [3]. Such critical thickness has been reached for commercial CMOS processes already a few technological generations ago, and the increase of the radiation tolerance with down-scaling has been verified in several works since [4, 5].

The radiation tolerant layout approach used in the optical receiver design is based on the use of enclosed shapes for the NMOS transistors and of guardrings. This technique prevents the opening of any leakage current path due to radiation-induced charge trapping in the still thick field oxide, and has been demonstrated on simple devices and complex mixed-signal circuits up to multi-Mrad total dose levels [6]. Additionally, the use of guardrings is an effective tool to decrease the sensitivity to Single Event Latchup (SEL) [7].

The design of the optical receiver ASIC has already been described in details in [8]. In this paper, we present the measurement of the performance of the first circuit prototype. Irradiation results that verify the radiation hardness of the circuit are also included. Finally, we describe the slightly modified version of the ASIC that has been submitted for the final prototype.

II. THE OPTICAL RECEIVER

The global architecture of the optical receiver is shown in Figure 1, and its details are described in [8]. The main specifications for the receiver are summarised in Table 1. The PIN diode is connected to the receiver circuit, which is mainly composed of four blocks: a transresistance preamplifier, a chain of limiting gain amplifiers, an LVDS driver and a block to detect and generate the reset signal. The PIN diode is DC coupled to the preamplifier, which also supplies the bias voltage to the photodiode (about 1.8 V). This solution also allows for an easy integration of a feedback loop to sink the radiation-induced leakage current of the photodiode.

Another feedback loop in the preamplifier controls the value of the variable transresistance. This sort of Automatic Gain Control (AGC) is necessary to cope with the large dynamic range required for the amplifier and optimises the noise performance: maximum gain (maximum transresistance), hence minimum noise, is used for small signals.

Both feedback loops need to be slow so as to be negligible at the signal frequency as they have to compensate for the slow radiation-induced damage in the PIN photodiodes. The quantum efficiency of the diode will

in fact decrease, and its leakage current will increase, during the whole LHC life cycle (10 years).

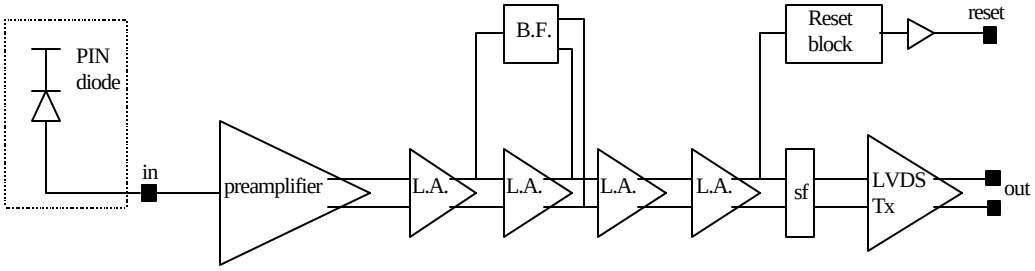

Figure 1: Global architecture of the amplifier circuit, DC connected to the external PIN diode. The transresistance preamplifier is followed by a chain of limiting amplifiers (L.A.), where a Balancing Feedback (B.F.) block ensures that the average of the two differential signals is identical.

Table 1: Main specifications for the optical receiver.

DC input current (PIN diode leakage current)	< 100 µA
AC input signal amplitude	-20 dBm ÷ -3 dBm
Bandwidth	> 80 MHz
Output voltage level	LVDS
Supply voltage	2.5 V
Power consumption	< 300 mW/channel
Bit Error Rate	10^{-12}
Sensitivity	< -20 dBm after irrad.

The limiting amplifier chain performs an amplification of the signal and limits it to a pre-fixed peak-to-peak value, preparing it for optimum input to the LVDS driver. The LVDS driver has been designed as a differential amplifier with load resistors, and its speed performance is well above the required 80 Mbit/s.

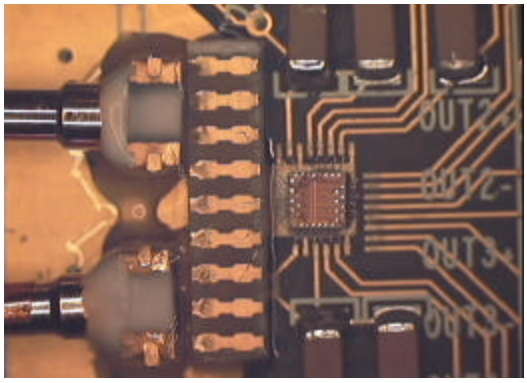

Figure 2: Two channels of the ASIC are bonded to two Fermionics photodiodes in the test board.

At the time of the first prototype design, the transmission protocol foresaw a reset signal coded as missing pulses for a long time period on the data line (2 µs or more) [9]. The amplifier circuit is required to detect the transmission of the reset and respond to it by changing the status of a flag on a dedicated output line. To perform this task, we have integrated a reset block in the amplifier, connected to one of the differential outputs of the limiting gain amplifier chain as shown in Figure 1. The reset transmission has since been differently coded, as missing signal for 20 clock cycles, and the design modifications to cope with this requirement will be described later.

The prototype ASIC includes 4 amplifier channels, each occupying an active area of 0.5x0.25 mm^2. The distance amongst the pads has been chosen to be compatible with wire-bonding and low cost bump-bonding techniques. The circuit was fabricated, then mounted on a dedicated test board bonding two channels to two Fermionics PIN photodiodes, as shown in Figure 2. One of the two diodes had been previously irradiated with neutrons (mean energy 6 MeV) to a level of $6.5 \cdot 10^{14}$ cm^{-2}, whilst the other was new.

III. OPTICAL RECEIVER PERFORMANCE

A. Measurement of the circuit functionality

The chip has been measured and the performance is well within all specifications. The current consumption for the full chip is about 50 mA, which for the operating voltage of 2.5 V corresponds to a power consumption of 125 mW, or approximately 32 mW/channel. We could test the functionality of the AGC over a wide input signal range up to +2.8 dBm (1.9 mA) without observing any sign of saturation: a dynamic range of more than 30 dB is therefore achieved. Increasing the DC level of the input signal to simulate the radiation-induced photodiode leakage current, we could test with success the functionality of the leakage compensation feedback loop up to 200 µA. The circuit performance is not affected by a change of the power supply voltage of ±20% around the nominal value of 2.5 V. Figure 3 shows an example eye diagram measured at the output of one of the receiver channels for an input signal modulation amplitude of –20 dBm at 80 MHz. In the lower picture, it is possible to appreciate the increase of the noise in presence of a diode leakage current of about 130 µA.

B. Bit Error Rate (BER) measurements

The most complete way to assess the transmission quality of a digital optical link is to measure its Bit Error Rate (BER), defined as the ratio of incorrectly received bits to the total number of bits received. We performed this measurement at a bit rate of 80 Mbit/s.

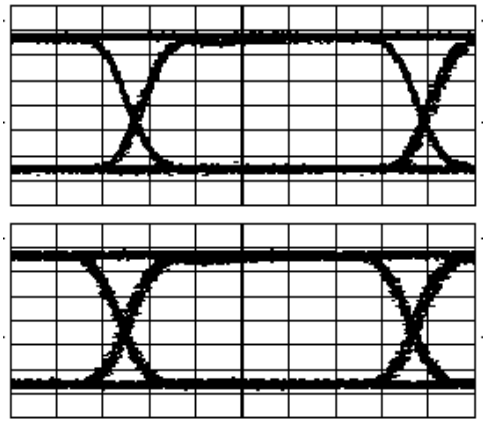

Figure 3: Eye diagram measured at the output of the receiver circuit (input signal = 10 µA at 80 MHz). Measurements performed without (top) and with (bottom) an input DC current of 130 µA. X-axis: 50 mV/divison. Y-axis: 2 ns/division.

We measured the BER of one optical channel of the receiver (the channel where the new photodiode was mounted) and evaluated the impact of the channel-to-channel crosstalk and of noise on the power supply line. The result is shown in Figure 4. We first measured the BER of the optical channel while keeping the other channel silent ("no crosstalk"). As in the application two channels will operate at the same time, this measurement is only representative of the "absolute" channel performance. Then, an uncorrelated signal of maximum amplitude (-3 dBm) was applied to the neighbour channel, and the measurement was repeated ("crosstalk"). This measurement, which is representative of the application, shows that the specified BER of 10^{-12} is achieved for an input optical power of about –27 dBm. Finally, this last measurement was repeated while simultaneously introducing a 20 mV peak-to-peak signal on the 2.5 V power supply ("crosstalk + noise on PS") to evaluate the Power Supply Rejection Ratio (PSRR) of the circuit. Even in this severe condition, the knee of the BER curve is around –24 dBm. The same set of measurements was repeated with very similar results on the channel where the irradiated photodiode was bonded. The diode was actually irradiated with neutrons several months before this measurement, and the damage from the neutron irradiation was very limited: the efficiency decreased by about 10% and the leakage current rose to less than 5 µA [2].

In presence of a leakage current from the photodiode, we expect the BER performance to degrade. This current is sunk to ground by an NMOS transistor whose drain is connected to the preamplifier input, introducing an additional noise source. We measured the performance degradation repeating the BER measurement in the "crosstalk" condition, and simulating the diode leakage current by increasing the input signal DC level. The comparison with the absence of leakage current in shows that the performance penalty is less than 1 dB for the highest current of 96 µA.

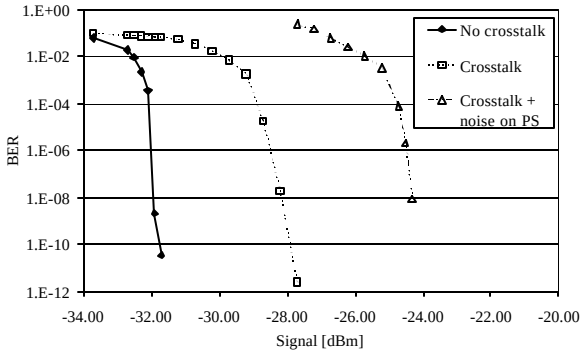

Figure 4: BER measured on one of the optical channels in different conditions.

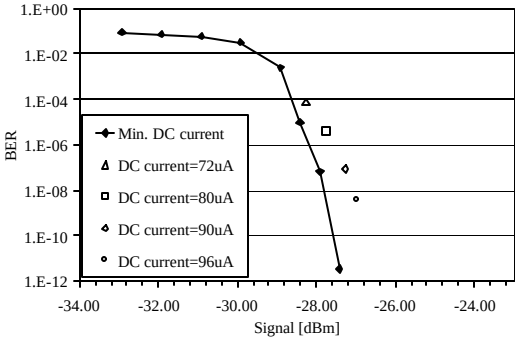

Figure 5: Influence of increasing levels of DC input current on the BER. The measurements were made in the "crosstalk" condition and simulate the effect of radiation-induced leakage current in the diode.

A final BER measurement was made to evaluate the receiver performance in the real operational condition, that is when both the clock and the data pattern are transmitted through the optical link. The two optical channels were therefore used, one to transmit the 80 MHz clock (signal amplitude: -3.46 dBm; DC current: 100 µA) and the other for the data pattern (signal amplitude: -18.5 dBm; DC input current: 96 µA). This represent a condition which is very close to the worse possible according to the design specification, with the additional use of an irradiated photodiode for the optical line where data were transmitted. In these conditions, the transmission line run without any error for 15 days and 14 hours, which indicates a BER below $9.27 \cdot 10^{-15}$.

C. Detection of the reset

At the time of designing the first ASIC prototype, the reset signal was foreseen to be transmitted through the data line as missing signal for more than 2 µs. The block to detect the reset was designed to comply with this scheme, and actually proved to work correctly. In Figure 6, the reset output from the ASIC is enabled (signal "high") about 2.45 µs after the stop of the input signal, and disabled when the signal is transmitted again.

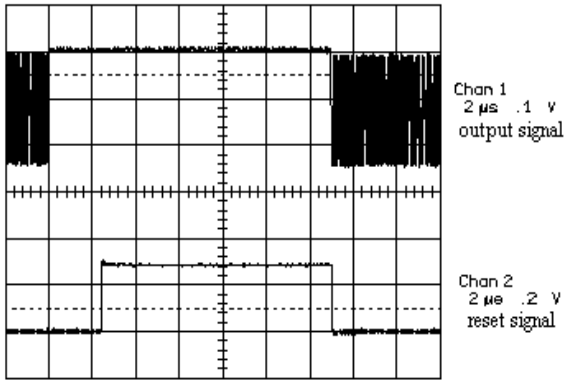

Figure 6: The reset signal (bottom plot) is enabled about 2.45 µs after the input signal (top plot) is stopped.

This scheme has proven in the measurement not to be very reliable. In particular, in the absence of input signal for a time longer than about 20 µs (which can happen when the transmission line is down for any reason), the gain of the preamplifier is set to its maximum value by the AGC. In this condition, noise at the preamplifier input can be amplified up to generate a full-swing signal at the output of the limiting amplifier chain. This in turn induces the reset output to randomly switch from high to low, and no clear reset signal is produced.

It is therefore preferable to change to a scheme where the reset can be transmitted in a time much shorter than the time constant of the AGC feedback loop. Since it does not affect the equilibrium point of the two slow loops, this scheme allows the transmission of valid data immediately after the transmission of the reset.

IV. IRRADIATION RESULTS

The receiver circuit has been irradiated with X-rays at our SEIFERT RP-149 irradiation system, which produces a spectrum peaked at about 10 keV. The irradiation took place at room temperature up to a total dose of 20 Mrad(SiO_2), at a dose rate of about 18.4 krad(SiO_2)/min. The functional test performed after irradiation showed that a 6% increase of the power consumption was the only measurable effect. To more precisely evaluate the impact of the irradiation, we repeated the BER measurement, then put the chip in the oven for an annealing at high temperature for 168 hours. Due to the presence of materials possibly damageable on the test board, we did not apply the standard 100°C [10] during the annealing, but we limited the temperature to 80°C. After annealing, the BER measurement was repeated again. Since no difference was observed in both the power consumption and the BER performance immediately after irradiation and after the annealing, only the after-annealing results are shown.

The radiation-induced performance degradation is observable in the BER curve measured on one optical channel while the other channel is kept silent. In that case, the shift of the knee towards bigger signal is limited to about 1 dB, as shown in Figure 7.

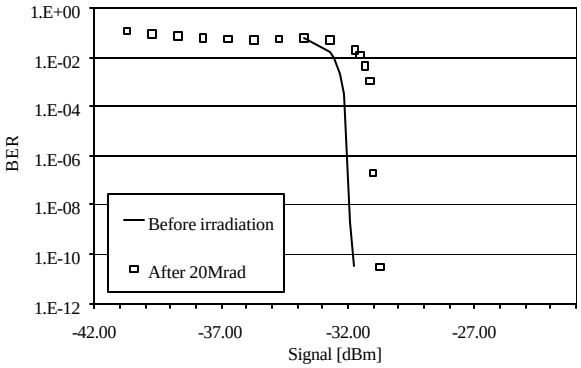

Figure 7: Shift in the BER curve induced by an irradiation up to 20 Mrad(SiO_2).

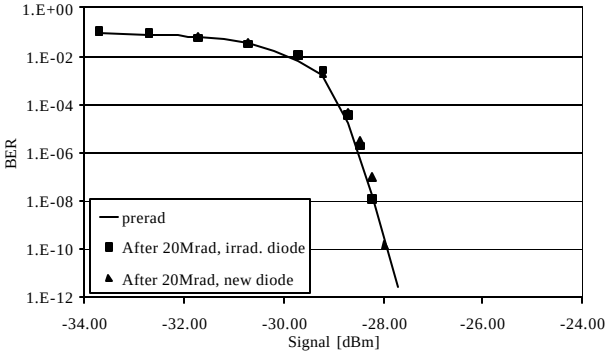

Figure 8: BER before and after irradiation in the "crosstalk" condition (representative of the application).

When the measurement is repeated in the "crosstalk" condition, that is with the neighbour channel operational, the BER curve superposes to the one measured before irradiation. Moreover, Figure 8 shows that no difference is observed between the two optical channels, even though one of them actually mounts an irradiated photodiode. Also in the presence of noise injected on the power supply, the BER performance is not affected by the irradiation.

V. DESIGN MODIFICATIONS

The first design modification has been introduced to agree with an upgrade of the circuit specifications

requiring an increase of the maximum DC input current up to at least 300 µA. This has been achieved by increasing the size of the NMOS transistor whose drain is connected to the preamplifier input to sink the photodiode leakage current. Simultaneously, the DC current in the input branch has been increased and the size of the transistor in parallel to the preamplifier feedback resistance has been decreased.

As anticipated in 3.3, the scheme for the transmission of the reset has been changed. The new scheme requires the consecutive transmission of zeros on the data line for 20 clock cycles (500 ns). The reset detection block in the first prototype has been replaced by another block sensing the output of the first limiting gain amplifier of the chain. In the new block, a RC circuit fixes the time constant for the reset detection: in case of transmission of zeros for a longer time, the reset signal is enabled at the circuit output. The duration of this reset signal is determined by the time constant of another RC, and has been chosen to be about 8 µs. Also the polarity of the reset signal at the ASIC output has been changed: the reset is now active for an output "low".

In 3.3 we pointed out that, in the absence of input signal for a long time, the noise at the preamplifier input could generate full-swing random signals at the receiver output. To prevent this undesirable effect, the new prototype has been modified so as to disconnect the LVDS output from the input for signals smaller than about –22 dBm. In this case, the LVDS output is stable and the reset output is enabled. Of course, this means that the dynamic range of the receiver has been cut in the new prototype and that no signal below –22 dBm can be received correctly.

Finally, to enable to test the functionality of the ASIC without the need to bond it to the photodiode, an injection block has been implemented to simulate both the DC and AC input signals. This feature will be very useful to discard the bad dices at the moment of the series production of the circuit.

VI. CONCLUSION

The first prototype of the optical receiver developed for the digital optical link of the CMS tracker has been fabricated in a commercial quarter micron CMOS technology. The thin gate oxide of such deep submicron process, together with the systematic use of enclosed NMOS transistors and guardrings in a radiation tolerant design approach, allow to achieve the multi-Mrad radiation tolerance required for the CMS tracker electronics.

The measured performance of the optical receiver is well within specifications: a dynamic range of more than 30 dB is achieved thanks to the use of AGC in the preamplifier, and the 80 MHz bandwidth is easily reached. The leakage current control feedback loop works beyond the required 100 µA to compensate the radiation-induced photodiode leakage current. All these characteristics are unaffected by an X-ray irradiation up to 20 M rad(SiO_2). The power consumption of the four-channel chip amounts to about 125 mW, and increases by only about 6% after irradiation.

We measured the BER of two adjacent optical channels, and found that the required level of 10^{-12} is reached for an optical power of the input signal modulation of about –28 dBm. Also the BER curve measured in these conditions was not affected by the irradiation, confirming the excellent hardness achieved using the radiation tolerant design approach.

A slightly modified version of the receiver circuit has been submitted for fabrication in the same CMOS technology. The modification to the previous design were required to cope with a change in the specification for what concerns the maximum DC input power. Moreover, a change in the detection of the reset signal was necessary to ensure a better reliability in the transmission of the system reset.

REFERENCES

[1] CMS, *The Tracker Project Technical Design Report*, CERN/LHCC 98-6, CMS TDR 5, 18 March 1998

[2] K.Gill *et al*., "Comparative study of radiation hardness of optoelectonic components for the CMS tracker optical links", *Proceedings of the Fourth Workshop on Electronics for LHC Experiments*, Rome, September 21-25, 1998, p.96

[3] N.S. Saks *et al*., "Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides", IEEE Trans. Nucl. Science, Vol.**33**, No.6, p.1185, Dec.1986

[4] G. Anelli *et al*., "Total Dose behavior of submicron and deep submicron CMOS technologies", *Proceedings of the Third Workshop on Electronics for LHC Experiments*, London, U.K., September 1997

[5] J.V.Osborn *et al*., "Total dose hardness of three commecital CMOS microelectronics foundries", *Proceedings of the Fourth European Conference on Radiation and Its Effects on Components and Systems* (RADECS97), Palm Beach, Cannes, France, 15-19 September 1997, p.265

[6] M.Campbell *et al*., "A Pixel Readout Chip for 10-30 Mrad in Standard 0.25 µm CMOS", IEEE Trans. Nucl. Science, Vol.**46**, No.3, p.156, June 1999

[7] T. Aoki, "Dynamics of heavy-ion-induced latchup in CMOS structures", IEEE Trans. El. Dev, Vol.**35**, No.11, p.1885, November 1988

[8] F. Faccio *et al*., "An amplifier with AGC for the 80Mbit/s Optical Receiver of the CMS digital optical link", Proceedings of Fifth Workshop on Electronics for LHC Experiments, Smnowmasss, Colorado, September 20-24, 1999, p.189

[9] K.Kloukinas *et al*., "A system for timing distribution and control of front end electronics for the CMS tracker", *Proceedings of the Third Workshop on Electronics for LHC Experiments*, London, 22-26 September 1997, p.208

[10] Total Dose Steady-State Irradiation Test Method, ESA/SCC Basic Specifications No.22900, Draft Issue 5, July 1993