Electronic Design Automation tools for high-speed electronic systems

Evans, B.J.
Calvo Giraldo, E.
Motos Lopez, T.

CERN, 1211 Geneva 23, Switzerland
John.Evans@cern.ch
Eva.Calvo.Giraldo@cern.ch
Tomas.Motos-Lopez@cern.ch

Abstract

The LHC detectors will produce a large amount of data that will need to be transferred very quickly. The signal-speeds and interconnect-density involved lead to difficult electrical design problems, particularly regarding signal-integrity issues such as crosstalk and ground bounce.

Various commercial Electronic Design Automation programs are now available to address these problems. These include 3-D full-wave electromagnetic-field solvers, SPICE-based circuit simulators and printed circuit board signal-integrity point products. We will show how these tools can be used in a complementary fashion to provide detailed studies of detector-electronic design.

Two case studies will be presented from LHC related projects.

I. EDA TOOLS AT CERN

Simulation tools have become essential in today's design processes. CERN is typically involved with ever more complex circuitry working at increasingly higher frequencies. Relying on established empirical laws is no longer sufficient to guarantee a successful design without much time-consuming and costly iteration.

Well-established products such as SPICE type circuit-based simulators have now been joined by commercially available Electromagnetic Field Calculation tools.

CERN has available two families of these tools. One is a very general type of solver where the user has control over essentially all aspects of the problem definition. Almost any physically realisable object can be analysed and applications range from designing physics detectors to examining the effects of PCB vias. A mechanical description of the structure to be analysed is entered and all materials and boundary conditions defined.

After the electromagnetic behaviour of the structure has been analysed, the results are typically examined in the form of field lines, strengths and gradients. However, the results can also be used for export to other programs.

Examples include:

- Physics detector electric-field patterns have been estimated and then input to Garfield [1]. This allows accurate particle drift simulations to be performed.

- The equivalent SPICE model for a structure can be extracted. We have extensively used PSpice® during our studies allowing analyses in both the time- and frequency-domains.

- The user might have available a specialized radio-frequency circuit design program e.g. Serenade Design® or DesignStudio®. The equivalent S-parameters description of a structure can be directly exported from the EM simulators to these programs.

CERN also has installed tools that are specifically used for signal-integrity analysis of high-speed digital signals on printed circuit boards. Using simplified models, what-if analysis in the pre-layout phase is possible as well as highlighting likely signal integrity violations at the post-layout stage. These programs are fully integrated with the PCB design tools and all calculations automatically include effects due to track widths, dielectrics and board stackup. The PCB layout itself can be driven by a set of defined design constraint rules. This can help the board-layout expert who may have no specialist EM field theory knowledge.

CERN supports the SpecctraQuest® programs for use with our Cadence® PCB tools.

A. Electromagnetic Field calculation overview

All of these tools solve Maxwell's equations for different geometry and boundary conditions. The solution space has to be discretized into sufficiently small elements so as to formulate a set of algebraic equations that are the equivalent of the partial differential equations description.

The resulting equations can be solved in many different ways, depending on the assumptions made when finding the solution (static, quasi-static and full wave solvers); the algorithms used (Finite Differences, Finite Elements, Method of Moments, etc); or the solution domain (time or frequency).

Table 1 shows some of the tools used at CERN.

For static problems, there are no time-dependent variations. This leads to the decoupling of the equations and to the notion of electrostatic- or magnetostatic-only solvers. These tools are typically used at CERN to characterize detector structures used in the different experiments.

In the pseudo-static solvers, the displacement current is ignored. This leads to solutions where the magnetic and electric fields are coupled, but radiation effects are neglected. This approach is followed in the Maxwell® 2D and 3D Extractors and the solutions are generally considered valid if the physical dimensions are less than one-tenth of the solution wavelength. The main use of these tools at CERN is for high-speed electronics e.g. characterization of connectors or board stack-up analysis.

In the full wave solvers, the complete set of equations is solved. The electromagnetic behaviour of the system can be analysed without an upper frequency limit but at the cost of an increased level of complexity and computing resources. HFSS®, Microwave Studio® and LC® use this approach. At CERN, these programs are used mainly in the RF engineering community to design resonant cavities and accelerating structures. LC® can also be used for high-speed digital electronics.

Different types of problems are better solved in the frequency- or time-domains. Frequency-domain codes assume time harmonic signals, and thus solve the problem for a single frequency at a time. They use adaptive FEM methods to iteratively refine the mesh in order to concentrate computational effort in areas of rapidly changing fields. These programs excel at solving for structures with large resonant behaviours.

Time-domain codes make no *a priori* assumptions about the fields and are thus more general in their approach. Time codes can perform a broadband analysis of the structure as a simple impulse excitation can contain a great amount of frequencies. However, they can place a heavy load on the computing resources due to the need to produce a mesh fine enough to model the smallest detail in the structure. They also handle resonant structures rather awkwardly.

Table 1. Comparison of the EDA tools at CERN

	Frequency-domain	**Time-domain**
Static	Maxwell 2D/3D Field Simulator	
Pseudo-static	Maxwell 2D/3D Extractors	
Full wave	HFSS	MWS, LC

There are costs related to electromagnetic simulation. One is the need for computing resources that have to be sufficiently large so as to allow the simulation of complex structures. Another is time - the structures have to be drawn, the materials and boundary conditions have to be specified and possibly many iteration cycles followed in order to optimize the design.

It is also important to note that any simulation is only an approximation of the real structure behaviour. In some cases, these programs may give poor results or even may not be able to find a solution at all. This is especially true of highly resonant, lossy or low energy problems.

Note that SpecctraQuest® has not been included in Table 1. This was considered apart as it is a specialised turnkey tool where the user has no need to know how the simulator works. In fact, it consists of a frequency-domain EM solver that is fully integrated with a SPICE-type time-domain circuit simulator.

II. CASE STUDIES

We will now describe two examples of how these tools are being used at CERN.

A. Case Study 1. ALICE pixel backplane meshed structure.

The main goal of this project was to simulate a meshed power plane in order to evaluate its performance in the ALICE Pixel Bus detector.

The Pixel Detector chip sits above the Readout chip that communicates with the serialiser to extract the gathered information [2]. This communication is done via a GTL bus that will propagate signals using the power and ground planes as reference.

As the Pixel chip will be the closest to the beam, it is desirable that as many as possible undetected particles are allowed to pass freely towards the other detectors.

'Transparent' power planes would allow more particles to pass through to the outer stages of the detector. One way to increase this 'transparency' would be to use meshed power and ground planes (Figure 1). This study describes how we evaluated the behaviour of such planes in terms of signal propagation and power distribution.

The following effects were considered:

- *DC voltage drop*: the power planes are primarily responsible for maintaining the proper DC levels (VCC, GND) for the chips. If the power planes are very thin, or the mesh is too fine, the DC resistance of the plane becomes too high to allow proper device functioning.
- *Signal integrity*: the mesh has to guarantee sufficiently good signal transmission to the receiver for the required signal rise-times.
- *Ground bounce*: the extra inductance associated with a meshed power plane, added to the loading currents of the GTL bus, will create significant local fluctuations of the local ground plane. This plays an

important role in the overall system signal quality and has to be estimated.

In order to tackle the problem, several approaches were taken. First, a theoretical characterisation of a full power plane was performed. The DC resistance of an aluminium plane of dimensions l = 215 mm, W = 16.8 mm, thickness = 25 um was computed as 13.4 mΩ. We then included the bonding wire resistance at the end of the power plane. While relatively high (38 mΩ) for a single wire, the problem was alleviated as there were 6 ground (and power) wires connected in parallel. The final calculated voltage drop for a full plane drawing 3A current for the five circuits was calculated as 40 mV.

The next step was to estimate the highest possible resistance a meshed plane could have so that the total voltage drop did not exceed 200 mV at the last chip. Figure 1 shows how the meshed plane was defined with a pitch length (p) and a track width (w_o). In order to optimize this structure, it was entered into Maxwell® 3D Extractor and parametric simulations were used to find the limiting ratio between track-width and pitch satisfying the maximum voltage drop condition. From the simulations, it was found to be approximately 3.

$$p/w_o \approx 3.$$

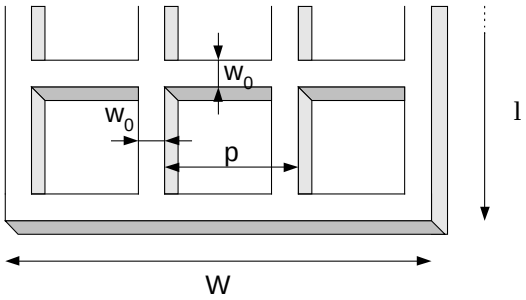


Figure 1: Layout of the meshed plane.

Once the structure complying with the first criterion (DC voltage drop) is found, it remains to be seen if the signal integrity can be maintained and for what signal edge- rates.

Using CST's Microwave Studio® and LC® from Cray Research, a time-domain simulation of the propagation of the signals was done. In order to test the worst possible condition, a track was placed at mid distance between the longitudinal traces. Two different signal rise-times were used and simulated (Figures 2 and 3). The results show the effects of very high-speed signals phenomena and how rise-time is the critical factor when determining signal integrity.

It is apparent that not all of the signal energy passes through the meshed plane. It is also clear that some resonant frequencies are excited when the rise-time is fast enough. A complete animation of current density in the ground planes has also been simulated [3].

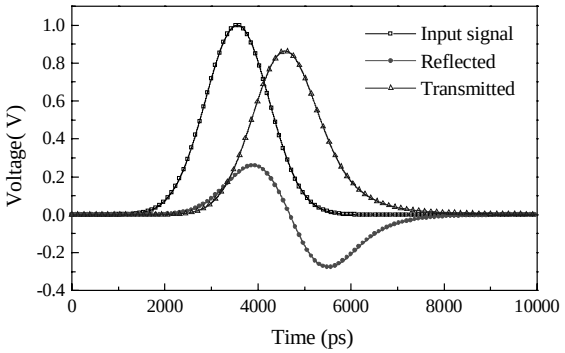


Figure 2: 1ns rise-time input signal.

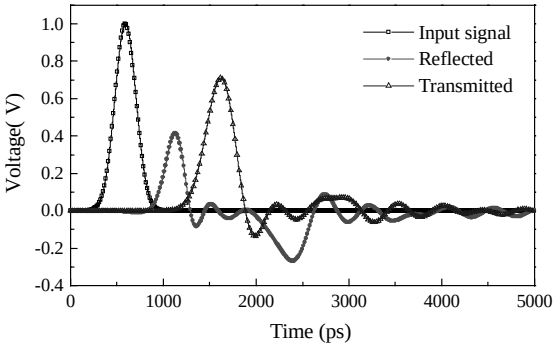


Figure 3: 200 ps rise-time input signal.

The main conclusion that can be drawn from these simulations is that in order to have a proper energy transmission in a similar system, (basically a low pass filter with some resonances), we have to limit the bandwidth of the signal to that of the structure pass-band. This implies that the most important parameter in the design will be the rise-time of the digital signals.

Given such a band-limited input signal, we have shown that this p/w_o ratio could satisfy the DC voltage-drop and signal-integrity requirements. We then evaluated how the meshed power-plane inductance can influence ground-bounce system behaviour and what parameters can be used to control it. Maxwell® 3D Extractor was again used to estimate the power plane inductance (3.4 nH). This was summed with the bonding wire contribution to give a total inductance of approximately 6 nH per signal pin. A system with GTL outputs and GTL loads was simulated in PSpice® for different rise-times.

The amplitude of the ground bounce was evaluated for different rise-times and for the worst-case condition of four simultaneously switching signals. (Table 2).

Table 2: Ground bounce versus rise-times

t_r (ns)	1	2	3	5	10
Vg (mV)	503	309	202	107	43

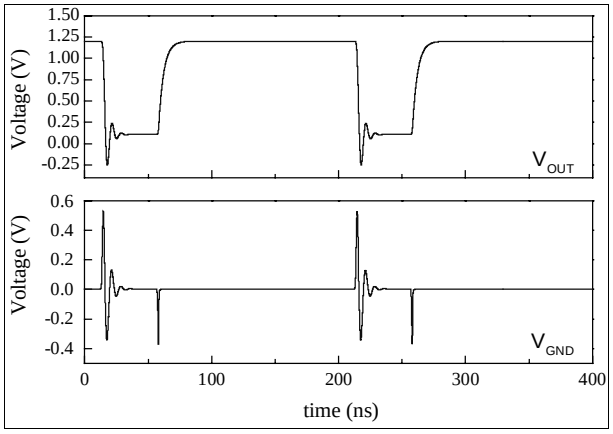


Figure 4: Ground bounce for 1ns rise-time input signal.

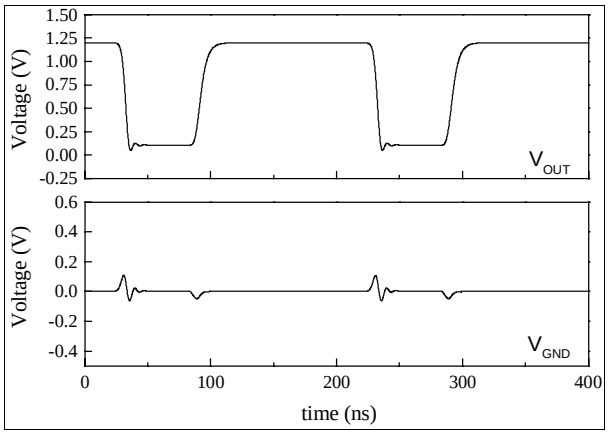


Figure 5. Ground bounce for a 5ns rise-time input signal.

The waveform results are shown in figures 4 and 5.

We can conclude from this study that a meshed aluminium ground plane is feasible for the ALICE Pixel bus but only if care is taken to limit the p/w_o mesh ratio and the signal edge-rates. Under these conditions, proper DC distribution levels will be ensured, crosstalk levels can be insignificant, signal-integrity will be maintained and ground bounce kept to acceptable levels.

B. Case Study 2. Altera® FLEX 10KE digital signal-integrity analysis

The SpecctraQuest® tools from Cadence® can be used to examine PCB layouts for possible signal-integrity problems. What the designer considers as critical paths can be highlighted and closely scrutinized. There are two possible methodologies: pre- and post-layout analysis.

Pre-layout analysis can be used to perform a what-if study of a topology to identify and correct signal-integrity problems [4].

Post-layout analysis can be used to improve PCB layout before manufacture or to debug boards having problems in the field. Figure 6 shows part of the initial PCB layout for a circuit designed at CERN [5]. This uses a fast (500ps rise-time) FPGA and so is very typical of a

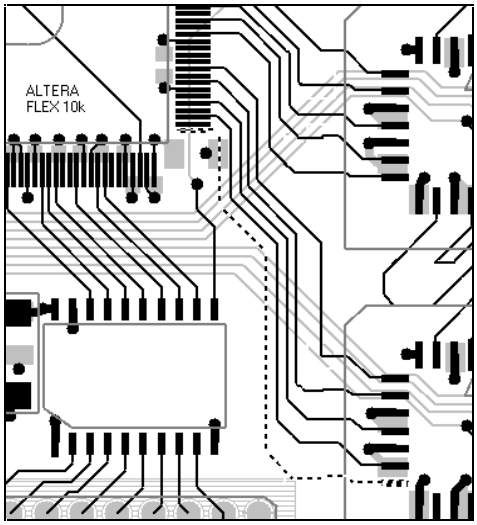


Figure 6: Track with suspected signal-integrity problem

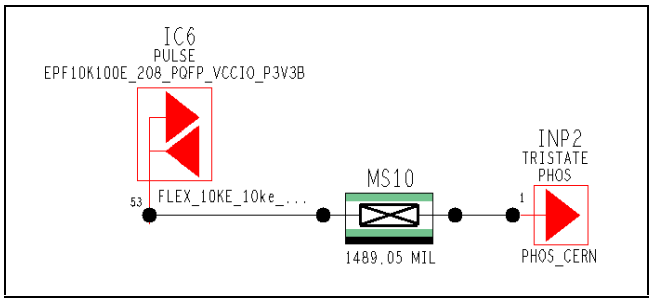


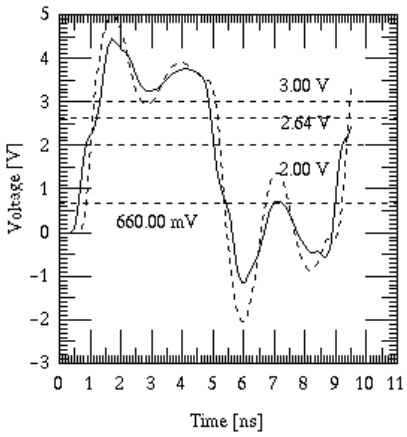
Figure 7: SpecctraQuest® output (extracted from PCB and with added IBIS models).

circuit that could exhibit signal-integrity problems. We will now describe the procedure followed to investigate one driver-receiver link (dotted trace, Figure 6).

SpecctraQuest® was used to extract the equivalent circuit for this trace (Figure 7). The program uses the PCB layout as input and automatically takes into account the previously defined board stackup and geometrical track sizes. The I/O devices were then attributed with IBIS signal-integrity models [6]. These are extensively utilized for signal-integrity analyses and use behavioural descriptions to characterize input and output cells in terms of V-I and V-t curves. They are often freely available from the chip manufacturer.

Next, it was necessary to define the simulation set-up. There are several options possible but here we are interested only in the reflections between the driver and receiver. Figure 8 shows the simulated signals at both pins. Note that even with such a short track, the high degree of ringing leads to a negative noise-margin – this is due to the very fast FPGA output edge-rates.

The designer now has the powerful option of doing a what-if analysis on the extracted circuit without immediately having to modify the PCB and recalculate the equivalent circuit. Analysing the effects of adding a "virtual" series termination resistor to the signal track



—— driver end - - - - receiver end

Figure 8: Waveforms for original PCB layout

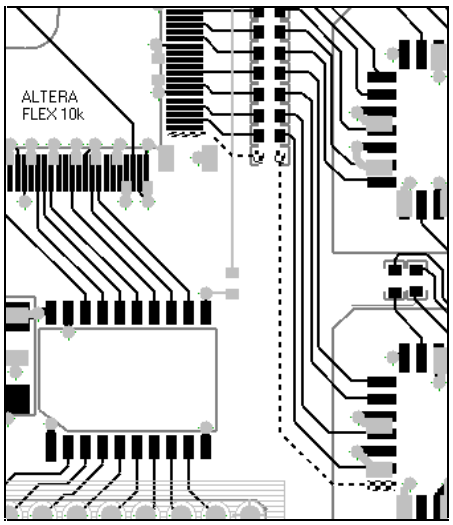


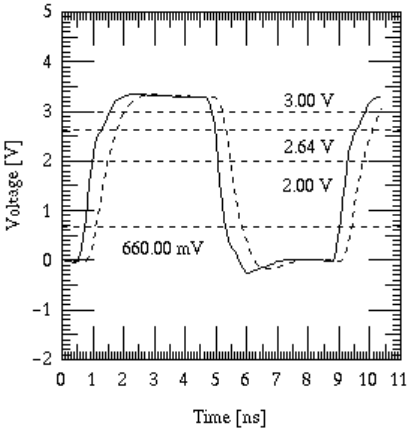
Figure 9: Modified PCB with series resistors

gave results that much reduced the ringing. This modification was implemented on the PCB (Figure 9) and the equivalent circuit was again extracted from the modified layout and simulated (Figure 10). The results confirmed the expected improvement due to the added resistor – under-shoot and over-shoot have practically disappeared and there is now no noise-margin violation.

III. CONCLUSIONS

Simulation is essential in today's design process. Different EDA tools for electromagnetic design and signal-integrity can be used to help to design high-end systems. We have shown two practical case studies and illustrated how these programs can help to avoid costly hardware modifications.

The tools described in this paper are available and fully supported at CERN by IT/CE-AE [7] [8].



—— driver end - - - - receiver end

Figure 10: Waveforms for modified PCB layout

IV. ACKNOWLEDGEMENTS

The ALICE pixel backplane example is based on input from EP/ED.

P. Fraboulet, V. Rossi and J-M. Sainson made invaluable contributions to the second case study.

The authors wish to thank Rudi Zurbuchen for his support and encouragement for this work.

V. REFERENCES

[1] Information on Garfield
http://consult.cern.ch/writeup/garfield/

[2] M. Burns, "The ALICE Silicon Pixel Detector Readout System", this workshop

[3] Meshed Plane Current Density Animation
http://wwwinfo.cern.ch/ce/ae/Maxwell/apps/crossing/crossing.html

[4] SpecctraQuest® pre-layout analysis example
http://wwwinfo.cern.ch/ce/ae/SpecctraQ/PDF/training/demo1to7.pdf

[5] V. Rossi, CERN, SL Division, SPS10213 "Digital notch filter & delay for the SPS/LHC transverse feedback/damper"

[6] IBIS Home page
http://www.eigroup.org/IBIS/Default.htm

[7] Maxwell® and HFSS® at CERN
http://wwwinfo.cern.ch/ce/ae/Maxwell/Maxwell.html

[8] SpecctraQuest® simulator at CERN
http://wwwinfo.cern.ch/ce/ae/SpecctraQ/SpecctraQ.html