HAMAC, a rad-hard high dynamic range analog memory for ATLAS calorimetry.

Dominique Breton, Vanessa Tocut

LABORATOIRE DE L'ACCELERATEUR LINEAIRE, IN2P3-CNRS et Université Paris-Sud, 91405 Orsay Cedex, France.

Eric Delagnes, Pierre Borgeaud

CEA, DSM/DAPNIA SACLAY, 91191 Gif-sur-Yvette, France.

John Parsons, William Sippach

NEVIS LABORATORIES, COLUMBIA UNIVERSITY, Irvington, NY 10533, USA

ABSTRACT

A 12 channel analog memory dedicated to the readout of the Atlas liquid argon calorimeter has been developed. Its main function is to sample, at a 40MHz rate, the data coming from a three gain shaper, to store it, waiting for the level-1 trigger decision, and then to send it more slowly (5MHz) towards a 12 bit ADC. For each trigger, the ADC will digitize 5 samples. As the system is supposed to present minimum dead time, the write operations will be unceasing even during the read phases. The chip can thus be seen as a simultaneous double random access analog memory array. The read and write addresses are generated by a separate controller chip and sent together with other control signals to the analog memory using low-voltage swings.

In the ATLAS calorimetry, the electronics will have to withstand a non negligible ionising dose over the 10 year lifetime. Thus the chip has been developed in DMILL technology.

The presentation will highlight the amazing level of performance achieved by this circuit whose dynamic range is in excess of 13 bits even while performing simultaneous write and read accesses.

1. REQUIREMENTS

The basic requirements for the whole liquid argon calorimeter readout system are the following :

- amplify and shape the signal coming from the detector with an optimisation of the signal relative to both electronics and pile-up noise ratios.
- sample the signals at 40MHz after shaping.
- store data during the level 1 trigger latency (~ 2.5us).
- read 5 samples per event accepted by level 1 trigger (the maximum rate should be 75 kHz and could raise up to 100 kHz) and perform the analog to digital conversion.
- format and transmit the data to DSP boards ("ROD") which will provide on the fly feature and energy extractions before sending data to the level 2 event buffers.
- operate fully simultaneous write and read operations and deal with interleaved events.
- cover a dynamic range of 16 bits without degrading the calorimeter resolution (0.7% for the biggest signals).
- feed the level 1 trigger system with analog sums of the input signals.

The total number of channels to be equipped is very high (200,000) and the electronics has to fit in a limited volume with stringent constraints on power dissipation and accessibility. Furthermore, the radiation level to deal with is at the level of 50kRads for photons and 2 E13 N/cm2 for neutrons, including the ATLAS standard safety margin for calorimeter electronics.

2. SYSTEM DESIGN

The idea to design a 128 channel board raised at the end of 1996. To fit the described above requirements, we chose the following solutions (Fig. 1) :

- the signal shape is bipolar with a rise time of 40ns what optimises both pile-up and electronics noise.
- the detector signals dynamic range of 16 bits going out of the preamplifiers is divided in three linear ranges of 12 bits. This operation, performed by tri-gain shapers (gains of 1,

10, 100), allows to split the dynamic range without degrading the intrinsic detector resolution (~7 bits).

- the signal coming out of the shapers is sent to analog memories. Inside each memory, the signal is sampled at 40MHz and stored until a level 1 trigger is received.

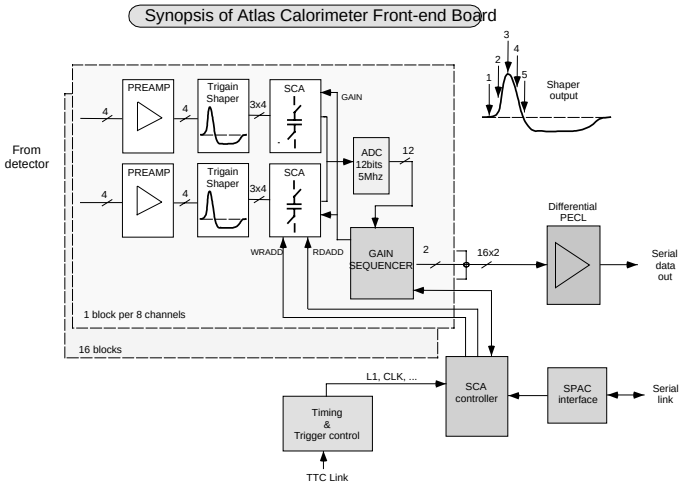

Fig. 1 : block diagram of the *Front-end board*

- then only the interesting data is converted by the ADC (1% of the total input rate) with all samples on the same gain and sent serially to the output drivers. Thus the number of ADCs and their speed are both divided by a factor 8.

One of the main difficulties to deal with is of course the digital to analog potential crosstalk.

3. FRONT-END BOARD SPECIFICATIONS

This board treats the 128 channels coming from the detector in 16 groups of 8 channels. Each block includes :

- 2 four channel preamps.
- 2 four channel shapers.
- 2 twelve channel analog memories or SCA (Switched Capacitor Arrays).
- 1 12bit / 5MHz ADC.

There are also a lot of digital components to ensure all the functionnalities :

- 8 Gain Selector Asics for gain selection and output data formatting (each for 16 channels).
- 2 SCA controller Asics (each for 64 channels) which provide write and read addresses to the SCA and the synchronization for all the read operations.
- a summation block for the first step of level 1 trigger analog sums.
- the TTC interface for the fast signals (CLK, L1, …).
- the interface for the fast serial link (SPAC) [ref 9] which allows the downloading of all electronics sited on the detector.

The way the system chooses the right gain is the following : after reception of a L1 trigger, the SCA controller sends the address of the peak sample (3) to all the SCAs. The gain sequencer chooses the medium gain for performing the comparison. Thus for each channel, the peak sample on the medium gain is compared both to saturation and to a low threshold. Depending on the result of the comparison, the right gain (high if small signal, low if large signal, medium if intermediate) is chosen and stored. Then the peak sample is read once again on the chosen gain, and sent to the ADC. Finally all the four other samples are also read on the same gain. The total time needed for reading a group of 8 channels is thus 9us.

Event output data is formatted in a 47 word block and sent serially on two lines (one for each byte) towards the ROD board.

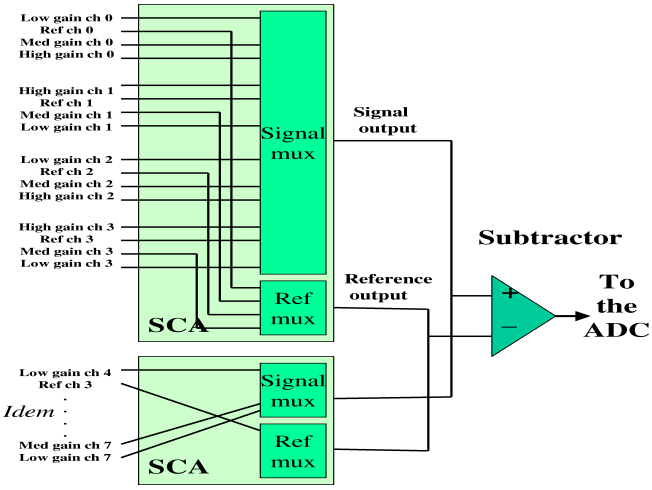

Fig. 2 : output cabling for 8 SCA channels

On the *Front-end board*, a special care has been taken to avoid as much as possible the crosstalk between the digital part running either at 40 or at 5MHz and the analog signals. This implied the use of common ground planes covering the complete board, special routing of critical signals, and high care of the numerous power supplies. Moreover, the most perturbative digital lines are transmitted in differential PECL or LVDS.

4. ANALOG MEMORY SPECIFICATIONS

After years of development in standard AMS and HP technologies, the latest version of the analog memory used on the *Front-end board* has been developed in the DMILL 0.8um rad-hard technology [ref 6, 7]. Tab. 1 summarizes the main features of the chip.

The memory consists in a switched capacitor array where the analog signal is sampled, stored, and read as a voltage. This allows to be independent of the dispersion of the cell capacitor values. Its global architecture is given on Fig. 3.

Nb of channels	12 + 4 references
Nb of cells per channel	144
Storage capacitor value	1pF
Sampling frequency	40MHz
Input bandwidth	50MHz
Output multiplexing rate	5MHz
Power supply voltages	-1.7V/+3.3V
Power consumption	300mW
Chip size	30mm2
Nb of transistors	25000
Package	PQFP 100

Tab. 1 : main features of SCA chip.

The chip contains 16 analog channels. 12 of them are used to store the signal coming out from the shaper. The remaining 4, equally spaced in the chip (Fig. 2), store a reference level. During the read-out operation, an off-chip amplifier subtracts the closest reference channel to each signal channel. This pseudo-differential mode offers a common mode noise rejection ratio improvement higher than a factor 4 when the chip is used in simultaneous read and write operation.

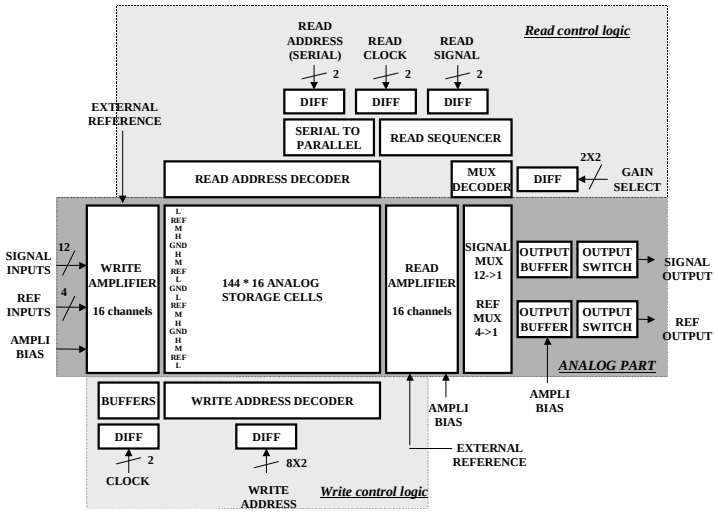

Fig. 3 : analog memory architecture.

Each of the 16 channels (Fig. 4) consists in 2 write amplifiers, 128 storage cells, and a read-out amplifier

The write buffer is an O.T.A. type amplifier with enhanced slew-rate capabilities (Fig. 5) used as a voltage follower. The same structure with different transistors sizes is used for all the other amplifiers of the chip. The purpose of the write amplifier is to present a constant high impedance to the shaper output and to avoid signal distortion caused by high dI/dt in the bonding wires. Its characteristics are the following :

- 50Mhz Gain-Bandwidth product in order to minimize the contribution of the write amplifier to the filtering.

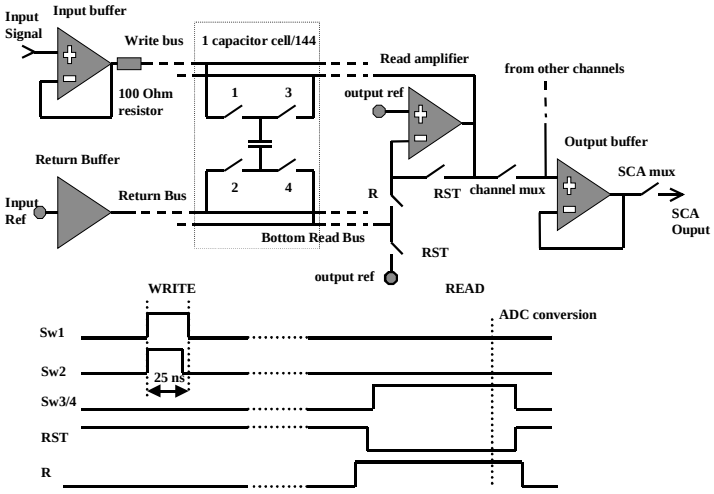

Fig. 4: channel block diagram

- Very good unity-gain stability, to avoid any signal distortion.
- Less than 0.2% integral non linearity on a 4V range with (VDD-VSS) =5V.
- 170 V/us slew-rate to limit distortion for high energy pulses.
- Low noise (80uV rms in a 100Mhz bandwidth).
- Very low power consumption (6 mW).

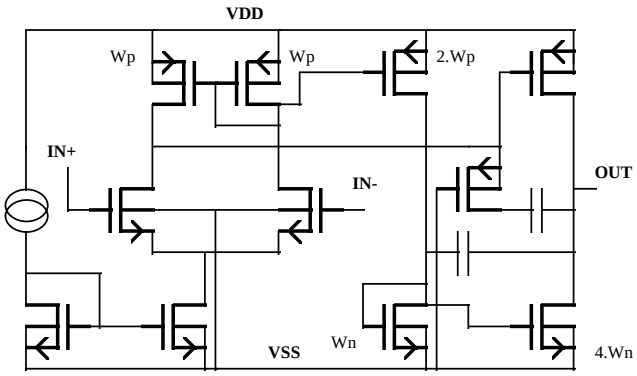

Fig. 5: pipeline amplifier schematics.

At each leading edge of the 40MHz clock, the write address is decoded and one of the 128 write columns is enabled and starts the following actions (see Fig. 4) :

- The S1 and S2 switches connect the capacitor between the output of the write amplifier and the return line during one clock cycle.

- The S1 switch is turned off one nanosecond before S2, so that the injected charge and sampling time are made independent of the input voltage. As S1 is a minimum size switch, the value and the cell-to-cell spreading of the injected charge are kept small. A special care has been taken in the layout of the clock and signal distribution to limit both the sampling time jitter and the cell-to-cell sampling time skew.

Before each read-out operation, a residual charge due to the non infinite open loop gain of the read amplifier is stored on the parasitic capacitor Cb of the 'bottom' read bus. So, when a read address is selected, this bus is immediately reset (RST closed, R opened on Fig. 4). The bottom RST switch must be quite big to allow a fast reset time. Its high injected charge during its turn-off is compensated by the correct sizing of R. This new reset operation presents important advantages compared to the conventional one [ref 4] :

- There is no risk of oscillations during reset.
- The noise sampled on Cb during the reset is low (only kT/Cb due to RST), compared to the noise of the read-out amplifier in a classical reset.

After this operation, S3 and S4 switches are turned on, connecting the storage capacitor across the read amplifier. Then the 12 channels are sequentially multiplexed toward the 2 output buffers at the rate of 5Mhz. All the digital inputs use differential PECL levels. To limit on-chip D/A couplings, digital and analog parts are separated by guard rings and have different power supplies. The switches command busses may be vectors of digital to analog pollution, via parasitic capacitors with analog busses or via couplings through the analog switches themselves. Thus to keep these signals noiseless, a extra set of power supplies is provided especially for the command buffers.

5. SCA PERFORMANCES

The performances summarized on Tab. 2 have been measured on the SCA dedicated test bench working in a simultaneous 40MHz write/read operation, and with the ADC continuously running at 5MHz. Fig. 6 gives an idea of the noise performances (pedestal run on 100 events).

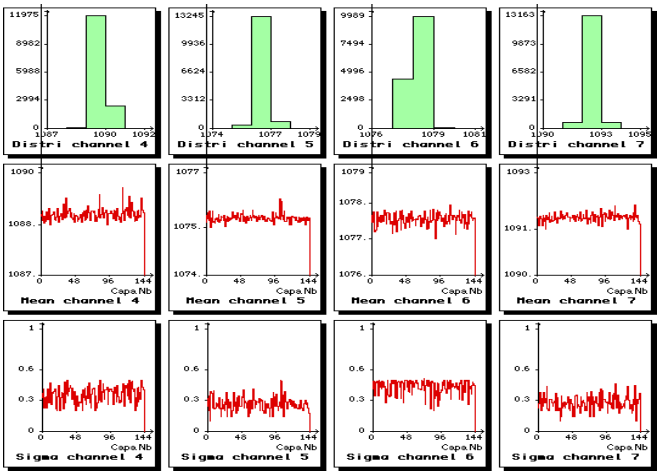

Fig. 6 : fixed sequence and noise distributions.

The performances of the chips are indeed impressive, for instance a dynamic range in excess of 13 bits and a better than 50ps time resolution.

Min DC signal	-0.95V
Max DC signal	+2.85V
Noise	300uV RMS
Fixed sequence noise	200uV RMS
Dynamic range	13.3 bits
DC gain	0.995
Cell-to-cell gain dispersion	<0.02% peak-peak
Channel to channel offset dispersion	10mV RMS
Cell leakage drift	<3mV/ms
Max DC input signal	5V

Tab 2. : DC performances of the SCA chip.

The fixed sequence noise is the fixed part of the noise. There are two major contributions to it :
- the dispersion of the switch charge injection along the cells,
- the position of the write pointer, but also other signals that could have the same state every time you sample the signal on a given capacitor.

Nevertheless, this part of the noise remains very small (typically 0.2mV), thanks to the optimized structure, and only has to be added in quadrature to other sources.

Max shaper signal	-0.8V -> +2.7V
INL @ peak (shaper signal)	<0.1%
Sampling jitter	<45ps RMS
Cell-to-cell sampling time dispersion	1.1ps/cell
Total sampling time dispersion	150ps peak-peak
Cell-to-cell peak value dispersion	0.05% peak-peak
Input bandwidth	50MHz
Input slew rate	170V/us

Tab 3. : transient performances of the SCA chip.

The measured crosstalks are very small, thanks to the absence of current flowing within the input bounding wires, and to the order chosen for the input pinout (see Fig. 2 and 3) . The so called "DC crosstalk" is due to the fast settling of a sampled signal on the top read bus during readout.

DC channel to channel crosstalk	<1/10000
5MHz multiplexing residue	=1/10000
Transient crosstalk	
Medium to high	1/4000
High to medium	1/4000
Others	<1/10000

Tab 4. : crosstalk performances of the SCA chip.

The chip has been irradiated both under gammas and neutrons (300kRads for gammas, 4.5 E13 N/cm2 eq 1MeV for neutrons), which is far above the standard ATLAS official levels for the calorimeter electronics. No measurable change was observed after both types of

irradiation. Moreover, the effects of the SEUs are negligible as the SCA doesn't include any static register.

The yield of the successive runs was rather irregular, with peaks at 90% and major difficulties during the last year. There was indeed a problem of cell capacitor leakage in the run of fall 1999, leading to a yield of only 10%, but the problem was fixed (polysilicon filaments within the trench oxyde), and the yield went back to 65%.

6. PRODUCTION TEST SETUP

50000 operational chips have to be mounted on the front-end boards. Thus we'll have to produce and test around 100000 of them. A dedicated fully automatic test setup is being developed for this purpose. Fig. 7 shows a diagram of this system. A computer driven robot tests and sorts the chips, with the help of a software running of a Power Macintosh. The time goal is less than 30s per chip, which however leads to close to one year of intensive tests. This setup takes advantage of the 10Mbit/s serial bus (SPAC) designed by the LAL for getting a fast block mode access to the test board data.

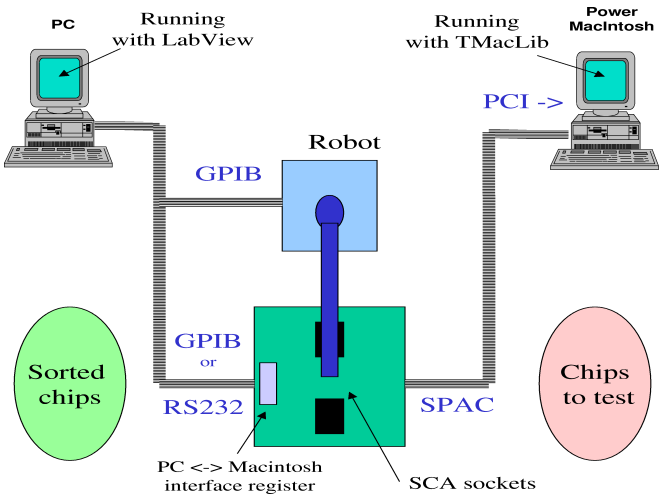

Fig. 7 : production test bench setup

All the types of measurements will be performed, including noise, dynamic range, channel offset dispersion, leakage currents, and scan of all the individual cells with very short transient signal. The latter allows to ensure the complete functionnality of the circuit.

Before the full production, this test bench will be used for the pre-production run in the spring of 2001 (~ 2000 circuits). This will allow to calculate all the thresholds needed for the production tests, and to get a good idea of the yield distributions. Most of those chip will be mounted on the prototypes of the final front-end boards during the summer of 2001.

7. CONCLUSION

We have been working on analog memories developments since 1992. After having worked with AMS and HP standard technologies, we switched to DMILL to follow the radiation requirements due to the location of our electronics on the ATLAS detector. Despite this technology change, we were able to keep the huge dynamic range and time precision already achieved. Moreover, our knowledge of SCAs now allows us to envisage other applications at much higher sampling speed and signal bandwidth.

The next major steps of the work are the pre-production run, which should occur in October 2000, and the full production at the end of 2001.

Those chips will also be used for the front-end electronics of the CSC muon chambers of ATLAS.

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