Implementation of the ASDBLR and DTMROC ASICS for the ATLAS TRT in DMILL Technology.

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Abstract

The ASDBLR and DTMROC chipset provide detector mounted signal processing, time digitization, pipelining and data sparsification for the ATLAS TRT (tracking and transition radiation) detector subsystem. Due to high levels of radiation in the detector environment, the radiation hardened DMILL BiCMOS technology was chosen for fabrication. A multi-institutional effort that included significant analog and digital simulation led to the fabrication of two highly successful designs in the fall of 1999. Test beam measurements utilizing these ASIC's to readout detector prototypes indicate that the chipset is capable of meeting the design requirements of the TRT.

I. THE ATLAS TRT STRAW TUBE DETECTOR

The ATLAS Transition Radiation Tracker, TRT, will be comprised of 424,000 straw sensors, with 4mm diameter and a maximum length of 80cm. The straw tubes will use a $70\%Xe+20\%CF_4+10\%CO_2$ gas mixture to allow prompt collection of the primary electrons and efficient conversion of the higher energy Transition Radiation, TR, photons. They will operate in the proportional region with an avalanche gain of $2X10^4$. The cathode (straw tube) will operate at negative high voltage and wire anode will directly connected to the input of the readout electronics. Table 1 lists the objectives expected for the ATLAS TRT detector mounted electronics.

The straw signal is characterized by a fast initial current pulse due to avalanche electrons attaching to the wire, followed by a decaying current that lasts until the positive ions created in the avalanche process contact the walls of the straw, about 50μs later. The signal shape and amplitude vary according to particle type, interaction mechanism and trajectory. A charged particle will lose about 2keV in passing through the straw resulting in a signal of about 20fC , but thresholds as small as 2fC will be required to efficiently trigger on the avalanche signal from the earliest clusters. On the opposite end of the scale, neutron interactions or charged particles with axial trajectories can result in signals as large as several picocoulombs. At full luminosity we expect a trigger rate of up to 20MHz in some straw tubes so an important objective of the signal processing electronics is to remove the long ion tail with high accuracy over a large dynamic range. In an ideal high rate readout, only the first few nanoseconds of signal are required to characterize point like energy depositions such as gamma conversions. Track depositions with extended primary ionization trails behave as superimposed point ionizations so that the width of the detection pulse may be as short as the sum of the point ionisation response plus the time it takes to sweep out all the primary electrons in the sensor.

For the TRT we find that an electronics peaking time of 7ns offers an ideal trade-off signal to noise position resolution and high rate performance. The point of closest approach to the wire of a charged particle track can be determined to high accuracy by recording the leading edge time with respect to the beam crossing time. Our target position resolution of 150μm can easily be achieved with 1ns timing resolution.

Layers of polypropylene foils and fibers placed between the straws form a transition radiation material. When energetic electrons pass through this material TR photons with a typical energy of about 6KeV are produced. Xenon in the straw gas mixture is used to efficiently absorb these photons converting them to primary drift electrons in the gas. Excellent differentiation between track depositions and TR photons is possible if the signal in the straw is integrated for about 10ns, long enough to collect the direct and reflected signal from the wire.

The ATLAS Level 1 trigger is a detector wide primary filter for reducing the raw data acquisition rate. It's maximum rate is 75KHz and minimum latency is 3μs. The TRT, detector mounted electronics will provide Level 1 sparsification of data from the detector with the ability to examine data from several beam crossings.

In the ATLAS environment, radiation is a significant factor in the design of detector mounted electronics. The tolerance required to operate for 10 years is 10^{14} neutrons per square centimer and 1.5Mrad ionizing radiation, well beyond the capabilities of most present day commercial electronics. Due to the relatively high radiation levels, Single Event Upset, SEU, is a potential problem as well as long term damage. This effect is caused when ionising radiation traverses the active electronics region of integrated circuits, disrupting the logic levels. Since no part of the circuit is immune, data and control functions are equally susceptible.

Table 1. Objectives for the ATLAS TRT readout electronics

Maximum Straw Trigger Rate	20MHz
Desired Position Resolution	150μm
Range of interest for signal	1fC – 120fC in 7.5ns
Desired Double Pulse Resolution	25ns
Level 1 Trigger Readout Rate	75KHz
10 yr. Integrated radiation Levels	~10^{14} N and 1.5Mrad

The ASDBLR and DTMROC application ASIC's have been designed to provide all signal processing, time encoding and

level 1 data sparsification functions for the ATLAS TRT. These devices were fabricated in the radiation hardened DMILL process in the fall of 1999. Both chips were fully functional and have been tested both individually and together in a high density readout. Test beam studies in the summer of 2000 showed that the combined chipset meets or exceeds all basic design goals.

II. The DMILL ASDBLR ASIC

The ASDBLR requires 36mW per channel and provides the complete signal processing chain for eight straw tubes. Figure 1 shows the block diagram for a single channel. The low noise dual preamp provides a DC balanced signal to the shaper stage with a gain 1.5mV/fC and peaking time of 1.5ns for an impulse input. Dual inputs provide common mode pickup rejection both on and off chip. The straw anode is attached to one of the inputs resulting in a single active signal and reference input to the shaper.

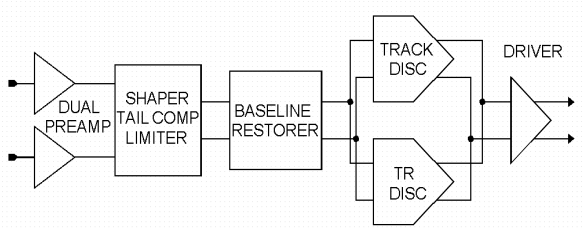

Figure 1: Block Diagram of the ASDBLR

The shaper block is comprised of three fully differential stages, each of which provides a 1.5ns integration along with other stage specific functions. Taken with the preamp, the shaper stage provides four equivalent 1.5ns poles of shaping to produce a symmetric output pulse with ~5ns peaking time for a straw point ionisation input. Stage specific functions are as follows: The first stage converts the dual preamp output to a differential signal with a gain of two. The second shaping stage includes ion tail cancellation for either Xenon or more conventional Argon based gases, selected externally. A full scale range of 600fC with soft limiting is maintained through this stage that the tail cancellation can be effective over a the widest feasible range of charge depositions. The final shaping stage cancels the short tail added by feedback components in the preamp and limits maximum output response the shaper at an effective input charge level of 120fC, the largest expected threshold setting the TR discriminator.

The baseline restorer, BLR, acts as an output controlled dynamic impedance C-R pass element. The differential signal from the shaper is coupled directly to two 8pF capacitors from input to the output buffers of the BLR. A bridge diode network with dynamic current control is used as a variable impedance between the differential outputs. Current in the bridge determines the dynamic impedance and is dependent on the polarity of the output. At baseline the time constant is ~4ns. The time constant increases as signals of the desired polarity are passed on to the discriminator, and when the shaper output returns to baseline, any overshoot due to discharge of the coupling capacitors is quickly eliminated by an increase in current in the bridge, lowering its impedance.

The Track discriminator adds 2.5ns to the peaking time in the first stage and can register signals between 1 and 10fC. The TR discriminator utilises the same basic configuration, but has a 10:1 attenuation at its input and adds 5ns to the shaping time to allow integration of the prompt and reflected wire chamber signal for accurate detection of the TR photons.

The Track and TR discriminators switch separate 200μA current sources between shared differential outputs to form a current sum of the combined discriminator outputs. This ternary encoding scheme is based on the assumption that the Track discriminator output is always present when the TR discriminator is triggered due to its lower threshold.

The DMILL implementation of the ASDBLR has been exposed to 10^{14} neutrons/square centimeter and 10^{14} protons/square centimeter, in the later case under power, and no substantial performance shifts have been observed.

Testbeam studies with the TRT prototypes at CERN have shown (See Figure 2) that this version of the ASDBLR is offers performance that closely matches that of a carefully tuned discrete component design with similar properties.

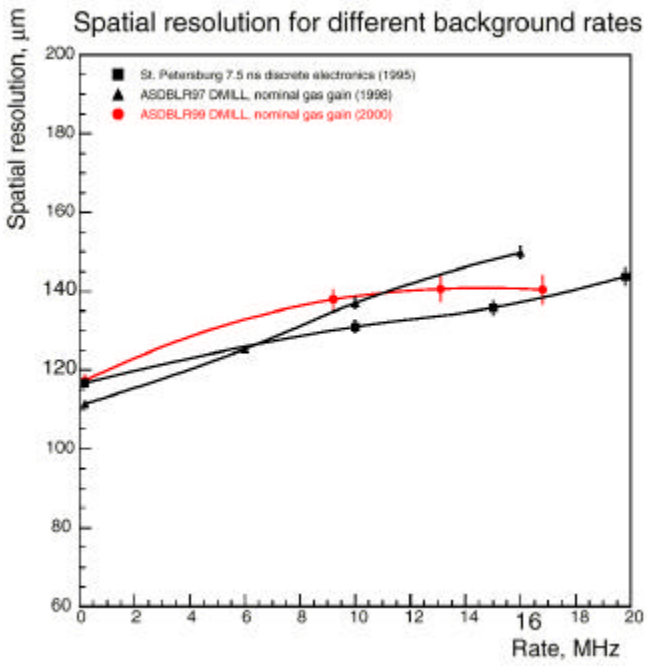

Figure 2: Summer 2000 test beam rate studies compared with discrete readout electronics and the 1997 ASDBLR prototype.

The most important remaining issue for the development of the ASDBLR is the parametric yield. Although the functional yield, defined as all channels working, is high, 88%, when the design objectives for channel to channel threshold offsets are applied, the acceptable yield is reduced to ~40%. Investigations have located two design sensitivities in the Track discriminator: an attenuation network unnecessarily referenced to analog ground that may cause offsets due to current flowing from the BLR buffer stage to

ground and a larger than expected mismatch between the DMILL NPN devices. These issues are being addressed in a design revision to be submitted in the Fall of 2000.

III. THE DMILL DTMROC

The main functional blocks of the Digital Time Measurement and Read Out Controller, DTMROC, are shown in Figure 3. A multi-institutional design team was utilized to meet the complex functional design requirements of this mixed analog and digital ASIC within the short time frame available for it's development.[1]

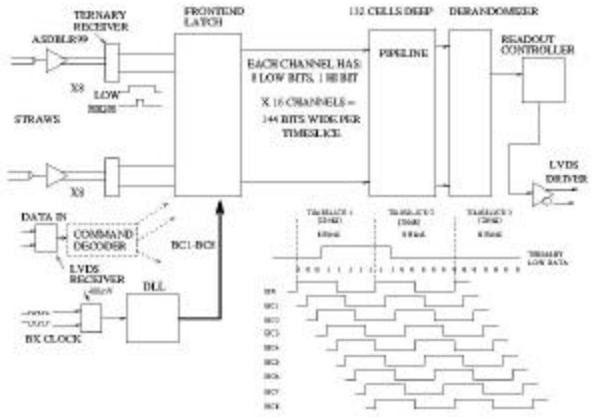

Figure 3: Functional Blocks of the DMILL DTMROC

The DTMROC interfaces to two eight channel ASDBLRs, time encodes their ternary outputs, stores the data in a pipeline and supplies Level 1 sparsified data to the Read Out Driver, ROD, located off detector. It uses the ATLAS 40MHz system clock (synchronous with the LHC beam crossings) supplied as an LVDS level signal for time reference markers for the DELAY LOCKED LOOP, DLL, and system clock for the rest of the chip. ATLAS Level 1 trigger and chip control information is serialized by the ROD onto a differential pair and sent as an LVDS level signal to the DTMROC. After being translated to a CMOS level by the LVDS receiver, the COMMAND DECODER checks the bit stream for the presence of a Level 1 trigger command then looks for commands for various resets, testpulse generation and data to load into the DTMROC registers. Level 1 sparsified data from the readout controller is serialized and sent over a dedicated line to the ROD by a dedicated LOW LEVEL DRIVER.

A specially designed TERNARY RECEIVER with low impedance inputs interprets the current step outputs from the ASDBLR companion chips separating out the Track and TR discriminator levels. Track discriminator level information for each of the 16 channels is digitized in 8, 3.1ns time bins for each 25ns beam crossing. A one bit indication of the state of the TR discriminator output is added to make a 9 bit word that is latched for each beam crossing and stored in the 144 bit wide PIPELINE. The 3.1ns time bins are derived from the ATLAS 40MHz system clock using an on-board DLL that generates eight 40MHz clocks with equally phased delays.

The PIPELINE is clocked by the ATLAS system clock and has 132 locations to match a 3.3μs latency of the Level 1 trigger. On reception of a Level 1 trigger three 25ns intervals of data are latched into the 13 event DERANDOMIZER. Data are readout of the DERANDOMIZER and serialized by the READOUT CONTROLLER then driven off chip by the LOW LEVEL DRIVER at the 40MHz system clock rate.

The DTMROC provides four 8-bit DACs for the remote programming of the two Track and TR discriminator thresholds on the ASDBLR chips. Two shaped, test-pulse outputs are provided for calibrating and commissioning of the detector. The amplitude and delay of these test pulses are programmable. An on-board band-gap voltage reference provides for the DAC reference currents.

The DTMROC was fabricated in the DMILL process in the Fall of 1999. The chip is fully functional and works well above the system clock rate of 40MHz even after exposure to high levels of ionizing radiation see Figure 4. The power dissipation is 37mW per channel when clocked at 40MHz.

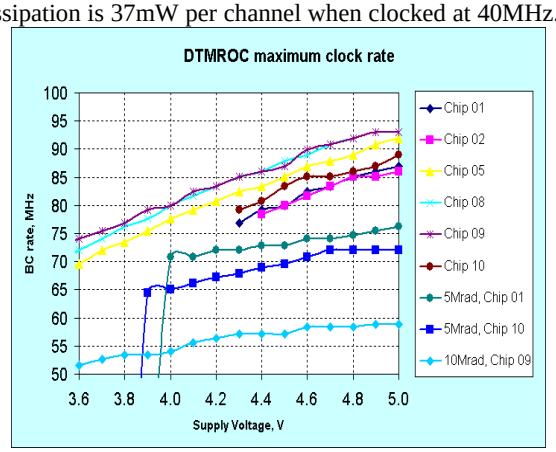

Figure 4: Tests of the DTMROC maximum clocking rate

The yield at about 40% is somewhat lower than expected and at this point no one critical element has been identified as having a significant yield problem. While not strictly a yield issue, the four 8 bit threshold DACs on chip vary unexpectedly by as much as 20% and an effort is being made to understand why.

IV. TESTBEAM STUDIES ON A TRT PROTOTYE

The compatibility of the ASDBLR and DTMROC has been successfully demonstrated on a 64 channel prototype readout board used for studies of the TRT sector prototype in the CERN test beam. With little effort and no serious deficiencies a track position resolution of 135μm was achieved.

[1] The following organizations and institutions were involved in the design and testing of this chip: CERN, Manhattan Routing Inc. (MRI), and the Universities of Kracow, Geneva, Lund, Michigan, and Pennsylvania.