Design of a comparator in a 0.25µm CMOS technology.

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Abstract

A comparator for the LHCb readout chip, the Beetle, has been designed in a 0.25µm CMOS technology and is sent for fabrication. To improve threshold uniformity, each comparator has a 3 bits DAC. The comparator can handle positive and negative input signals. A polarity signal changes the polarity of the threshold level and makes the output signal always active high. The output signal is latched by a 40MHz clock and is selectable between time-over-threshold mode (in 25ns bins) and one pulse mode (25ns). Simulation results will be discussed in section II.

I. INTRODUCTION

For fast primary vertex reconstruction and pile-up rejection, binary hit information is needed from the LHCb vertex detector front-end electronics. Therefore a comparator for the Beetle chip has been designed.

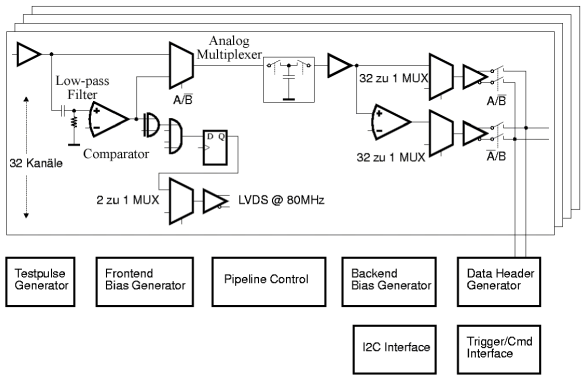

Figure 1: Block diagram of the Beetle chip

The Beetle is a 128 channel analog pipeline chip for the LHCb experiment and can either be used as an analog pipeline chip or as binary pipeline chip. Each channel consists of a charge sensitive preamplifier / shaper, an analog pipeline of a programmable maximum length of 160 stages with integrated derandomizing buffer of 16 stages and a serial read-out for up to 40MHz read-out speed. In case of using the chip as binary pipeline the discriminated output of the shaper is stored into the pipeline and a fast binary multiplexer is used to read out the chip at a speed of 80MHz maximum.

The comparator is, like the Beetle, implemented in a 0.25µm CMOS technology, using rad-tolerant layout rules.

To make the comparator insensitive for low frequency input signals, e.g. temperature drift and different offsets, one of the inputs of the comparator has a low-pass filter to obtain the DC-level of the incoming signal. This level is summed to the threshold level. The threshold level consists of a controllable level used for all comparators (global) and an individual level controlled by a 3 bits DAC for each comparator (local).

The comparator output signal is latched at a well-defined time by a 40MHz clock, which is related to the bunch crossing frequency. The width of the analog comparator input signals is on average 40ns and therefore the time-over-threshold can be longer than one period. By means of an "output mode selection" the output signal can be in time-over-threshold mode (in 25ns bins) or in one pulse mode (25ns) once the input signal went over threshold.

The comparator can deal with positive and negative input signals. A polarity signal switches the polarity of the threshold level and controls the output stage in such a way that the comparator output signal remains positive.

In addition a multiplexer has been designed to store hits as binary information. The multiplexer selects between the front-end shaper output and the comparator output and converts the digital comparator signal in a 0 or

10 MIP analog signal before sending it to the analog pipeline.

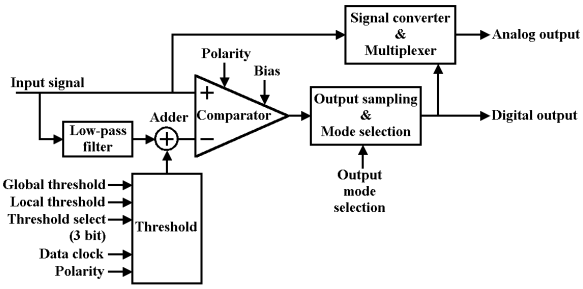

Figure 2: Block diagram of the comparator

In the following subsections each block in the design will be explained in more detail.

A. *Low-pass Filter*

The comparator-input signal from a front-end amplifier-shaper combination consists of a DC-level with a shaped pulse. The DC- level depends on temperature, offsets and bias settings in earlier stages. To make the threshold level insensitive for these fluctuations, the DC-level is obtained with a low-pass filter and added to the threshold level.

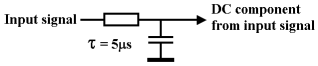

Figure 3: Low-pass filter

The low-pass filter consists of a capacitor and a resistor. The capacitor is made by the gate-source capacitance of a transistor and is about 2.3 pF. The resistor is made by a long channel transistor and has a resistance of about 2 MΩ. So the time constant is about 5μs.

A disadvantage is that also the signal pulses are integrated which causes an error voltage in the threshold level. The size of this error voltage depends on the signal pulse amplitude and the repetition rate.

$$\text{Error voltage} = \frac{t}{T-t} \cdot V_p \quad [\text{V}]$$

Where t is the width of the signal pulse [40ns shaping time], T is the repetition rate [s] and Vp is the amplitude of the signal pulse [V].

Assume a channel receives a hit every μs (1MHz). The error of the threshold voltage will be about 4% of the signal pulse amplitude and will not have a big consequence for the performance of the comparator.

$$\text{Error voltage} = \left(\frac{40}{1000-40} \right) \cdot 100\text{mV} = 4.2\text{mV}$$

This is simulated in simulation 4 (figure 15)

B. *Adder*

The adder consists of a source-follower and a resistor. The source-follower buffers the output voltage from the low-pass filter. The threshold level is the voltage on the source plus or minus the voltage drop across the resistor. This voltage drop is made by a current (I threshold) from the threshold circuit (figure 5).

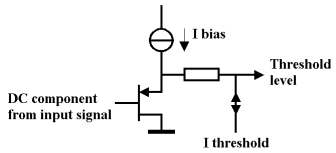

Figure 4: Adder

C. *Threshold*

The controllable threshold level is the sum of a level used for all comparators (global) and an individual level controlled by a 3 bits DAC for each comparator (local). The sum is converted into a current (I threshold) and is used for the adder above (figure 4). The threshold current can be switched positive or negative, depending on the polarity of the input signal.

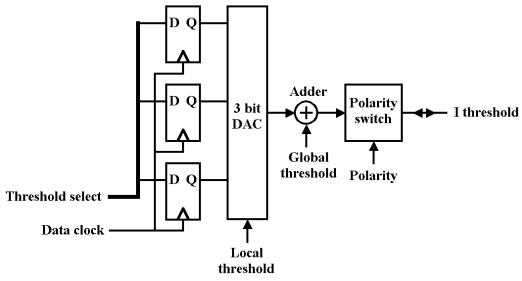

Figure 5: Threshold circuit

D. *Comparator*

The comparator consists of two differential amplifiers with a gain of 30 x. The first stage has a differential output to use its gain twice. A buffer decreases the gain with 0.7 x. So the total gain is 0.7 x 2 x 30 x 30 = 1260. This is simulated and can be seen in figure 14.

The signal input has a source follower to keep the DC-levels on both inputs the same. The source follower of the threshold input is placed in the adder (figure 4).

With a polarity signal the output signal can be inverted. This makes the output signal always active high, in spite of the polarity of the input signal.

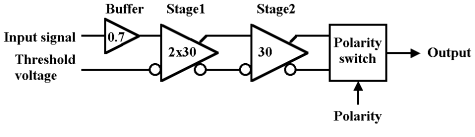

Figure 6: Comparator

The circuits of the two inputs are symmetrical to make an accurate comparison of the input signals. This can be seen in the circuit diagram of the comparator (figure 8).

The transistors with the same function are paired and matched. Matching tolerances are minimized by appropriate layout techniques. An example is given for the two buffers.

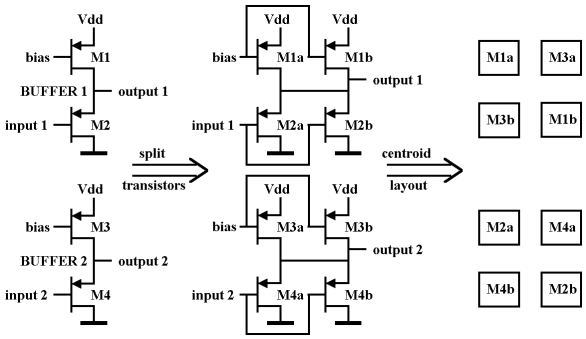

Figure 7: Layout example for better matching

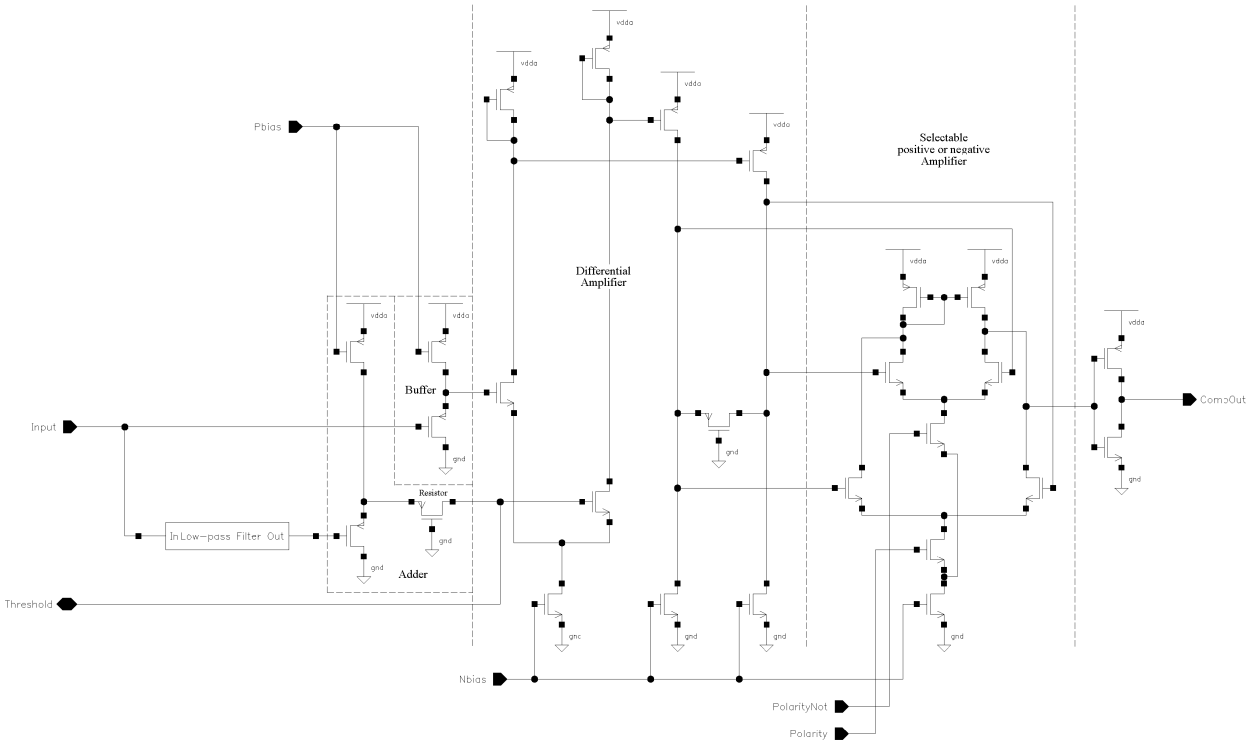

Figure 8: Circuit diagram of the comparator

E. Output sampling & Mode selection

The output signal of the comparator is latched at a well-defined time. This latch is clocked by a 40MHz clock, which is related to the bunch crossing frequency.

The time-over-threshold can be longer than one period. By means of an "output mode selection" the output signal can be in time-over-threshold mode (in 25ns bins) or in one pulse mode (25ns) once the input signal went over threshold.

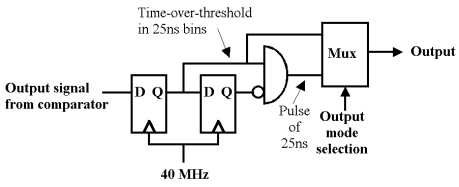

Figure 9: Output sampling & Mode selection

The 2 modes of output selection are simulated and can be seen in figure 10

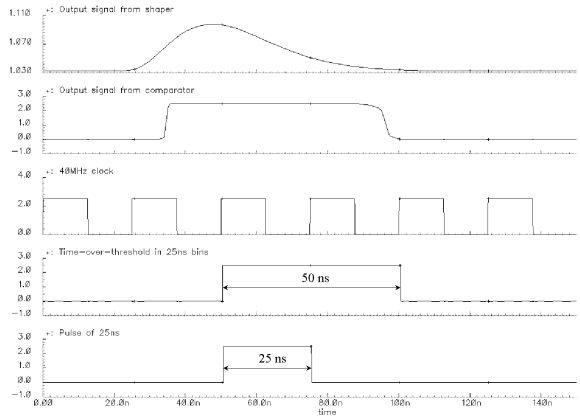

Figure 10: Two modes of operation

F. Signal converter & Multiplexer

For fast primary vertex reconstruction and pile-up rejection, binary hit information is needed from the LHCb vertex detector front-end electronics. Therefore one can select between binary information from the comparator and an analog signal from the shaper. The selection is done with an analog multiplexer and the digital output voltage of the comparator has to be converted into 0 or 10 MIP analog signal.

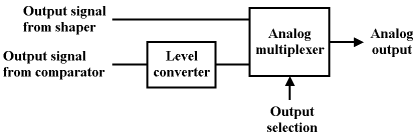

Figure 11: Signal converter & Multiplexer

II. SIMULATION RESULTS

A. Simulation 1

The input signal (F/E shaper output) is swept from 1 to 10 MIP. The shaper output is about 16mV per MIP. The threshold level is set just below 5 MIP. In the figure 12 one can see successively the input signal, the comparator output signal, the sampled output signal of the comparator and the sampling clock. As expected the output signal is only active when the input signal is 5 MIP or more.

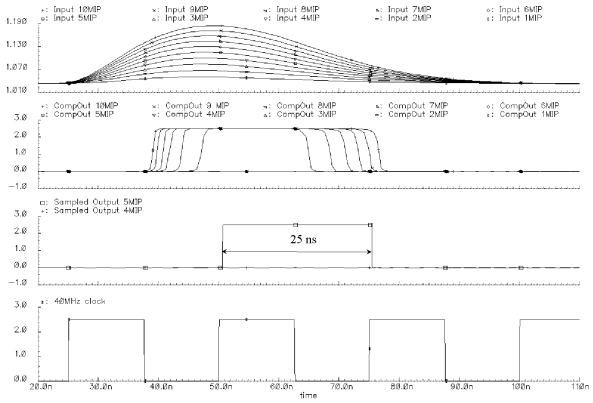

Figure 12: Output signals Vs input signal at a 5 MIP threshold level

B. Simulation 2

The threshold level is set to 0.5 MIP. Now all inputs will generate an output signal. In figure 13 one can see the time-walk from 1 to 10 MIP. This is about 8ns.

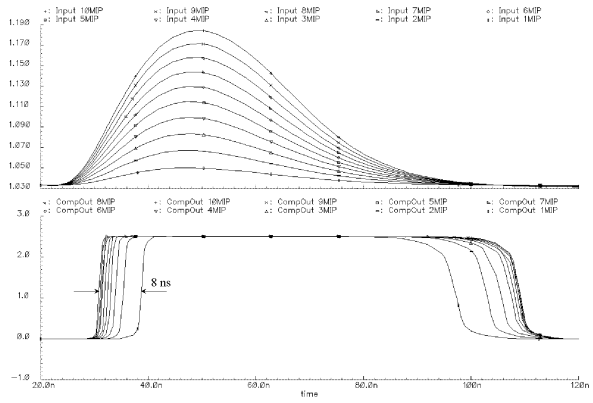

Figure 13: Output signals Vs input signal at a 0.5 MIP threshold level

C. Simulation 3

As calculated in subsection “D. Comparator” the gain is about 1260 times. With a power supply voltage of 2.5V the input signal must go 2mV above threshold to make a full swing output signal. In the figure 14 the input signal swings +/- 2mV around the threshold level and the output signal goes from ground to Vdd.

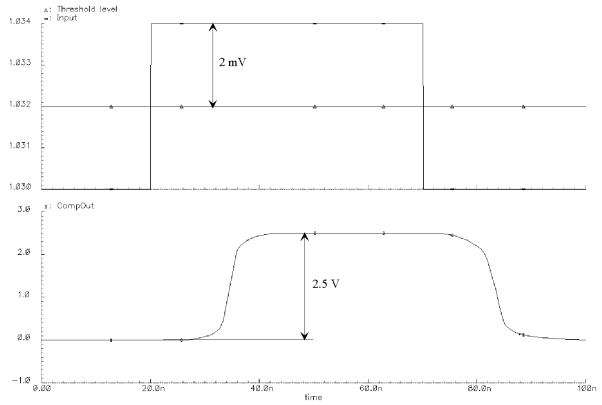

Figure 14: Output signal Vs 2 mV input signal

D. Simulation 4

In this simulation the behavior of the low-pass filter (figure 3) is simulated. Every micro second the filter gets an input signal with a pulse width of 40ns and an amplitude of 100mV. The output signal climbs with a timing constant of 5 µs to 4.8mV, which is almost the 4.2mV as was calculated in subsection "A. Low-pass filter".

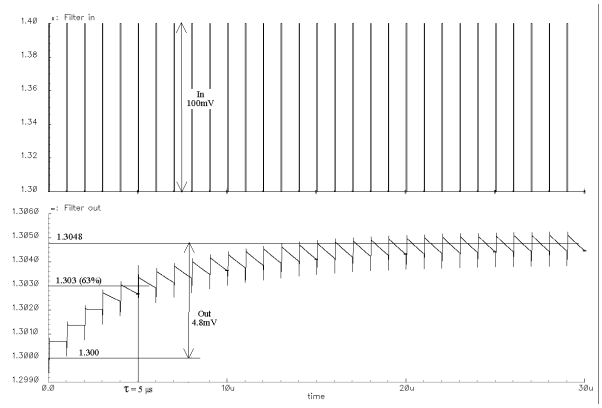

Figure 15: Output signal filter Vs an input signal every micro second

The simulation results are summarized in Table 1.

Table1: Comparator specifications

Input range	GND+0.8V < Uin < VDD–0.8V
Time-walk	8ns
Min. detectable pulse	2mV above threshold
Power consumption	350µW

III. LAYOUT DESIGN

The layout of the comparator (without the output sampling and analog multiplexer), low-pass filter and threshold circuit is shown in figure 16 and 17. The size of the design is 107 x 40 µm.

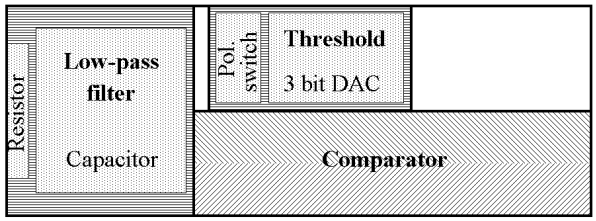

Figure 16: Placement of the components on the layout

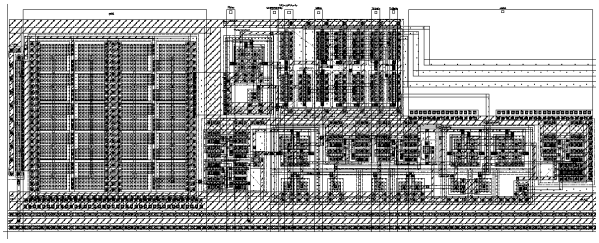

Figure 17: Layout of comparator, threshold circuit and low-pass filter

IV. WORK TO BE DONE

The comparator will be tested in a Frontend-Comparator test-chip and in the Beetle 1.0 chip.

Output DC-signal variations of frontends and comparators will be measured to obtain more information about the matching tolerances. With the threshold DAC one can compensate for some mismatch, but if one can compensate for the DC-signal variations of all components, the low-pass filter can be omitted. The results will be implemented in the next submission of the Beetle chip, which is planned in spring 2001.

V. CONCLUSION

The simulation results show that the comparator works as was intended and that it meets the requirements [2] as foreseen for the pile-up detector.

VI. REFERENCES

1. Wolfgang Fallot-Burghardt, *"A CMOS Mixed-Signal Readout Chip for the Microstrip Detectors of HERA-B"*, A thesis for his examination for the doctors degree., 24 June 1998.
2. M. Feuerstack-Raible, *"Beetle – A Readout Chip for LHCb"*, http://wwwasic.ihep.uni-heidelberg.de/lhcb/
3. Willy M.C. Sansen, Zhong Yuan Chang, *"Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies"*, Kluwer Academic Publishers, 1991, ISBN: 0-7923-9096-2.
4. AMS, *Analog & Mixed Signal Application Note – Device Matching rules.*