Use of External Resistor to Prevent Radiation Induced Latch-up in Commercial CMOS IC's

Skorobogatov P.K., Nikiforov A.Y., Demidov A.A.

Specialized Electronic Systems, Kashirskoe shosse, 31, 115409, Moscow, Russia
pkskor@aha.ru)

Abstract

It is shown that in the case of external resistor usage to prevent radiation induced latch-up in commercial CMOS IC's we have the increase of IC recovery time up to tens of microsecond due to deep saturation of parasitic bipolar transistors. Under experiments and numerical calculations it was found that there is an optimal value of external resistor that provides the minimal recovery time of IC.

I. INTRODUCTION

The usage of commercial-off-the-shelf (COTS) CMOS IC's in radiation environment is restricted by the possibility of their latch-up behaviour under irradiation. The external resistor in power supply circuit is a well-known way to prevent latch-up [1]. This method is found on the restriction of IC power supply current at the value below then holding level. However in this case we unfortunately have the increase of IC recovery time up to tens of microsecond due to deep saturation of parasitic bipolar transistors. A resistor in the power supply line may cause excessive voltage drop in dynamic operation.

A technique to prevent latch-up in COTS CMOS IC's has been investigated and presented in this paper. It is found on the search of optimal resistor value that provides the reliable latch-up prevention with minimal recovery time and power supply voltage drop.

The specialized CMOS test structure was manufactured to investigate the influence of external resistor on latch-up parameters. The two-dimensional software simulator "DIODE-2D" was used for numerical analysis of test structure. The results obtained were verified experimentally and applied to commercial CMOS IC's.

II. TEST DESCRIPTION

The specialized CMOS test structure TSCLU2 is manufactured in conventional 2-μm bulk CMOS process and includes n-well p-n-p-n structure with well-substrate p-n junction 48x78 μm size. It is described in [2] in detail.

The devices selected for the investigations were bulk COTS CMOS IC's 564LA8 and 537RU6 (functional analogues of 2x4NAND CD4012A and 4kx1 static CMOS RAM HM6504).

Pulsed laser simulator "RADON-5E" with 1.06 μm wavelength and 11 ns pulse width was used in the experiments as a radiation source to induce latch-up. The laser pulse maximum intensity was varied from $6 \cdot 10^2$ up to $2.1 \cdot 10^6$ W/cm^2 with laser spot size covering the entire chip. It provides in silicon the equivalent dose rates up to 10^{12} rad(Si)/s. The power line transient response was registered with "Tektronix TDS-220" digital oscilloscope.

In order to perform the test structure latch-up analysis the "DIODE-2D" software simulator was used which is the two-dimensional solver of fundamental system of equations in semiconductor [3].

II. NUMERICAL TO EXPERIMENTAL COMPARATIVE RESULTS

First of all the latch-up free region of test structure was determined. The results of numerical simulation are presented in Fig. 1 for Vcc = 5V. When the external resistance R_e becomes more than some critical value R_{ec} we have the reliable prevention of latch-up. Numerical calculations give R_{ec} =1005 Ω for TSCLU2 test structure.

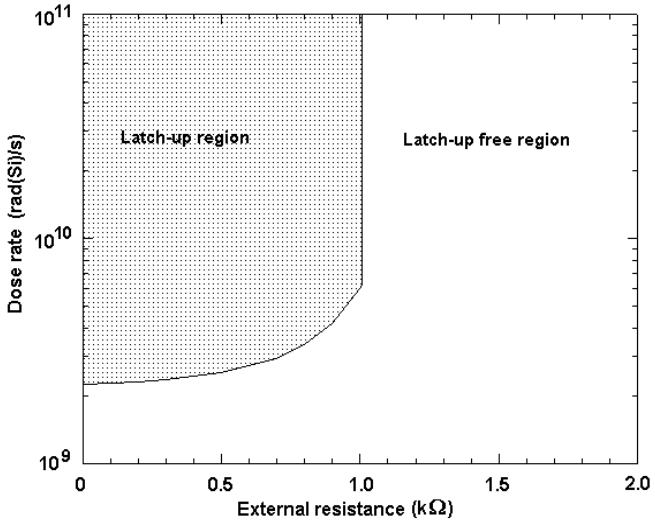

Figure. 1: Numerical TSCLU2 test structure latch-up threshold level vs external resistor value

The experimentally determined R_{ec} value is equal to 950 Ω. The absence of latch-up (in latch-up free region) was observed in the range up to 10^{12} rad(Si)/s. The experiment

confirmed that the influence of external resistor value on latch-up level (in the latch-up region) is relatively small.

The experimentally observed power supply line voltage waveforms are presented in Fig. 2 for different values of external resistance. The increase of external resistance tends to deep a saturation of parasitic bipolar transistors that increase a recovery time.

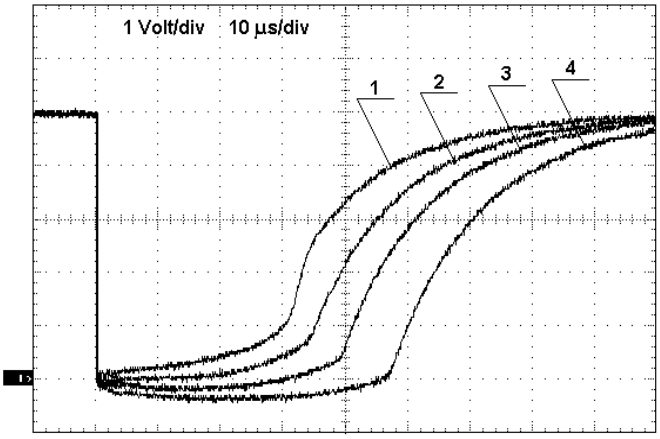

Figure. 2: Test structure power supply line voltage waveforms at dose rate $5.3 \cdot 10^{11}$ rad(Si)/s for different external resistances: 1.1 kΩ (1), 2 kΩ (2), 3 kΩ (3) and 5 kΩ (4)

It is very interesting for practice to determine the influence of external resistance on test structure recovery time. The experimental results together with numerical calculations are presented in Fig. 3. The test structure is considered to be recovered if power supply line voltage reaches the level below 0.5V of nominal value (criterion of recovery).

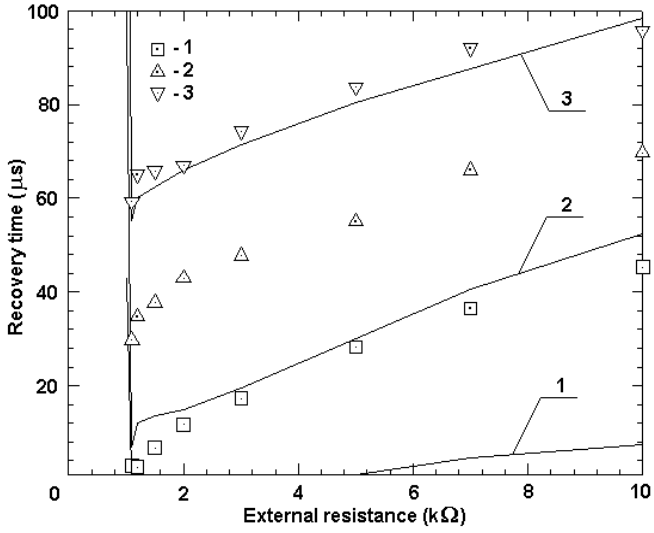

Figure. 3: Numerical and experimentally determined TSCLU2 test structure recovery time vs external resistance for different dose rates: $6.6 \cdot 10^{9}$ (1), $4.7 \cdot 10^{10}$ (2) and $5.32 \cdot 10^{11}$ (3) rad(Si)/s

One can see that the recovery time tends to reduce with external resistance reduction up to critical value. The experimental data confirm the numerical curves tendency. However the absolute values of recovery times differ from that of numerical for low dose rates.

To determine the optimal value of external resistance the initial part of Fig. 3 is represented in Fig. 4.

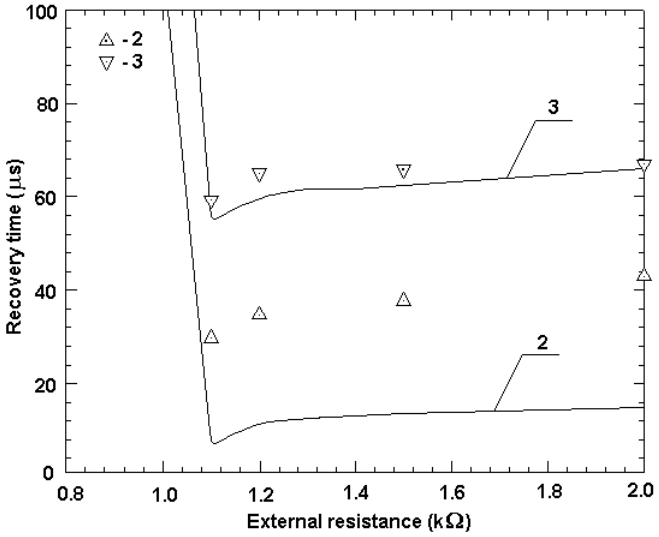

Figure. 4: Numerical and experimentally determined TSCLU2 test structure recovery time vs external resistance for different dose rates: $4.7 \cdot 10^{10}$ (2) and $5.32 \cdot 10^{11}$ (3) rad(Si)/s

You can see that the calculated optimal value of external resistance (R_{eopt}) is equal 1.1 kΩ that is near the critical value of 1.005 kΩ. It is very important to note that when external resistance is in the range $R_{ec} < R_e < R_{eopt}$ the recovery time tends to rise very sharply. From the other hand if the increase of R_e over R_{ec} does not exceed $(1.5 - 2) \cdot R_{ec}$ the rise of recovery time is not very sufficient.

To investigate the features of COTS CMOS IC's latch-up behaviour the experiments under the samples of 564LA8 and 537RU6 IC's were conducted. The results for 564LA8 at dose rate of $5.4 \cdot 10^{9}$ rad(Si)/s are presented in Fig. 5.

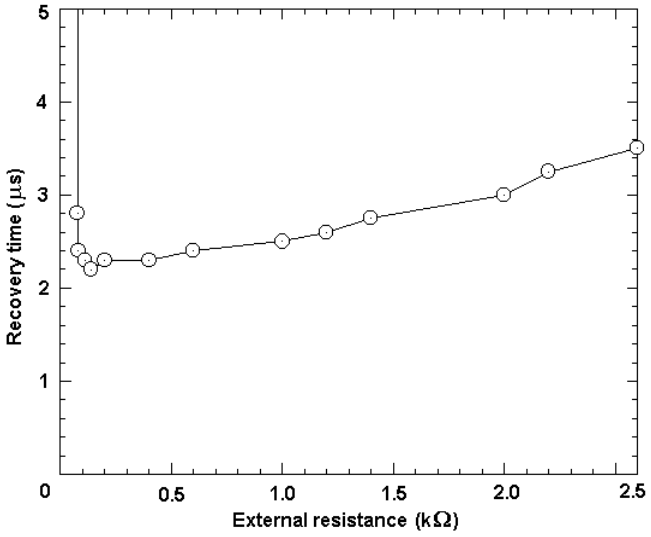

Figure. 5: Experimentally determined 564LA8 recovery time vs external resistance for dose rate $5.4 \cdot 10^{9}$ rad(Si)/s

In this case the optimal value of R_e is near the 130 Ω and more sufficiently differs from the critical value 75 Ω. The rise of recovery time with external resistance is also weak.

The experimental results for the CMOS RAM 537RU6 are presented in Fig. 6. It was found that for this IC the optimal external resistance value is approximately equals to its critical value $R_c \cong 76$ Ω.

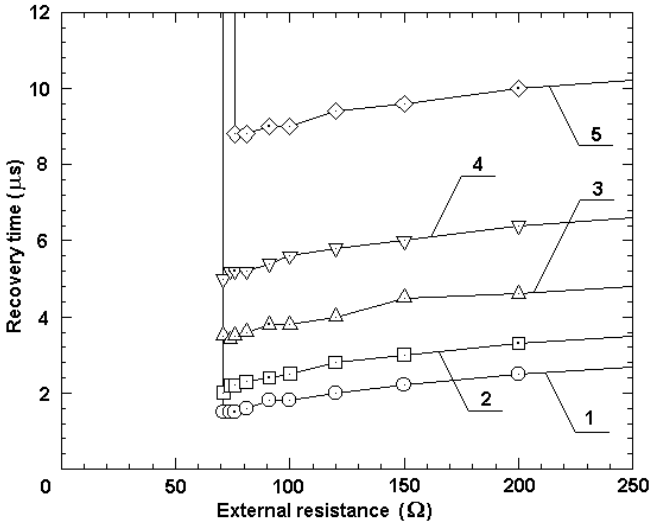

Figure. 6: Experimentally determined 537RU6 recovery times vs external resistance for different dose rates: $2.8 \cdot 10^8$ (1), $5 \cdot 10^8$ (2), $1.4 \cdot 10^9$ (3) and $5.8 \cdot 10^9$ (4) rad(Si)/s

III. Discussion

The results obtained show that the external resistance in power supply line can successfully prevent latch-up in COTS CMOS IC's. If the value of resistance more than critical the latch-up behavior is avoided at any dose rate. The optimal value of external resistance that provides minimal recovery time exceeds its critical value not more than twice. The time recovery vs external resistance dependence over optimal value of resistance is relatively weak. The most unfavorable regime takes place in the case if external resistance is in the range $R_{ec} < R_e < R_{eopt}$.

The precise definition of optimal external resistance is a complex procedure. To estimate the possibility of COTS CMOS IC usage in radiation environment it is necessary to determine the critical value of external resistance by any method (electrical overstress, laser simulation) at maximum level of influence. The value of external resistance may be chosen in the range of $(1.5 – 2) \cdot R_c$. The additional recovery time due to non-optimal chose of R_e is not sufficient.

The possibility of COTS CMOS IC implementation in radiation environment depends on obtained resistance value. If the voltage drop over external resistance in dynamic regime does net exceed admissible value this method may be used to prevent the latch-up behavior. In other case it is necessary to use more complex external circuits [1].

IV. Conclusion

Radiation induced latch-up of COTS CMOS IC's can be prevented with the use of external resistance in the power supply line. The value of external resistance must be carefully selected. The simple way to find the required value is to determine the critical value of resistance that prevents latch-up at maximum available dose rate. The value of the external resistance may be chosen in the range from 1.5 to 2 of critical value. It provides near the optimal conditions for minimization of recovery time. The method is applicable if the voltage drop over external resistance in dynamic regime does net exceed admissible value

The results obtained were verified experimentally and applied to specialized test structure and commercial CMOS IC's.

IV. References

[1]. D.D.Huffman, "Prevention of Radiation Induced Latch-up in Commercially Available CMOS Devices", *IEEE Trans. Nuc. Sci*., Vol. NS-27, No.6, p.1436-1441, December 1980.

[2] A.A.Demidov, A.Y.Nikiforov, P.K.Skorobogatov, "Use of Diffused Laser Irradiation to Improve Dose Rate Simulation Adequacy", Proceedings of the Fifth Workshop on Electronics for LHC Experiments. Snowmass, Colorado, September 20-24, 1999. P. 547-550.

[3]. A.Y.Nikiforov, P.K.Skorobogatov, "Dose Rate Laser Simulation Tests Adequacy: Shadowing and High Intensity Effects Analysis", *IEEE Trans. Nuc. Sci*., Vol. NS-43, No.6, p.3115-3121, December 1996.