Total Dose Irradiation of a 0.25μm Process

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Abstract

A 50 kV X-ray source and an 8 MeV electron beam were used to irradiate MOS transistors from a commercial 0.25 μm process to doses of 50 Mrad(SiO_2) and 80 Mrad(Si) respectively. Threshold voltage shifts of up to -140 mV were observed in PMOS transistors whilst noise measurements showed very little degradation in the white noise region after irradiation and annealing. Detailed results of both static characteristics and noise are presented.

I. INTRODUCTION

Readout electronics at the heart of the CMS microstrip tracker will have to fulfil stringent requirements in terms of speed, density and radiation tolerance. Ionising doses of up to 10 Mrad over ten years of operation are expected for the innermost layers of silicon microstrip detectors and associated readout electronics [1]. The inaccessibility of the CMS detector requires the careful design of all electronic components for these to be fully operational over the projected lifetime of the detector.

The readout system for the silicon microstrips adopted by the CMS collaboration is based on the APV chip series. The APV chips will sample, amplify and store signals from their corresponding microstrip detectors. Until recently, all generations of APV chips were designed and built using qualified radiation hardened technologies. Work done by the RD49 collaboration identified commercial technologies as viable alternatives to older and more expensive radiation hardened technologies [2]. The APV25 is the first chip in the APV series designed in a commercial 0.25 μm CMOS technology [3]. Although no steps are taken in the fabrication process to harden the APV25 chip, it is radiation tolerant by its nature (very thin gate oxide) and by design (the chip features p+ guard-rings and enclosed transistor geometries to suppress leakage current paths).

The best way to characterise radiation tolerance is to expose a circuit directly to a source of ionising radiation. However, a lot of information can be obtained by studying radiation effects on individual transistors, built on relatively simple test structures using the same process. In addition, simple test structures can easily be manufactured by more than one foundry. Past experience has shown that devices from the same process fabricated by two different foundries can exhibit very different behaviour [4]. This could lead to production of chips which might fail to achieve the criteria for operation at CMS.

This report presents results on measurements before and after irradiation of the static characteristics and noise of transistors manufactured by two foundries owned by the same company and employing the same 0.25 μm process.

II. EXPERIMENTAL DETAILS

A Devices

The 0.25 μm process is characterised by the following:

- 5.5 nm gate oxide thickness,
- 2.5 V operating voltage,
- twin well CMOS process,
- shallow trench device isolation (STI).

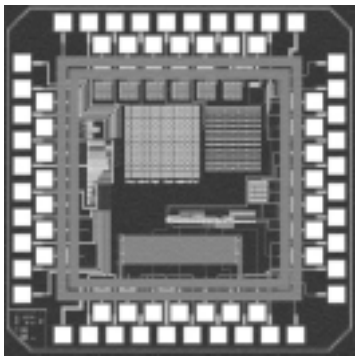

Figure 1: Foundry B test structure.

The test structures contained several transistors, Figure 1. Most of the transistors tested were PMOS transistors with a channel width of 2000 μm. These were chosen because the dominant contribution to the noise in the APV25 is given by the input preamplifier transistor, which is a PMOS transistor with a channel length of 0.36 μm and width of 2000 μm operated with a bias current of ~ 400 μA.

The dimensions of the conducting channels of the transistors are given in Table 1.

Table 1: Channel dimensions for the transistors used in this study.

	Type	Width [µm]	Length [µm]
Foundry A	PMOS	2000	0.36
	PMOS	2000	0.50
	PMOS	2000	0.64
	NMOS	2000	0.36
Foundry B	PMOS	2000	0.24
	PMOS	2000	0.36
	PMOS	2000	0.48
	PMOS	2000	0.60
	PMOS	250	0.36

B Radiation Sources

Two sources of ionising radiation were used to irradiate the test structures, a 50 kV X-ray source and an 8 MeV electron beam.

The 50 kV X-ray source was used to irradiate test structures from both foundries. Most of the dose was delivered by X-rays with energies around 10 keV. The dose rate obtained was approximately 0.5 Mrad(SiO_2)/hour with a 10% uncertainty on the dose rate measurement. Transistors were irradiated in steps to a final dose of 50 Mrad(SiO_2).

A pulsed 8 MeV LINAC electron beam was used to irradiate a test structure from foundry B only. The LINAC produced 0.624krad(Si)/pulse with 50 pulses/s. The dose rate obtained was 112 MRad(Si)/hour, much higher than that given by the X-ray source. The uncertainty on the measurement of the dose rate was 10%. The test structure was irradiated to a final dose of 80 Mrad(Si) with one intermediate step at 40 Mrad(Si).

C Biasing

All devices tested were biased with their gate voltages above threshold ($|V_G|$>500 mV). This does not represent worst case bias conditions for PMOS transistors, where all terminals should be grounded, but represents the actual operating conditions of transistors in the CMS tracker. All devices irradiated by the X-ray source were placed in an oven at 100^o C for a week to speed up the annealing processes. The transistors were also biased during annealing.

D Noise Measurement Setup

Two slightly different setups were used to measure the noise in transistors irradiated by the two different sources. The setup used to measure the noise in transistors irradiated by the X-ray source is described in more detail in [5]. A spectrum analyser (HP4195A) was used to measure the gate referred voltage noise spectra of the device under test (DUT). Both systems were based on converting the noise current at the drain of the DUT to a voltage by a transimpedance amplifier and by referring the voltage noise spectrum back to the gate of the DUT. Noise measurements were performed in the moderate inversion region with 400µA<$|I_{DS}|$<500µA and $|V_{GS}|$=500mV.

III. STATIC CHARACTERISTICS

The threshold voltage is the static parameter which degrades the most and therefore more attention is paid to it in this section. It is calculated by interpolation of the I_{DS}-V_{GS} curve in the linear region of operation of the transistor between two values of drain current. The threshold voltage shift, ΔV_{th}, is calculated by subtracting the pre-irradiation value of the threshold voltage from its value after irradiation.

A X-ray irradiations

Transistors from both foundries were irradiated with the X-ray source.

1) PMOS Transistors

Both interface traps and oxide trapped charge in the gate oxide cause a negative threshold voltage shift in PMOS transistors. Figures 2 and 3 show ΔV_{th} for PMOS transistors taken from both foundries, with the points without background representing the shift after the annealing stage.

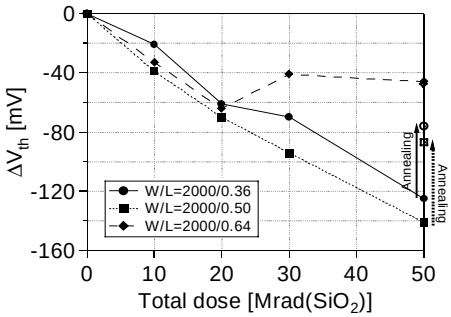

Figure 2: PMOS transistor threshold voltage shift, foundry A.

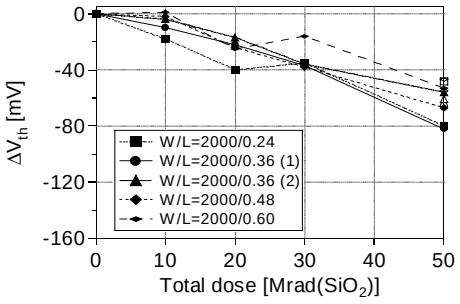

Figure 3: PMOS transistor threshold voltage shift, foundry B.

The maximum shift is around -125 mV for foundry A and -80 mV for foundry B at 50 Mrad(SiO_2) for transistors of comparable dimensions (W/L=2000/0.36). The non-linear behaviour in Figure 3 is due to the fact that the transistors were left for different time periods between irradiation steps, allowing some room temperature annealing to take effect. After

the oven annealing, most transistors show some partial recovery, with lower threshold voltage shifts. These shifts in the threshold voltage are very low and would not cause a loss of functionality in ASICs such as the APV25.

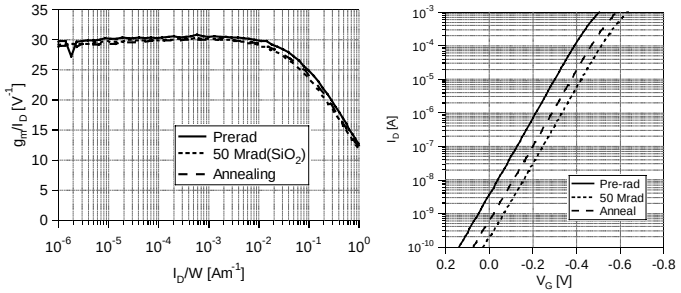

Figure 4: PMOS transistor transconductance and subthreshold slope.

The effect of interface states can be distinguished from that of oxide traps by analysing the subthreshold slope of the I_D-V_G curve. The subthreshold slope is taken in the linear region of operation of the chip, where I_D increases linearly with $|V_G|$. Charge traps at the interface can cause a reduction in mobility (reducing $\partial I_D/\partial V_G$). When the reduction in mobility is high, the slope is visibly less steep. Although the threshold voltage shift can clearly be seen, there is no significant change in the slope for PMOS transistors, Figure 4. This would suggest that very few interface states contribute to ΔV_{th}. There is no significant change in transconductance.

2) NMOS Transistor

Oxide traps cause a negative threshold voltage shift in NMOS transistors whereas interface traps cause a positive threshold voltage shift. The two types of traps compensate and the dominant type will cause a shift in its direction. Since ΔV_{th} is positive, the contribution from interface states is larger than that from oxide traps, Figure 5. After 50 Mrad, ΔV_{th} is 14 mV. After annealing however, ΔV_{th} increases to 73 mV. It is unlikely that new interface states are being created. The most likely explanation for the jump in ΔV_{th} is that the number of oxide traps is being reduced by the thermal annealing process.

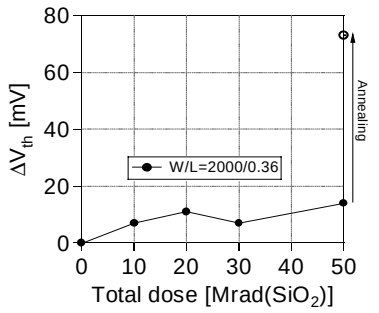

Figure 5: NMOS transistor threshold voltage shift, foundry A.

A reduction in the slope of the I_D-V_G curve is visible after irradiation and after annealing, Figure 6. This is a clear indication that the irradiation process has generated interface states, which cause a reduction in the mobility of charge carriers within the thin conducting channel beneath the oxide. The reduction in mobility can also be seen in a plot of the normalised transconductance (g_m/I_D), Figure 6. g_m/I_D decreases by 9 % after 50 Mrad and by 15 % after annealing (weak inversion region, $I_D/W = 10^{-5}$ Am^{-1}).

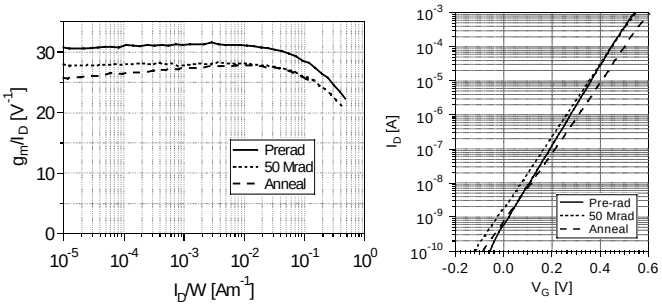

Figure 6: NMOS transistor transconductance and subthreshold slope.

B Electron Beam Irradiations

The 8 MeV electron beam was used to irradiate one test structure from foundry B. The threshold voltage shift for the transistor with W/L=2000/0.36 is -126 mV at a total ionising dose of 80 Mrad(Si), Figure 7.

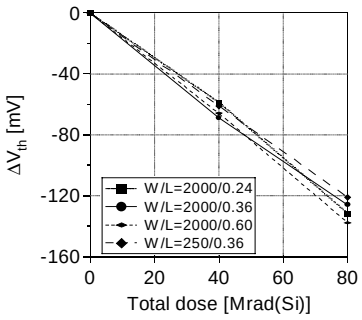

Figure 7: PMOS transistor threshold voltage shift.

The transconductance and the subthreshold slope curves (not shown here) have very similar characteristics to those obtained from measurements of PMOS transistors irradiated with X-rays (Figure 4).

IV. NOISE

The determination of flicker noise characteristics in PMOS transistors was made difficult by the fact that noise measurements were done over a relatively small frequency range. For PMOS transistors the flicker noise corner before irradiation lies between 50 and 100 kHz. An analysis of the evolution of the white noise levels with irradiation is useful since the region of interest in the frequency spectrum (for the

operation of APV25 chips) lies above 2 MHz. All results presented in this section relate to transistors with W/L=2000/0.36.

A X-ray irradiations

The noise characteristics for PMOS transistors from both foundries irradiated with X-rays are shown in Figures 8 and 9. The transistor from foundry A shows lower flicker noise and white noise levels.

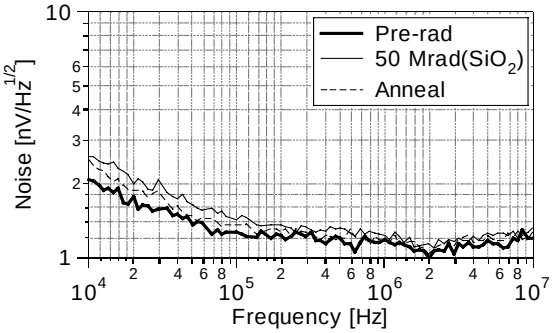

Figure 8: Noise of a PMOS transistor from foundry A.

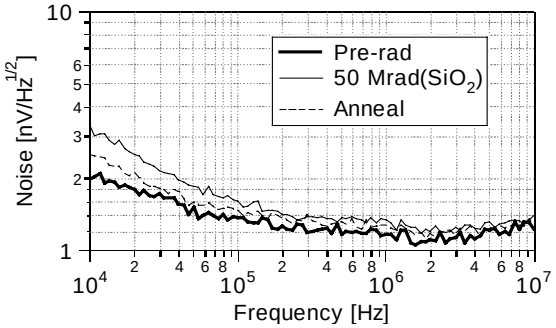

Figure 9: Noise of a PMOS transistor from foundry B.

The white noise levels for the PMOS transistors are reported in Table 2. These were calculated by averaging the white noise values for frequencies above 1 MHz. They change very little after irradiation and annealing. The PMOS transistor from foundry B has a slightly higher white noise level before irradiation and this level increases by a higher fraction after irradiation compared to the PMOS transistor from foundry A.

Table 2: White noise levels and percentage increase w.r.t pre-rad values for PMOS transistors irradiated with X-rays.

	PMOS Foundry A		PMOS Foundry B	
Dose [Mrad(SiO_2)]	Noise level [nV/√Hz]	% increase	Noise level [nV/√Hz]	% increase
0	1.12	0	1.14	0
50	1.2	7	1.25	10
Anneal	1.17	4.5	1.21	6

The corner noise frequency for the NMOS transistor lies around 2 MHz, Figure 10. After irradiation, the white noise level increases significantly compared to the PMOS transistors measured. This provides more evidence suggesting that interface states are being generated during the irradiation process.

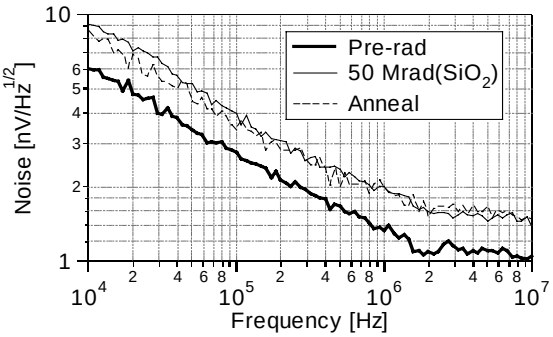

Figure 10: Noise of an NMOS transistor from foundry A.

B Electron Beam Irradiations

Figure 11 shows the evolution of the noise characteristics of the PMOS transistor irradiated with 8 MeV electrons. The corner noise frequency increases from 50 kHz before irradiation to 400 kHz after 80 Mrad(Si).

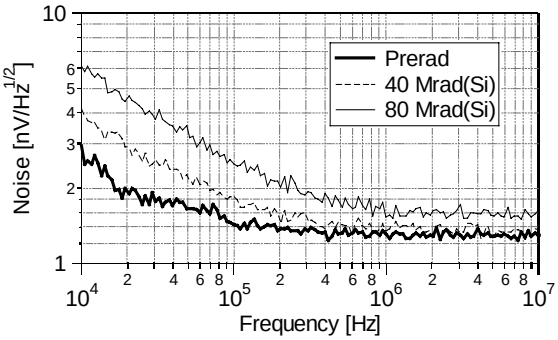

Figure 11: Noise of a PMOS transistor from foundry B.

The average white noise level does not increase significantly after 40 Mrad(Si). However, after 80 Mrad(Si) there is a 20 % increase in the white noise level, Table 3.

Table 3: White noise levels and percentage increase w.r.t pre-rad values for the PMOS transistor irradiated with electrons.

Dose [Mrad(Si)]	Noise Level [nV/√Hz]	% increase
0	1.29	0
40	1.34	4
80	1.55	20

The higher noise levels in Table 3 (compared to Table 2) can be explained by the fact that the bias conditions during the noise

measurements were different ($|I_{DS}|$=500μA for measurements in Table 2, $|I_{DS}|$=400μA for measurements in Table 3).

V. DISCUSSION

A Comparison of the Two Ionising Sources

Radiation induced parameter degradation depends on the energy of the incident radiation. Two effects which are energy dependent are absorbed-dose enhancement (important for X-rays) and electron-hole recombination. For example, at low fields (not the case here) nearly twice as much electron-hole recombination occurs for 10 keV X-rays compared to Cobalt-60 gamma radiation [6].

10 keV photons and 8 MeV electrons were used to irradiate PMOS transistors. For 10 keV X-rays, Dose(Si) ≈ 1.8 x Dose(SiO_2) [7] so 50 Mrad(SiO_2) should be roughly equivalent to 90 Mrad(Si). We might expect the results in Figures 3 (X-rays) & 7 (electrons) to be similar. This is not the case. For the PMOS transistor with W/L=2000/0.36, ΔV_{th} = -82 mV for X-rays and ΔV_{th} = -126 mV for electrons.

The dose rate used for the electron irradiations was around 200 times higher than that used during X-ray irradiations. In addition, the electron source was pulsed. These factors, combined with electron-hole recombination and absorbed-dose enhancement, contribute to the differences observed between Figures 3 & 7. The relative importance of each factor is unknown.

B Comparison of the Two Foundries

All the test structures involved in this study were manufactured by two foundries owned by the same company. The behaviour of transistors was expected to be the same after irradiation and annealing since the two foundries use the same process. However, Table 4 shows some small differences between the two foundries. Transistors from foundry A have a higher threshold voltage shift after irradiation, although they show better recovery after annealing. Transistors from foundry B have a higher white noise level, which increases more significantly after irradiation. These results suggest that more oxide traps are being generated in the oxide of foundry A but its Si/SiO_2 interface is of higher quality.

Table 4: Comparison between PMOS transistors from foundries A and B (W/L=2000/0.36).

	Foundry A	Foundry B
ΔV_{th} after 50 Mrad(SiO_2)	-125 mV	-82 mV
ΔV_{th} after annealing	-76 mV	-66 mV
White noise level increase after 50 Mrad(SiO_2)	7	10
White noise level increase after annealing	4.5	6

More statistics are needed to confirm these differences, since only one test structure from each foundry was irradiated.

VI. CONCLUSIONS

Transistors from the 0.25 μm CMOS process used to manufacture APV25 chips were irradiated to ionising doses of 50 Mrad(SiO_2) with an X-ray source and 80 Mrad(Si) with an electron beam, much higher doses than those expected in the CMS microstrip tracker. The maximum shift observed in PMOS transistors was less than -140 mV, with most transistors showing some recovery after annealing. The NMOS transistor showed a small positive shift (14 mV) after irradiation and an increase in the value of this shift after annealing (73 mV). These radiation induced shifts would not significantly affect the functionality of the APV25.

The white noise levels for the PMOS transistors did not increase significantly after X-ray irradiation. There was a 20 % increase in the white noise levels after the 80 Mrad(Si) electron beam irradiation. The noise degradation in the NMOS transistor was much more pronounced, with a 40 % increase in the white noise levels after X-ray irradiation.

VII. REFERENCES

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