Comparative Accuracy Study of Current-Mode versus Voltage Mode Analog Memory in 0.25µm Technology.

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Abstract

The aim of this work is the study of switched-current and voltage-mode memory cells in order to develop a model including non-ideal effects such as charge injections, non-linear capacitance and readout system influence. These models will allow non-linearity control regard to surface, speed and power criteria in digital dedicated submicrometer technology. Such models lead to a memory cell optimization in order to include it in an analog memory. The goal of our work is to identify accuracy limits that can be reached with minimum size architectures in a deep submicrometer technology (0.25 µm) for both types of cells: voltage mode and current mode. By studying operating phases of each cell, we have developed theoretical models that include non-linear effects.

I. INTRODUCTION

This work is focused on the Silicon Tracker detector for CMS experiences. In the front-end chip the analog data's are stored in an analog memory waiting the first level trigger decision [1]. To preserve precisely the signal the memory must be accurate; a good value for such memory is about 8 to 10-bit resolution. But the high-energy environment needs low-power, radiation-hard and small area solutions. For cheaper solutions single polysilicon submicrometer CMOS technology are selected. So the new challenge is to develop accurate analog memory in digital dedicated low voltage CMOS Technologies.

By definition, an analog memory consists of several thousands of channels of several hundreds of depth cells. The study of these memories goes through memory cell performance identification followed by the superposition of random distribution of the characteristics due to a spatial distribution of the cells. The cells have to be faithfully reproducible, low-noise, of minimum area and power.

Power per cell and area per cell are critical points. In a front-end chip as FILTRES [1] or APV the size of the analog memory is about 1/4 to 1/3 of the total area. In fact a little area increase for one cell is dramatic for all the circuit. A state of the art on analog memories works show that the balance between power and area can be achieved by using submicrometer technologies. Moreover, such technologies can be used in radiating environment. But the supply voltages are reduced thus limiting the dynamic range of voltage-mode signals. So an interesting alternative is the current mode approach. Such memory cell is based on a second-generation current copier [2] that introduce a feedback loop in the acquisition phase implying lower non-linearity and for which dynamic range is not intimately bound to power supplies. These structures are fully compatibles with the new CMOS submicrometer technologies dedicated to digital circuits. Indeed, there are not limited (first approximation) by linearity and hysteresis of storage capacitors, like in voltage-mode. In this work the two approach (voltage and current) are studded and than compared. With supply voltage down scaling, the Non-linearity of the devices is a new limitation in the high precision feasibility. The classical voltage storage cell is greatly affected by the capacitor non-linear behavior and in second order by the charge injections [3,4].

As stated above the dynamic range reduction impose that the acceptable linearity deviation must be reduced for preserving the accuracy before conversion into a digital form. Our idea is to limit the non-linearity deviation of the static characteristic below a fraction of the quantum resolution. It is then important to related the non-linear characteristic with the quantization noise power and decide to keep the power of the harmonics lower then the quantization noise power.

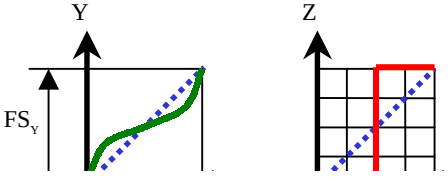
To achieve such study we develop a polynomial model of the static transfer characteristic using Taylor series developments: $y(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + ...$, where the term a_0 is an offset a_1 the small signal gain and all other coefficients are the Non-Linear error terms. The coefficients are than analyzed to control the Non-linearity effects. In the two approaches we take into account the read out system which has an important effects.

The aim of such a study is to propose an easy and accurate model for a non-linearity quantitative analysis that allows to obtained a non-linearity error NL less than half a quantum. This analysis highlights the predominant factors that influence the non-linearity. Such models allow optimized design for minimum size of the cell, high speed, accurate and low-power criteria.

II. NON LINEAR FORMALISM

Generally in an acquisition system the analog signal is processed before it is converted into a digital form. If the analog part must be transparent then his linearity deviation from an ideal straight-line characteristic must be lower then the quantification error “the quantum”. This statement set the linearity deviation ε_{NL} of the analog part by:

$$\varepsilon_{NL} \leq \frac{q}{k}$$



This figure depicts a typical acquisition system with a Sample and Hold cell in front of an ADC converter. FS_X and FS_Y express the full-scale swing of the variables X and Y around their own quiescent point X_0 and Y_0 respectively. We will assume that ideally $FS_Y = FS_{ADC}$ where FS_{ADC} is the input full-scale of the converter.

The static transfer function of the sample and hold cell is described by a polynomial: $Y=Y_0+y=f(X_0+x)$ with $y=a_1x+a_2x^2+a_3x^3$.

We define the **Non-Linear deviation** by: $\varepsilon_{NL} \equiv y - a_1x \equiv a_2x^2+a_3x^3$. The **Non-Linearity error** is then expressed by:

$$NL \equiv \frac{\max|\varepsilon_{NL}|}{FS_Y} = \frac{\max|\varepsilon_{NL}|}{FS_{ADC}} = \frac{\max|\varepsilon_{NL}|}{q \cdot 2^N} \equiv \frac{1}{k \cdot 2^N}$$

For general expressions of these two terms, we introduce the reduced input variable $m=x/X_0$ and normalize the output signal to the small signal gain of the cell. It becomes for the output signal:

$$\bar{y}(m) = \frac{y(m)}{\bar{a}_1} = m + \frac{\bar{a}_2}{\bar{a}_1}m^2 + \frac{\bar{a}_3}{\bar{a}_1}m^3$$

$$\bar{y}(m) = m + \bar{\bar{a}}_2 m^2 + \bar{\bar{a}}_3 m^3$$

As consequence the Non-Linearity term is expressed by:

$$NL \equiv \frac{1}{2}\max\left|\bar{\bar{a}}_2 m^2 + \bar{\bar{a}}_3 m^3\right|$$

For a sinusoidal input signal $m(t)=M\sin(\omega t)$ with $M \in [-1,+1]$, the output signal becomes: $y(m) \approx Y1\sin(\omega t) + Y2\sin(2\omega t) + Y3\sin(3\omega t)$. The output signal power can be decomposed in the sum of the fundamental and of the harmonic components power: $P(y) = P_f + P_{NL}$ with: $P_f = Y_1^2/2$ and $P_{NL} = (Y_2^2 + Y_3^2)/2$. The **Total Harmonic Distortion** is then given by:

$$THD^2 \equiv \frac{P_{NL}}{P_f} = \frac{1}{4}\left(\bar{\bar{a}}_2^2 + \frac{1}{4}\bar{\bar{a}}_3^2\right)$$

Assuming that ε_{NL} is a random variable with a probability density $p(m)$ expressed by $1/\pi \bullet \sqrt{(M^2 - m^2)}$ for a sinusoidal signal, one can calculate its standard deviation which is related to the Non-Linear Harmonics power: P_{NL}. With the assumption that ε_{NL} is lower then q/k, the Non-Linear Harmonic power P_{NL} is limited by the quantization noise power P_{QN} as follows:

$$P_{NL} \le \frac{3}{2k^2}P_{QN} = \frac{3}{2k^2}\frac{q^2}{12}$$

For an ADC the signal to noise ratio is given by $SNR_{dB} = 6{,}02N + 1{,}76$. The THD is then limited by:

$$THD^2 = \frac{P_{NL}}{P_f} \le \frac{3}{2k^2}\frac{P_{QN}}{P_f} \equiv \frac{3}{2k^2}\frac{1}{SNR}$$

We have treated the **special case k = 2** so the two most important terms can be expressed as follows:

$$NL = \frac{\max\left|\bar{\bar{a}}_2 m^2 + \bar{\bar{a}}_3 m^3\right|}{2} = \frac{\left|\bar{\bar{a}}_2\right| + \left|\bar{\bar{a}}_3\right|}{2} \approx \frac{1}{k}\cdot\frac{1}{2^N}$$

$$THD = \frac{\sqrt{\bar{\bar{a}}_2^2 + \frac{1}{4}\bar{\bar{a}}_3^2}}{2} \approx \frac{1}{k}\cdot\frac{1}{2^N}$$

$$THD_{dB} \approx 10\cdot\log\left(\frac{3}{8}\right) - SNR_{dB} = -6{,}02[N+1]$$

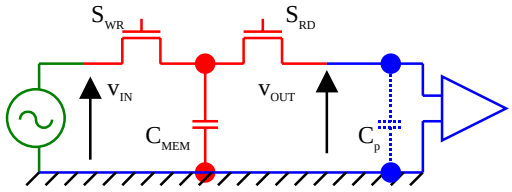
The table 1 shows relations between the ADC resolution in bits, the Non-Linearity error (NL%) and the THD(dB) allowed to the sample and hold cell under our assumption.

N bits	NL%	THD(dB)
8	0,19	-54
9	0,097	-60
10	0,05	-66

Table 1: Non-linearity error and THD related to the number of bits

III. VOLTAGE-MODE CELL STUDY

The input is modeled by an ideal voltage source and the output by an ideal voltage buffer with infinite input impedance. An additional parasitic capacitance is added to model layout contribution.



The memory capacitor designed in a 0,25µm single polysilicon technology is Non-Linear and expressed by:

$$C_{mem} \cong C_n - C_0 \exp\left(-m\frac{V_B}{SL}\right)$$

The reduced variable m is defined around the quiescent point V_B:

$$v_{IN} = V_B(1+m)$$

Through the operating phases the input voltage v_{IN} is related to the output voltage v_{OUT} . The output signal takes the charges injection, the charges sharing, the parasitic capacitor C_p and the Non-Linearity of the storage capacitor C_{mem} into account.

$$v_{OUT} = \frac{C_{mem}}{C_{mem} + C_p}\left(v_{IN} + \Delta V_{INJ}\right)$$

Replacing all the previous terms in the expression of v_{OUT} and using Taylor series we can obtain the final polynomial expression:

$$v_{OUT} = \bar{a}_0 + \bar{a}_1 m + \bar{a}_2 m^2 + \bar{a}_3 m^3$$

The limitation imposed to NL and / or THD need to control the coefficients. We can found three influence parameters defined in the annexes:

- η_0 is linked with the Non-Linearity of the capacitor C_{mem}
- (αC_G and C_{OV}) are linked to the size of the Write switch S_{WR}
- C_p which influence the performance trough the term C_n/C_T.

For a single poly memory capacitor, the write switch size is of less importance. The major contribution of the Non-Linearity comes from the memory capacitor. Figure 1 shows the THD versus the nominal design value C_n of the memory capacitor for various switch sizes. A 1pF memory capacitor allows a precision of 8 bits (see Table 1).

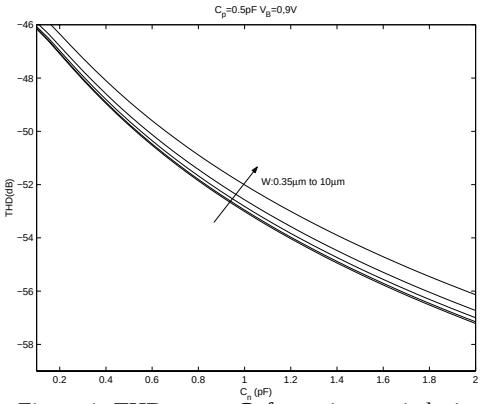


Figure 1: THD versus C_n for various switch size

For an ideal constant capacitor ⇔ [C_0=0], the major Non-Linearity contribution comes from the charges injection combined with switch size.

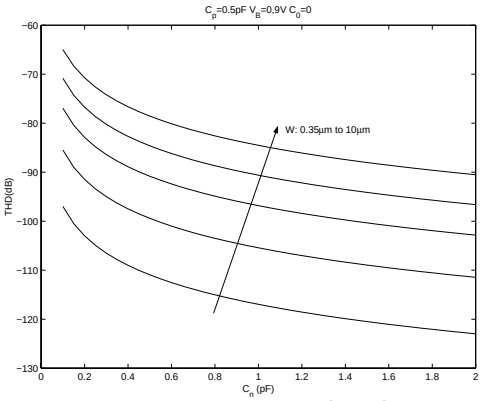
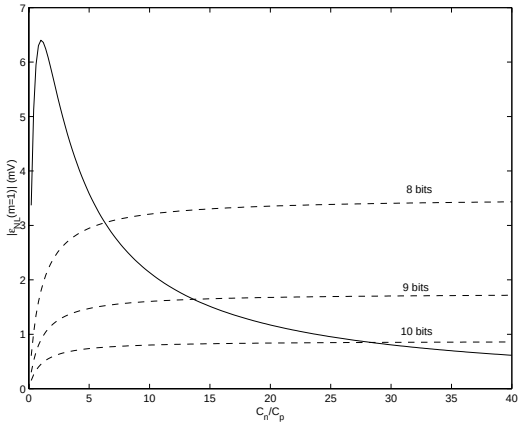


Figure 2: THD versus C_{mem}=C_n

The parasitic capacitor C_p acts as a voltage divider and therefore reduces the signal to noise ratio. The figure 3 shows the linear deviation term ε_{NL} as a function of C_n/C_p ratio. For a ratio greater than 6 we can reach a precision better than 8 bits.



A 10 bits accuracy can be reached if the ratio C_n/C_p is greater than 28.

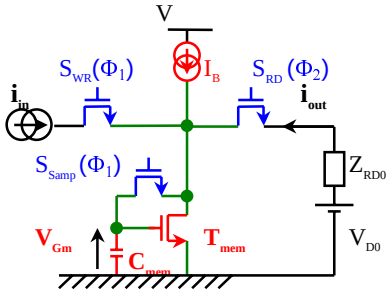
Figure 3: Effect of Cp on the Linear deviation

Measurements on a typical cell designed in the 0,25µm ST Thomson technology are close from the model prediction and simulations results. A Non-linearity error (NL) of 0,175% (better than 8 bits, see Table 1) has been achieved for this cell parameters:

- C_{mem} = 0,8pF
- S_{WR} = (0,35/0,25)µm
- Area = 15x20µm^2

IV. CURRENT-MODE CELL STUDY

The used cell is a second-generation current copier cell. The input source is an ideal current source. The output current buffer is modeled by a Thévenin model around the quiescent point. Through the operating phases the input current i_{IN} is related to the output current i_{OUT}.



During the acquisition phase, the quiescent point is determined for the special case m=0.

$$i_{Dacq} = I_B = \frac{\beta}{2}(V_{G0} - V_{T0})^2 = \frac{\beta}{2}(V_{GT0})^2$$

$$g_{m0} = \left.\frac{\partial i_{Dacq}}{\partial v_{Gacq}}\right|_{m=0} = \beta\frac{W}{L}V_{GT0} = \sqrt{2\beta I_B}$$

In this phase the input current sets the gate voltage v_{Gacq}. Using Taylor series we can express v_{Gacq} as a power series of the reduced variable m=i_{IN}/I_B.

$$i_{IN} = m \cdot I_B = \frac{\beta}{2}\left(v_{Gacq} - v_{T0}\right)^2 - I_B$$

Through the three last operations phases (sampling, storage and read-out) the output current expression becomes:

$$i_{OUT} \approx \frac{\beta}{2}\left(v_{Gacq} - v_{T0} + \Delta V_{INJ} + \Delta V_{\lambda}\right)^2\left(1 + \lambda V_{Drd}\right) - I_B$$

where we found the terms:

- ΔV_{INJ} relating the charges injected by the Sampling switch
- ΔV_{λ} relating the charges injected through the C_{GD} capacitor from T_{mem}
- the channel length modulation term λ from T_{mem}
- V_{Drd} the drain voltage during read-out phase.

Replacing all the previous terms in the expression of i_{OUT} and using Taylor series we can obtain the final expression:

$$i_{OUT} = \bar{a}_0 + \bar{a}_1 m + \bar{a}_2 m^2 + \bar{a}_3 m^3$$

The limitation imposed to NL and / or THD need to control the coefficients. We can found three influence parameters defined in the annexes:

- Γ_n is linked to the capacitors through the K_j terms
- $(1+\lambda V_{D0})$ is linked to λ
- Z_{RD} the impedance seen by the drain of T_{mem}.

For an input signal m(t)=Msin(ωt) with M∈[0,1], the amplitude M acts on the Non-Linearity terms NL or THD. For M=0,3 we can reach a precision of 8 or 9 bits. The figure 4 shows the relation between the Non-Linearity term NL% and the memory capacitor C_{mem} for various sizes of T_{mem} (e.g. for various λ). It can be defined an optimal memory capacitance: $C_{mem}(Opt) \approx 0{,}4pF$.

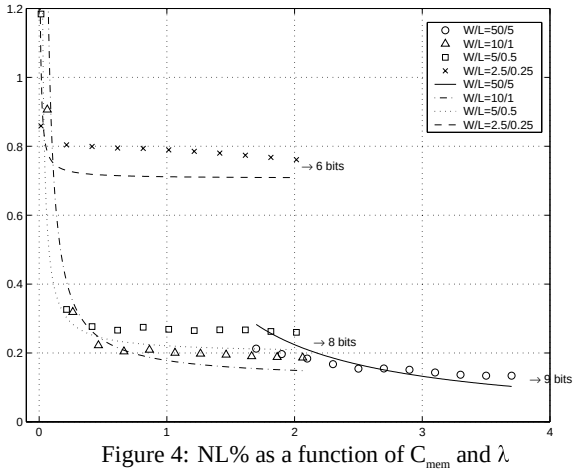


Figure 4: NL% as a function of C_{mem} and λ

The modulation factor λ will be reduced for larger memorization transistor T_{mem} which do not need additional capacitor C_{mem}. So in figure 4 the first point for the transistor with W/L = 50/5 is plotted without additional capacitance.

In the read-out phase, the output current buffer and the read-out switch set the drain voltage.

The total small signal resistance seen by the memory transistor is given by: $Z_{RD} = R_{DSON(RD)} + Z_{RD0}$ the channel resistance during the "ON" condition of the switch and the input impedance of the output buffer respectively. Figure 5 shows the linearity deviation as a function of the input signal m for various Z_{RD}. On the top there are model results, on the bottom there are simulation results.

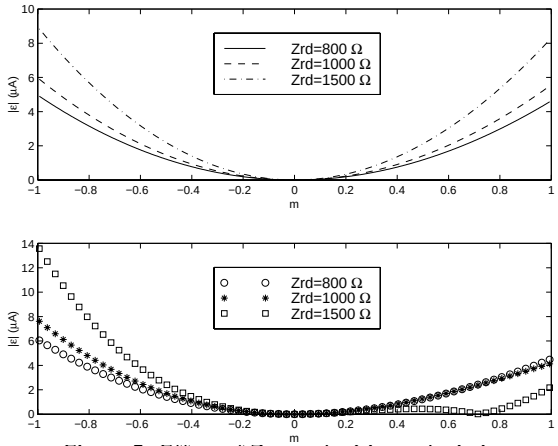


Figure 5: Effect of Z_{RD} on the Linear deviation

The more we reduce Z_{RD}, the more we reduce the Non-Linearity error NL and THD. The differences between model and simulation are du to the R_{DSON} variation over the full-scale input range of m as plotted in figure 6.

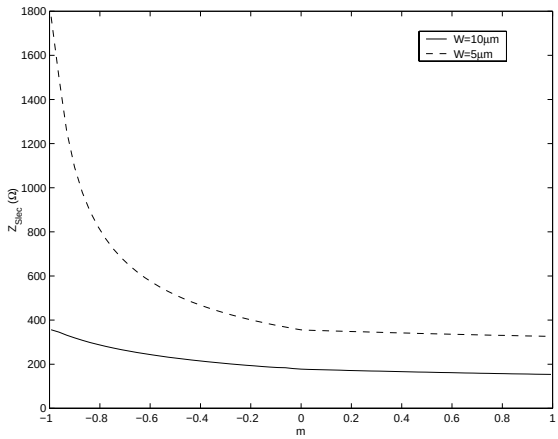


Figure 6: Switch "ON" resistance

Measurements on a typical cell designed in the 0,25µm ST Thomson technology are close from the model prediction and simulations results. A Non-linearity error (NL) of 0,186% (better than 8 bits, see Table 1) has been achieved for this cell parameters:

- $C_{mem} = 0{,}6pF$
- $S_{WR} = (2{,}5/0{,}25)\mu m$
- $T_{mem} = (5/0{,}5)\mu m$
- $Area = 15x25\mu m^2$

V. CONCLUSIONS

We have analyzed the non-linear static transfer function of the two types of analog memory cells. The resulting models help the designer to reach a resolution of 8 to 10 bits in a Deep submicrometer digital dedicated CMOS technology. A prototype circuit has been developed and very close results between measurement and model prediction have been achieved. For the voltage mode we obtain 8 bits resolution with a 0,8pF capacitance and a 300µm^2 area. For the current mode we obtain also 8 bits resolution with a 0,6pF capacitance and a 370µm^2 area.

The comparison of the two approaches will give similar possibility. But for the voltage mode the capacitance non-linearity will be in the future smaller technologies more restrictive. Furthermore with reduced supply voltage the voltage approach seems to be a poor solution.

VI. BIBLIOGRAPHY

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Annexes

Voltage Mode Equations

$$\begin{cases} \Delta V_{INJ} = \dfrac{\alpha Q_{channel} + Q_{overlap}}{C_{mem}} \\ Q_{channel} = -K_{inj}\left(VDD - v_{T(WR)} - v_{IN}\right) \\ Q_{overlap} \approx -K_{OV} VDD \\ v_{T(WR)} = V_{T0} + \gamma\left(\sqrt{\phi + v_{IN}} - \sqrt{\phi}\right) \end{cases} \qquad \begin{cases} K_{inj} = \dfrac{C_{G(WR)}}{C_{mem}} \\ K_{OV} = \dfrac{C_{OV(WR)}}{C_{mem}} \end{cases}$$

$$\begin{cases} \bar{a}_0 = \xi_0 \\ \bar{a}_1 = V_B \cdot \xi_1 \\ \bar{a}_2 = V_B^2\left[\xi_2 - \eta_0 \dfrac{\xi_1}{SL}\right] \\ \bar{a}_3 = V_B^3\left[\xi_3 - \eta_0 \dfrac{\xi_2}{SL} + \left(\dfrac{\eta_0}{2} + \eta_0^2\right)\dfrac{\xi_1}{SL^2}\right] \end{cases}$$

$$\begin{cases} \xi_0 = \dfrac{C_n}{C_T}[V_B] - \eta_0[V_B] - \dfrac{\alpha C_G}{C_T} VDD + \dfrac{\alpha C_G - C_{OV}}{C_T} V_{G0} \\ \xi_1 = \dfrac{C_n}{C_T}\left[1 - \dfrac{V_B}{SL}\eta_0\right] - \eta_0\left[1 - \dfrac{V_B}{SL}\right] - \dfrac{\alpha C_G}{C_T}\dfrac{VDD}{SL}\eta_0 + \eta_0^2\dfrac{V_B}{SL} + \dfrac{\alpha C_G - C_{OV}}{C_T}\left[1 + \dfrac{V_{G0}}{SL}\eta_0 + \dfrac{\gamma}{2\sqrt{V_B + \Phi}}\right] \\ \xi_2 = \dfrac{C_n}{C_T}\left[\dfrac{V_B}{2SL^2}\eta_0\right] + \dfrac{\eta_0}{SL}\left[1 - \dfrac{V_B}{2SL}\right] - \dfrac{\alpha C_G}{C_T}\dfrac{VDD}{2SL^2}\eta_0 - \eta_0^2\dfrac{V_B}{2SL^2} + \dfrac{\alpha C_G - C_{OV}}{C_T}\left[\dfrac{V_{G0}}{2SL^2}\eta_0 - \dfrac{\gamma}{8\left(\sqrt{V_B + \Phi}\right)^3}\right] \\ \xi_2 = -\dfrac{C_n}{C_T}\left[\dfrac{V_B}{6SL^3}\eta_0\right] - \dfrac{\eta_0}{2SL^2}\left[1 - \dfrac{V_B}{3SL}\right] + \dfrac{\alpha C_G}{C_T}\dfrac{VDD}{6SL^3}\eta_0 + \eta_0^2\dfrac{V_B}{6SL^3} + \dfrac{\alpha C_G - C_{OV}}{C_T}\left[\dfrac{V_{G0}}{6SL^3}\eta_0 + \dfrac{\gamma}{24\left(\sqrt{V_B + \Phi}\right)^4}\right] \end{cases}$$

$$\begin{cases} C_T = (C_n - C_0) + C_p \\ \eta_0 = \dfrac{C_O}{C_T} \\ V_{G0} = V_{T0} + V_B \end{cases}$$

Current Mode Equations

$$\begin{cases} \Delta V_{INJ} = \dfrac{\alpha Q_{channel} + Q_{overlap}}{C_{mem}} \\ \text{with} \begin{cases} Q_{channel} = -K_{inj}\left(VDD - v_{TO(Samp)} - V_{T0} - v_{Gacq}\right) \\ Q_{overlap} \approx -K_{OV} VDD \end{cases} \\ \Delta V_\lambda = K_\lambda\left(v_{Drd} - v_{Gacq}\right) \\ v_{Drd} = V_{D0} - Z_{RD} \cdot i_{OUT} \approx V_{D0} - Z_{RD} \cdot i_{IN} \end{cases}$$

$$\begin{cases} \bar{a}_0 \cong I_B\left[(1 + 2\Gamma_0)(1 + \lambda V_{D0}) - 1\right] \\ \bar{a}_1 \cong I_B\left[(1 + \Gamma_0 + \Gamma_1)(1 + \lambda V_{D0}) - (1 + 2\Gamma_0)\lambda Z_{RD} I_B\right] \\ \bar{a}_2 \cong \dfrac{I_B}{4}\left[(2\Gamma_1 - \Gamma_0 - \Gamma_{23})(1 + \lambda V_{D0}) - 4(1 + \Gamma_0 + \Gamma_1)\lambda Z_{RD} I_B\right] \\ \bar{a}_3 \cong \dfrac{I_B}{8}\left[(\Gamma_0 - \Gamma_1)(1 + \lambda V_{D0}) - 8(2\Gamma_1 - \Gamma_0 - \Gamma_{23})\lambda Z_{RD} I_B\right] \end{cases}$$

with

$$\begin{cases} K_{inj} = \dfrac{C_{G(Samp)}}{C_{mem}} \\ K_{OV} = \dfrac{C_{OV(Samp)}}{C_{mem}} \\ K_\lambda = \dfrac{C_{GD(Tmem)}}{C_{GD(Tmem)} + C_{mem}} \end{cases}$$

with

$$\begin{cases} \Gamma_0 = \dfrac{gm_0}{2I_B}\left[K_\lambda(V_{D0} - V_{G0}) - K_{inj}\left(VDD - V_{To(Samp)} - V_{G0}\right) - K_{OV} VDD\right] \\ \Gamma_1 = K_{inj} - K_\lambda(gm_0 Z_{RD} + 1) \\ \Gamma_{23} = K_{inj} - K_\lambda \end{cases}$$