Fiber Optic based readout for BTeV's Pixel Detector

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Abstract

The current paper describes the design of Fiber Optics Links for BTeV's Pixel Detector readout. BTeV pixel detectors chips will be located as close as 6mm from the accelerator's beam into the vacuum pipe. The readout electronics will be located at about 6cm from the beam, imposing strong constrains regarding radiation, mass, power dissipation, and size. The current development is the first prototype designed to initialize, control and readout pixel detector chips using optical links. Results of link performance are shown. The current development is designed in two boards, which will become the major parts of a test stand for pixel detector bench and beam tests.

I. Introduction

BTeV's pixel detector consists of 31 double-plane stations of about 100 cm² of active detection area. These planes are perpendicular to the direction of the beam. The beam passes through the center of each plane formed by two halves. One of the half planes is shown in Figure 1. Since BTeV will use the pixel detector as part of the lowest level trigger system, one of the most important requirements is hit readout speed [1]. The primary goal is to achieve a data transfer rate capable of handling the hit rate generated by Fermilab's Tevatron beam with a luminosity of $2 * 10^{32}\ p/cm^2$ and a bunch crossing (BCO) time of 132 ns. Furthermore, the required readout bandwidth must be achieved while keeping a small power and mass budget. In particular, mass is very critical for the Pixel Detector, the most inner part of BTeV's detector where multiple scattering must be minimized.

A fiber optic based design, as proposed in this paper, is the technology that best adapts to BTeV's requirements. Every pixel plane will generate up to 16 Gb/s of data. The pixel amplifier and discriminator chips, located underneath the pixel detectors will store that information. However, since the pixel detector is the primary component of BTeV's trigger, the data must be readout as soon as possible. A multi chip module (MCM) design is being proposed for the pixel detector electronics as shown in Figure 1. Every module is autonomous. It groups a certain number of Pixel amplifier/discriminator chips and the readout electronics to transfer the data from the pixel planes to the trigger processor and DAQ. Furthermore, every module must allow for an incoming link to receive commands to initialize and control the pixel devices and provide them with timing information (i.e. clocks). A second approach under consideration moves the Pixel Detector Fiber Optic components 25 cm away of the MCMs. The advantage here is that the optoelectronics, and specially, the serializers and decoder chips receive much less radiation. Furthermore, it decreases the amount of mass in the active region.

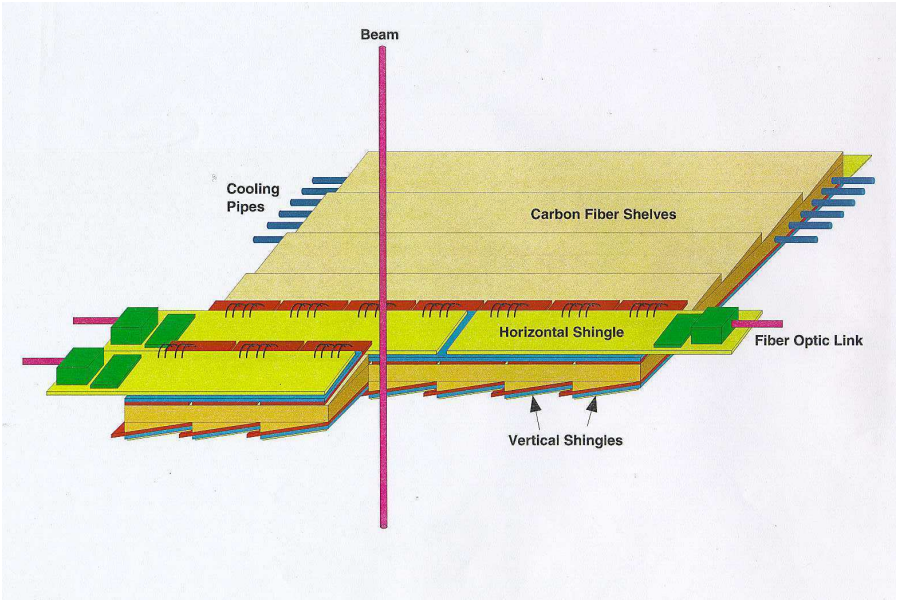


Figure 1: BTeV's Pixel Detector Plane

II. The Control and Readout Optical Link Prototype

A Control and Readout Optical Link prototype has been designed with the following purpose:

- Test optical transmission and reception issues such as dynamic range, noise, biasing, bandwidth, optical power, etc.
- Test the bi-phase mark encoded signal concept for the FPIX pixel chip [2] initialization and control link.
- To provide a good step toward the system integration of BteV Pixel Detector's.

The Optical Link Control and Readout prototype is organized in such a way that builds up a test stand for Pixel Detector Modules. Figure 2 shows a block diagram of the system.

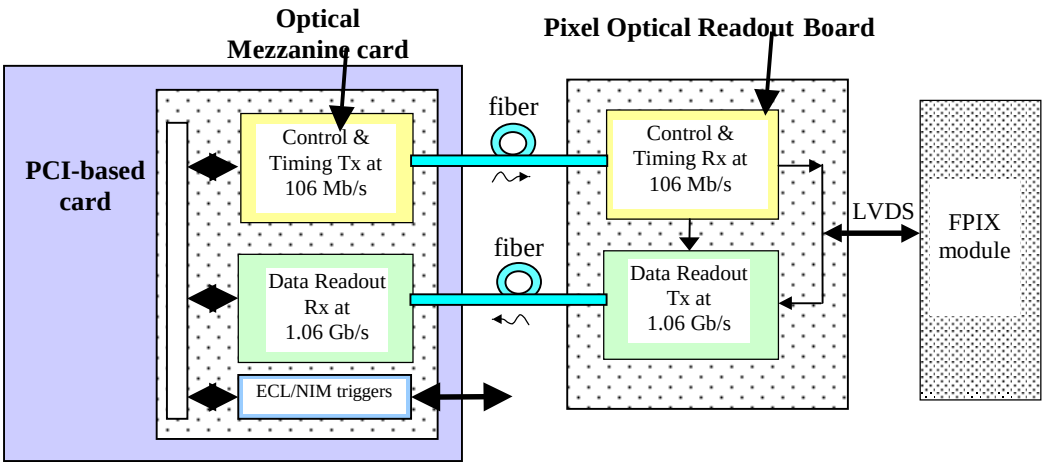


Figure 2: Two board Control and Readout Optical Link prototype

III. The Control Optical Link

The Control Optical Link carries initialization, control and timing information for the Pixel chips. The encoding used for this link is of bi-phase mark type. A 53 MHz clock modulates the initialization and control data in order to reduce the total number of fibers and provide an electrically balanced transmission. The bi-phase mark encoding guaranties at least one transition per bit reducing synchronization problems at the receiving end. As shown in Figure 3, the receiver uses a Phase Lock Loop (PLL) to recover the clock and data. The PLL must serve the double function of recovering the clock and reduceing the jitter. The Command interpreter decodes the serial information. Commands are of two different types, the ones used to initialize pixel cell and chip parameters and others to control or reset the FPIX chip in running mode. The commands are decode by the Command Interpreter and sent to the MCM as LVDS signals.

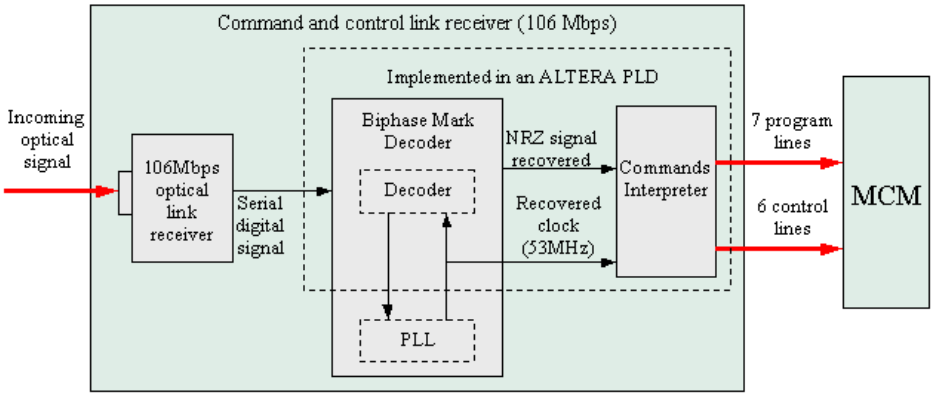


Figure 3: Control & Timing Receiver block diagram

The Control link receiver utilizes a Mitel 1A354 PIN photodiode operated in photovoltaic mode, connected to a high speed amplifier and discriminator as shown in Figure 4. The peek optical power in the fiber is 1mW. The PIN output signal is about 90mV and the output of the amplifier is 370 mV. Figure 5 shows scope images of the optical eye pattern and the bi-phase mark signal decodification at the receiving end. The amplifier used is high bandwidth allowing for a rise and fall time of about 1.5 ns. The PIN's response is very linear up to at least 1.5 mW.

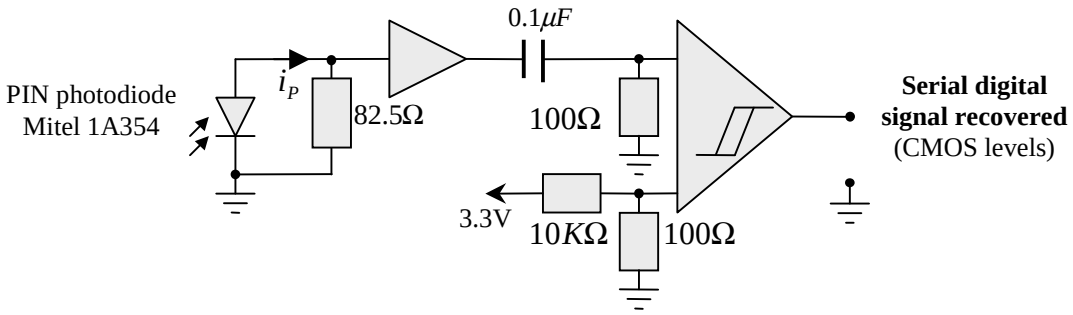


Figure 4: PIN, amplifier and discriminator

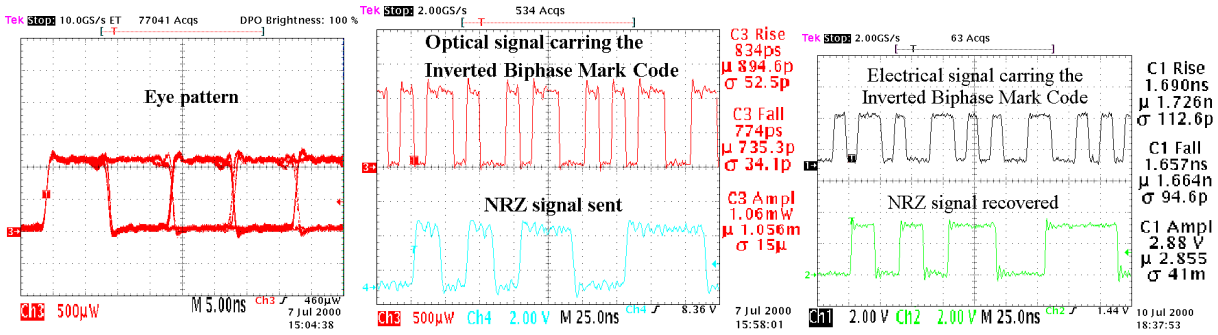


Figure 5: 53 MHz link signals: a) Eye pattern, b) NRZ-bi phase sent, c) NRZ-bi phase received

A strong constraint on the recovered clock is jitter, because the clock is used to readout pixels and to clock the Gigabit serializer. Gigabit serializers multiply the input clock frequency by 20 but they are unable to reject jitter. A small jitter may represent a big percentage of the output data's period, increasing the bit error rate in the channel. As it can be appreciated in Figure 6a, the jitter of the recovered clock in the present board is very low, about 64 ps peek-to-peek. The bit error rate of the channel has been measured to be better than 10^{-14}. Figure 6b shows the signal rise and fall time of the clock to be around 1.05ns.

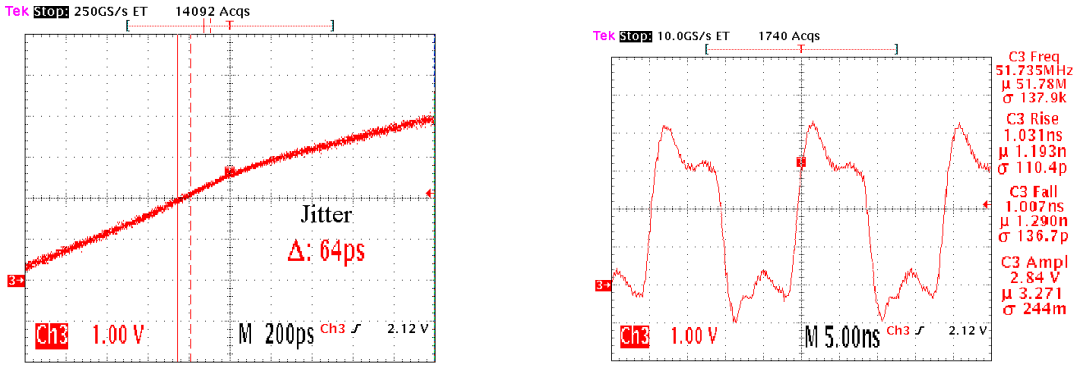


Figure 6: a) Clock's jitter, b) Clock's rise and fall time

IV. The readout optical link

The readout electronic serializes the data from the 5-chip Pixel Module into a G-Link based serial link operating at 1.06 Gb/s. In the final design the G-Link will be replaced by a radiation hardened serializer [3]. Alternative approaches are also being analyzed to relocate the optoelectronics. Extending the LVDS signals from the FPIX module to about 25 cm will allow us to place the optoelectronics outside the high radiation area. Performance of the G-Link has already been reported in [4].

V. Integration of the optical links to the readout of a pixel module

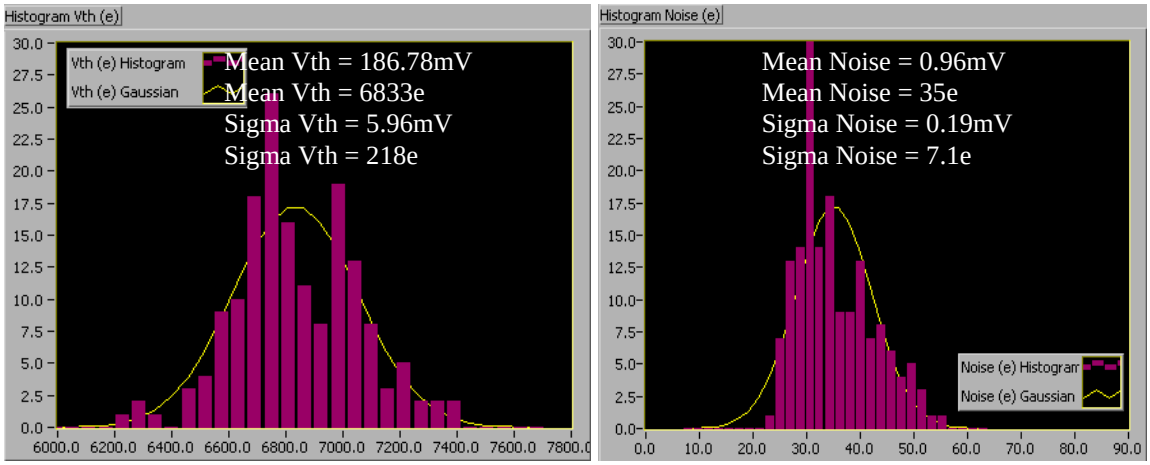
As shown in Figure 2 the optical links will be used to initialize and deliver commands and clocks to the Pixel chips as well as to readout the pixel data. BTeV Pixel Detector chip characterization has been extensively carried out at Fermilab and is reported elsewhere [5][6]. However, the optical links were integrated with the existing pixel assemblies. Several comparison tests were run using a single FPIX chip and a MCM with 5 pixel devices. Figure 7 shows the current setup.

Figure 7 Control and Readout Optical Link prototype setup

Table I compares mean and sigma of noise and threshold of a five-chip FPIX module using two different setups. In the first experiment, the MCM was controlled by a probe station and the data was stored directly into a logic state analyzer. The FPIX initialization patterns were generated by a pattern generator, whose outputs were directly connected to the MCM inputs. In the second case, the initialization and control data is provided through the Control Optical Link at 52MHz and the data is readout through the 1.06 Gb/s optical link. Figures 8 and 9 show the comparative histograms of noise and threshold for both tests.

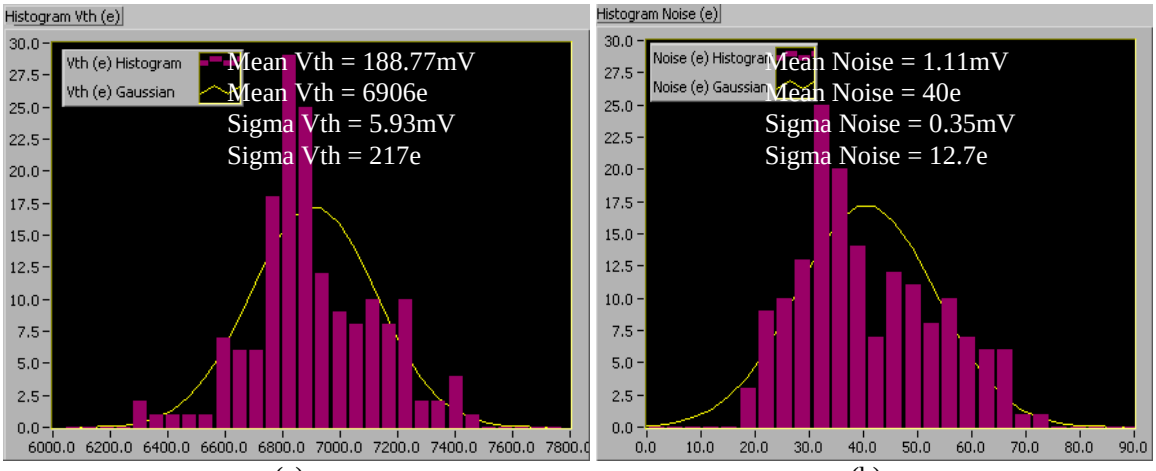
Vth0 = 1.95V	**Results of the characterization of the MCM without Optical Link**				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6833	6657	6581	6792	6956
Sigma threshold (e-)	218	239	217	168	146
Mean noise (e-)	35	37	37	31	31
Sigma noise (e-)	7.1	8.1	9.0	5.9	6.2
Vth0 = 1.95V	**Results of the characterization of the MCM with Optical Link**				
	Chip 1	**Chip 2**	**Chip 3**	**Chip 4**	**Chip 5**
Mean threshold (e-)	6906	6886	6820	6910	7051
Sigma threshold (e-)	217	184	179	142	161
Mean noise (e-)	40	37	38	32	30
Sigma noise (e-)	12.7	13.5	12.9	9.6	9.6

Table I MCM characterization comparison



(a) (b)

Figure 8: Five FPIX1 MCM without using the optical links. a) Threshold distribution and b) Noise Distribution.



(a) (b)

Figure 9: Five FPIX1 MCM using the optical links. a) Threshold distribution and b) Noise Distribution.

VI. Conclusions

A 5 chip FPIX1 Pixel Detector Multichip Module has been integrated to be controlled and readout through fiber optics. The first prototypes have proved to have an excellent performance. The readout clock has been recovered from the bi-phase signal with only 65 ps of jitter. This noise is acceptable for clocking a high-speed serializer at 1.06 Gb/s. The BER of the 106 MB/s link is better than 10^{-14}. EMI and radiation tests will define the location of BTeV's optoelectronics.

References

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