

Production database for the ATLAS–SCT front–end ASICs

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Abstract

The ATLAS–SCT will soon enter into the production phase. The large amount of electronic ASICs to be handled requires a well defined procedure both to monitor the performance of the production and to trace the distribution of the components down to the individual module level. That involves not only the development of a testing policy and method for the ASICs, with the corresponding criteria defining the pass/fail tagging of the chips, but also a mechanism to handle the substantial amount of data generated in this process.

This paper covers and discuss those aspects of the production and will report on the approach followed by the ATLAS–SCT towards the design of a testing procedure and the development of a production database.

I. INTRODUCTION.

The paper covers the main aspects of the ATLAS–SCT approach towards the definition of a production database. There are some key aspects that deserve some thought.

The first step is the definition of the test procedure. That involves the definition of what is to be measured and the coverage of those measurements. In the end, one needs to know the yield and to tag the ASICs as usable or not. The extreme operation conditions of the devices and the required performance of the detectors call for very exhaustive tests on the ASICs, whose complexity propagates into the level of complexity of the tests to be performed and the amount of data to handle. Those requirements are very specific to ASICs and demand much more than a simple good/bad analysis. Schedule is another constrain that forces, somehow, the philosophy of the measurements. Ideally, one would like to measure everything, regardless of the results of previous tests, in order to have a clear picture of the failure pattern. However, if time constrains are too demanding one

would need to make exclusive tests and stop the measurements as soon as one failure occurs.

The second aspect is that related to data handling. Once the tests have been performed a decision has to be taken on what to do with the data and to which extent the measured parameters can be used afterwards. It has to be understood that from the point of view of a production data base, the key issues are the production monitoring and the chip distribution, but also the possibility of having ready the relevant information for the beginning of the experiment.

In the following sections we describe the approach we follow for the ATLAS–SCT front–end ASICs, namely, the ABCD chip.

II. THE ABCD CHIP.

The Atlas Binary Chip (ABCD [3]) design is a single chip implementation of the binary readout architecture for silicon strip detectors in the ATLAS Semiconductor Tracker [1]. The Radiation Hard DMILL technology [2], in which the ABCD chip is fabricated, offers the unique possibility of combining a bipolar front–end amplifier/comparator with the CMOS logic in a single chip.

A description of the chip functionality can be found elsewhere [4] and here we only mention that it has 128 channels, a number of DACs to control its behavior and a set of tools that allow to test the most important blocks.

III. TEST PROCEDURE.

The ABCD chips will be assembled on the hybrids as unpacked devices and, in consequence, the chip preselection and characterization process has to be carried out at the level of wafer screening. The characterization process needs to be complete, accurate and as fast as possible since about 50000 good chips need to be preselected. As the ABCD chip employs the binary architecture, a considerable amount of measurements are needed to obtain any information on

the analogue performance of the front-end. Also a complete set of digital tests proving the readout protocol, different modes of operation and functionality of the whole logic, together with the characterization of the on-chip digital to analogue converters (DAC), need to be designed and carried out. A detailed description on the test setup and the tests performed can be found in [5]. In the following subsections we will very briefly describe them in order to be able to extract the sort of data that we can get.

A. Test setup.

The setup, as sketched in Fig. 1, is based on a Karl SUSS PA200-II probe station with a fully motorized chuck stage whose movement is totally controlled through the GPIB interface.

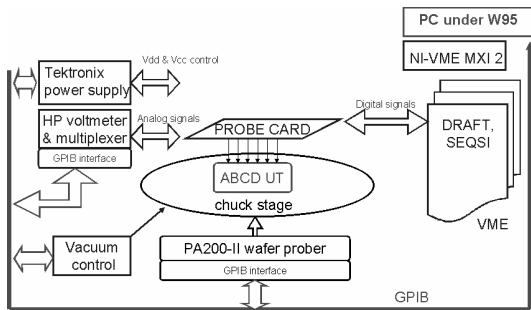


Figure 1. Schematic diagram of the wafer test system.

Data acquisition and chip control are based on two VME modules [6], one providing the clock and the commands to the chip (SEQSI) and a data receiver and decoder (DRAFT).

For DAC measurements we used a HP voltmeter with an analogue multiplexer which is also used to monitor the vacuum that sucks the wafer on the chuck. The supply voltages, Vcc and Vdd, for the chip are controlled by a TekTronix power supply that also measures the current drawn by those lines at different chip states. Both, the digital signals, like clock and commands, and the analogue signals are driven by a

custom designed PCB. The whole system was driven by a dedicated program written in C++ and running under W95.

The system takes on the order of four minutes to perform all the tests in a single chip. The average total time to screen a whole wafer is about 20 hours, given the current yield.

B. Digital tests.

A number of tests are made to check the digital functionality of the chips. The main characteristics are connected to chip control, inter-chip communication and data compression. Additionally, some functionalities like channel masking and redundancy mechanisms should be proven. Fig. 2 shows schematically the tests carried out. Only the tests concerning configuration and addressing are considered as exclusive, for which a failure directly tags the ASIC as unusable. The rest of the tests are all performed regardless of the results of the previous ones.

Another key issue to determine with the results of the digital tests is the speed margin of the devices. Due to the limitation on the maximum clock frequency provided by the setup, the chip degradation is simulated by scanning Vdd together with the available clock frequencies (40 MHz and 50 Mhz) for every digital test.

C. Power consumption and DACs.

The ABCD has four main digital to analogue converters: two of them control the threshold, the first globally and the second on a channel by channel basis, and another two control the shaper and preamplifier biases. For any of them a full scan of all the DAC bits is performed, allowing to determine their linearity. There is a fifth DAC to control the amplitude of the calibration pulse, but a failure on that one will translate into problems on the analogue tests, to be described later.

Also the power consumption of the devices is measured, both in the analogue and digital lines, with different chip configurations: master and slave. In order

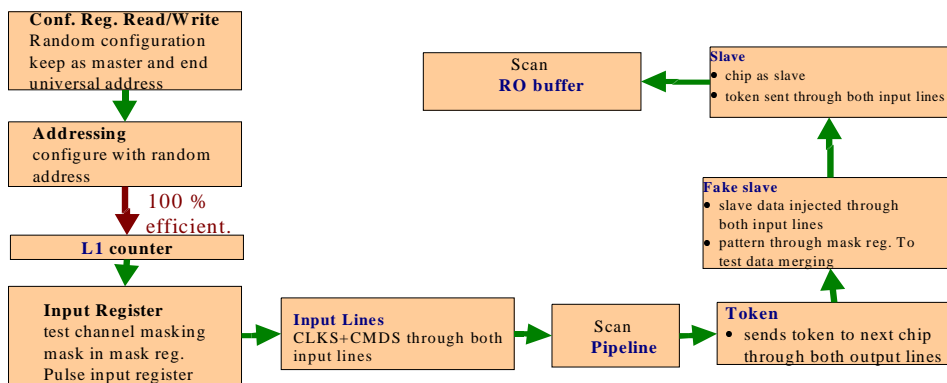


Figure 2. Sketch of the digital tests performed on the chip during the wafer screening. All the aspects of the digital block are covered, ranging from configuration and addressing to the performance of the pipeline and readout buffer.

Table 1: List of information tokens that can be obtained with the ABCD wafer screening setup.

Wafer	Chip				Channel
	Position	Digital	Analogue	DACs	
Batch	X	Flag	Ndead	ThrsNonLin	Flag
ID	Y	40 Mhz	NonTrim	ThrsSlope	Gain
Yield		Vdd40MHz	Gain	ThrsOffset	Offset
		VddConf	GainSpread	PreamNonLin	Noise
		VddAddr	Offset	PreamSlope	Efficiency
		VddL1Cnt	OffsetSpread	PreamOffset	TrimSlope
		VddInpResg	Efficiency	ShaperNonLin	TrimOffset
		VddInpLin	Noise	ShaperSlope	
		VddFakeS		ShaperOffset	
		VddSlave			
		VddToken		TrimRange	
		50 Mhz			
		Vdd40MHz			
		VddConf			
		VddAddr			
		VddL1Cnt			
		VddInpResg			
		VddInpLin			
		VddFakeS			
		VddSlave			
		VddToken			
		P.C	P.C		
		MasterCurrent	MasterCurrent		
		SlaveCurrent	SlaveCurrent		

to simulate the nominal requirements for the ATLAS–SCT occupancy and L1 trigger rate, the measurement is made with a trigger rate of 100 kHz and an occupancy of 3%, built up with randomly selected channels. The distribution of the power consumption in a wafer for both lines and chip configurations is shown in Fig. 3.

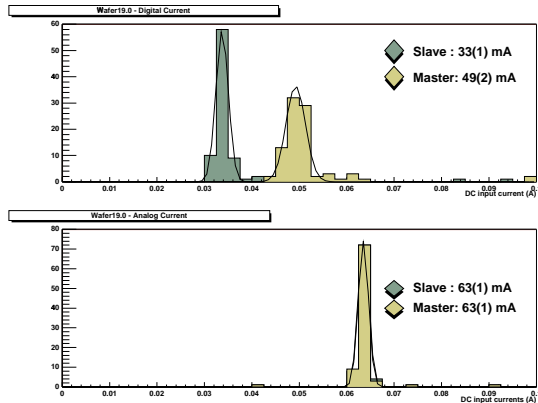


Figure 3. Spread of the power consumption in a wafer as measured both in the digital and analogue lines with different chip configurations: master and slave.

D. Analogue tests.

The main goal of these tests is to determine the basic analogue parameters of the front–end: gain, noise and discriminator offset spread. To this end, a threshold scan for three different input charges, delivered by the calibration circuitry, is done for every channel in each chip, as described in [5,7]. The input transistor current and the shaper bias are set to the nominal values and the chip is driven by a 40 MHz clock. The s–curves obtained from the scan are fitted to a complementary error function. The response curve is built from the 50% points of the fit and from it the gain and offset are

derived. The noise is taken directly from the fit and the s–curve plateau gives the chip efficiency, that provides information on possible defects in the pipeline.

E. YIELD.

As already mentioned, the complexity of the devices and, accordingly, of the tests to be carried through, as imposed by the desired performance of the ATLAS detectors, results in a huge amount of information to be handled. Table 1 shows the smallest information tokens that can be obtained from the setup. In order to estimate the yield of the process all that information has to be combined, according to a well defined criteria.

Fig. 4 shows the variation of the digital and total yield, at 40 MHz and 50 MHz, as a function of Vdd and for different levels of strictness, that is, accepting zero, one or two defects at most. In order to quote a number for the final yield we always select the most unyielding situation: only chips with no defects or dead channels are considered.

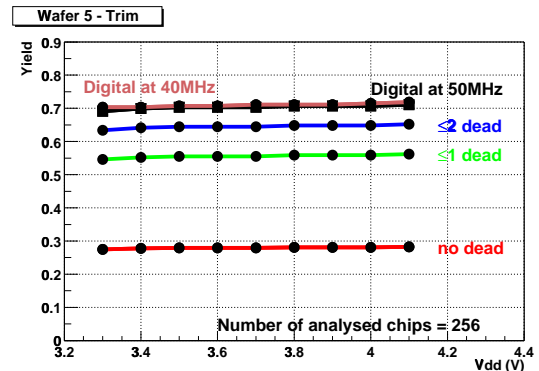


Figure 4. Variation of the yield with respect to the applied Vdd in the digital tests and different levels of strictness.

IV. A PRODUCTION DATABASE.

Having defined the behavior of the data producer, that is, the test procedure, the next major point is how to define the data holder or, in other words, the production data base. The main goals of a production data base could be classified in two groups. The first is defined by the data needs at the beginning of the experiment, while the second is driven by the production phase.

Of paramount importance is the centralization of the data, in an agreed format, and having all that information available at the beginning of the experiment. In that context two groups could be identified. First, the off-line data, concerning aspects like the alignment and dead channels, that would allow for a fast start of detector data analysis. Second, the monitoring of the system, which would handle aspects related with the performance of the system and its components. In the case of binary front-end ASICs that would involve information on gain, threshold values and nominal settings for operation.

Of equal significance are all the aspects covering data handling: availability, insertion and retrieval of information during the production phase. For that, the cleanest solution is the definition of a WWW-based user interface that would hide all the complexities of the database server and protocol.

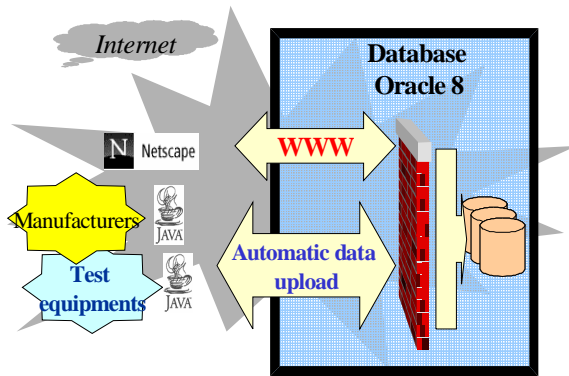


Figure 5. Scheme of the ATLAS-SCT production database functionalities.

A. SCT production database.

The architecture proposed for the ATLAS-SCT database is based on the client-server model, with a main ORACLE© version 8 server set in Geneva on a dedicated Sun server. Access is granted from client machines communicating over the network, either by means of special data-entry applications, like the OMNIS-based developed in Manchester [8], or WWW browsers, like the one developed in Geneva [9,10]. The principle for the two interfaces is the same and only the layout may change. The access is secure and an institute-based authentication mechanism has been implemented. In the OMNIS approach a subset of the data is stored in a local cache data-file, and periodically

merged with the master server over the network. The web solution provides direct access to the master server for consultation, insertion, deletion and update. When mass data and raw-data need to be entered, the Java application, also developed at Geneva, is used, allowing for any kind of data to be upload in an automatic way.

The data in the DB is organized hierarchically, see Fig. 6, starting from the building blocks, items, that group into what is called an assembly, which in turn can be assembled to form bigger assemblies. Any object has associated a unique identifier and some specific fields. Associated with those objects is a data structure, containing the list of tests, together with their results, performed on each item of the assembly. For the ABCD chip, one could have the tests made on the wafer, the ones made on the hybrid (an assembly) and then the tests performed on the module itself (another assembly).

Also attached to any object of the database is the information concerning the shipment and location of those objects.

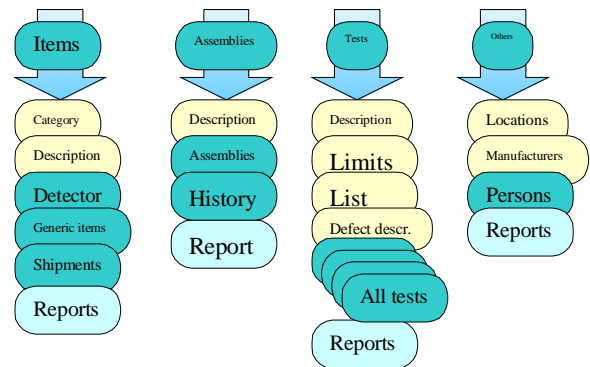


Figure 6. Data organization in the ATLAS-SCT database.

B. The ABCD in the SCT database.

The ABCD enters in the database as an item, with its associated tests and defects. The data structure should be general enough to include any of the tests. It includes, see table 2, the minimum Vdd at full efficiency for the scanned clock frequencies, the power consumption, the settings (Vcc, Vdd, shaper bias and input transistor current) and some general properties like the gain, offset, noise and the slopes and offsets of the DACs. One could, eventually, add some information on irradiation tests, like the total dose received or the irradiation type.

Together with the chip characteristics as a whole, some information in a channel by channel basis is also stored. That would include the channel gain, offset, mask and trim dac value for a nominal trimming at 1fC. These data would constitute the starting point for the system monitoring in the starting phase of the experiment and would also provide the initial settings of the chips.

Table 2. ABCD data structure in the ATLAS–SCT production database.

TSTABCD			I_VCC	NOT NULL	NUMBER(10,4)	Defects		
Name	Null?	Type	I_VDD	NOT NULL	NUMBER(10,4)	Name	Null?	Type
			DELAY_DELAY	NOT NULL	NUMBER(10,4)			
DOSE_GAMMA		NUMBER(10,4)	PR_BIAS	NOT NULL	NUMBER(10,4)	DEFECT_NAME	NOT NULL	VARCHAR2(20)
DOSE_NEUTRON		NUMBER(10,4)	SH_BIAS	NOT NULL	NUMBER(10,4)	TEST_NO	NOT NULL	NUMBER(11)
CHIP_CFG	NOT NULL	VARCHAR2(3)	THRESHOLD_1FC	NOT NULL	NUMBER(10,4)	CHAN_1ST	NOT NULL	NUMBER(11)
CHIP_CFG_VDD40		NUMBER(10,4)	GAIN	NOT NULL	NUMBER(10,4)	CHAN_LAST	NOT NULL	NUMBER(11)
CHIP_CFG_VDD50		NUMBER(10,4)	GAIN_SPREAD	NOT NULL	NUMBER(10,4)	LAST_MOD	NOT NULL	DATE
CHIP_HEAD1	NOT NULL	VARCHAR2(3)	IPRE_DAC_SLOPE	NOT NULL	NUMBER(10,4)	URL		VARCHAR2(200)
CHIP_HEAD1_VDD40		NUMBER(10,4)	IPRE_DAC_OFFSET	NOT NULL	NUMBER(10,4)	OWNER	NOT NULL	VARCHAR2(30)
CHIP_HEAD1_VDD50		NUMBER(10,4)	IPRE_DAC_LINEAR	NOT NULL	NUMBER(10,4)			
CHIP_HEAD2	NOT NULL	VARCHAR2(3)	ISH_DAC_SLOPE	NOT NULL	NUMBER(10,4)			
CHIP_HEAD2_VDD40		NUMBER(10,4)	ISH_DAC_OFFSET	NOT NULL	NUMBER(10,4)			
CHIP_HEAD2_VDD50		NUMBER(10,4)	ISH_DAC_LINEAR	NOT NULL	NUMBER(10,4)			
CHIP_TOKEN	NOT NULL	VARCHAR2(3)	TH_DAC_SLOPE	NOT NULL	NUMBER(10,4)			
CHIP_TOKEN_VDD40		NUMBER(10,4)	TH_DAC_OFFSET	NOT NULL	NUMBER(10,4)			
CHIP_TOKEN_VDD50		NUMBER(10,4)	TH_DAC_LINEAR	NOT NULL	NUMBER(10,4)			
CHIP_INP1	NOT NULL	VARCHAR2(3)	TEMPERATURE		NUMBER(10,4)			
CHIP_INP1_VDD40		NUMBER(10,4)	LAST_MOD	NOT NULL	DATE			
CHIP_INP1_VDD50		NUMBER(10,4)	OWNER	NOT NULL	VARCHAR2(30)			
CHIP_INP2	NOT NULL	VARCHAR2(3)	TEST_NO	NOT NULL	NUMBER(11)			
CHIP_INP2_VDD40		NUMBER(10,4)						
CHIP_INP2_VDD50		NUMBER(10,4)						
CHIP_MASTER	NOT NULL	VARCHAR2(3)	TSTABCDchs					
CHIP_MASTER_VDD40		NUMBER(10,4)	Name	Null?	Type			
CHIP_MASTER_VDD50		NUMBER(10,4)						
CHIP_SLAVE	NOT NULL	VARCHAR2(3)	CHAN_NUM	NOT NULL	NUMBER(3)			
CHIP_SLAVE_VDD40		NUMBER(10,4)	GAIN	NOT NULL	NUMBER(10,4)			
CHIP_SLAVE_VDD50		NUMBER(10,4)	OFFSET	NOT NULL	NUMBER(10,4)			
BIN_NUMBER		NUMBER(1)	T_DAC	NOT NULL	NUMBER(10,4)			
Q_FACTOR	NOT NULL	NUMBER(10,4)	MASK_SET	NOT NULL	VARCHAR2(3)			
VCC	NOT NULL	NUMBER(10,4)	LAST_MOD	NOT NULL	DATE			
VDD	NOT NULL	NUMBER(10,4)	OWNER	NOT NULL	VARCHAR2(30)			
			TEST_NO	NOT NULL	NUMBER(11)			

V. CONCLUSIONS.

In the ATLAS–SCT we have developed the two tools needed for the definition of a production data base: the data producer, that is, the test procedure on the ASICs, and the data holder.

The system is able to test all the ABCD functionalities, performs fast and accurately, provides all the information needed to tag the chips and has been successfully used up to now. It provides enough information to feed our production database as currently defined. Certainly some information is kept outside the database and it is not yet decided whether the current implementation of the ABCD item in the database needs to be extended or not. Also subject to discussion is whether all the chips will enter in the database or only those that will be used to build the models.

Concerning the database itself, it has proven to be a powerful tool, fulfilling all the requirements concerning data availability, insertion and retrieval, not only for the ASICs, but for any of the building components of the detector, as already seen with the silicon detectors pre-series.

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