THE ATLAS PIXEL ON-DETECTOR ELECTRONICS

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Abstract

Large advances have been made over the last two years in the development of the front-end readout electronics for the ATLAS [1] Pixel Tracker [2]. I describe here the first phase of the Pixel *Demonstrator* programme which involved the production of two realistic ATLAS prototype readout-chips in radiation-soft technologies, along with the first Module Controller Chip. I will also describe the design of the first fully-functional FE-chip to be submitted to a radiation-hard foundry (Temic), which is currently being fabricated.

1. THE ATLAS PIXEL TRACKER

The Inner Detector of ATLAS will be composed of semiconductor-based discrete tracking elements with both strip and pixel geometries. The volume closest to the ***pp*** interaction region will be occupied by the Pixel Sub-system since the degree of granularity given by two-dimensional segmentation is most suited to the track densities and radiation levels encountered therein.

In Figure 1 the positioning of modules within the Pixel Tracker is depicted. There are three concentric barrel layers at 4.15, 9.7 and 12.7cm in *r*, along with 5 disc structures in each of the forward regions. Each module, of which there are a total of 2228, comprises a single 16.4 X 60.8mm active-area sensor tile. A tile incorporates 46080 pixel implants with pitches of 50μm in $r\phi$ and 400μm in the *z*-direction. The innermost barrel layer or *B-layer*, differs from the rest of the system in that the *z* pitch is 300μm with 61440 pixels per module.

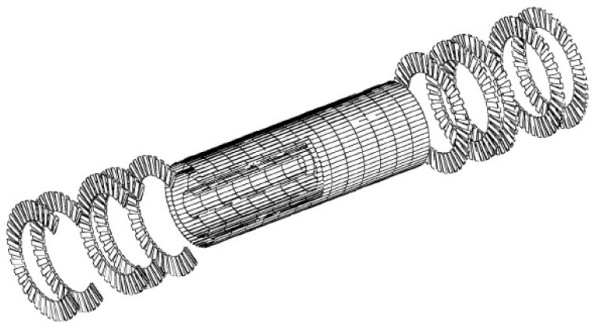

Figure 1: Module positioning in the Pixel Tracker.

Every individual pixel is DC-coupled to a preamplifier on one of the 16 front-end readout chips via a bump-bond. Each module is also instrumented with one Module Controller Chip (MCC), the primary purpose of which is to collect the hit data from the FE chips through 16 input FIFOs and to build up local `events' for subsequent serial transmission. The modules also have the optical transmission devices, local termination resistors, decoupling capacitors and a temperature-sensor integrated onto them.

2. MODULE INTEGRATION

There are two hybridization strategies incorporated in the ATLAS Pixel system. The flex-kapton approach is the baseline choice everywhere except for within the B-layer where a technique known as MCMD is preferred. Modules constructed in both ways have been parameterised in laboratory and testbeam environments

2.1 Flex-Kapton Hybridization

Figure 2 shows schematically a flex-hybrid module. The lowest layer is formed from the 16 FE-chips which have

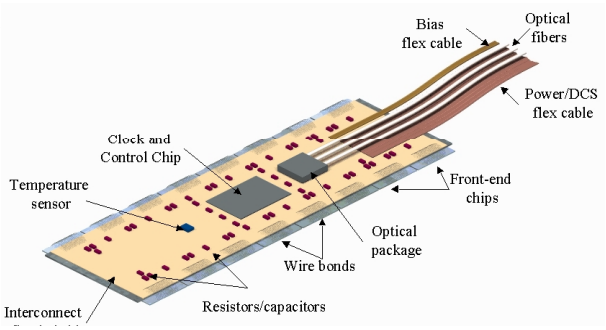

Figure 2: The flex-kapton hybrid concept.

their backplanes facing down and in thermal contact with the support structure. These are bump-bonded to the sensor tile which in turn has a single kapton bussing piece glued on to its backplane.

Along the long edges of the module the 16 FE chips (8 each side) protrude such that they may be connected up to the top surface of the hybrid using conventional wire bonds. These connections provide the necessary power, clock and control signals along with the output data link towards the MCC which is located in the centre of the hybrid. Connections between the MCC and bussing on the hybrid are also made with wire bonds.

2.2 MCMD Hybridization

In the MCMD (Multi-Chip-Module-Direct) scheme the necessary bussing is directly fabricated on the active side

of the detector surface. This is a post-production lithographic process providing up to 5 layers of copper with BCB dielectric. An individual via is crafted for each pixel to connect it electrically to the top surface of the sensor where solder or Indium bumps form the bond to the readout electronics. This enables the pixel connections to *fan-in* hence all pixels may have the same geometry whilst providing complete coverage in the inter-chip gaps. In the flex-hybrid scheme these gaps are covered by stretching the outer column implants by 50% and including eight extra rows of pixels which are *ganged* with other pixel rows. Avoidance of the extra channel occupancy and hit ambiguities implied by this approach is particularly beneficial in the B-layer.

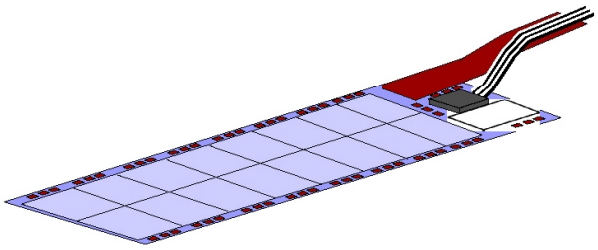

Figure 3: MCMD scheme.

3. THE DEMONSTRATOR PROGRAMME

The aim of the Demonstrator Programme was to develop on-detector readout-electronics designs which addressed all of the requirements of ATLAS. The initial phase of the programme resulted the development of two separate front-end chips and an MCC, which although conceived for radiation hard processes, were realised at non-radiation hard foundries.

The first of the front-end chips, FE-A, was designed at CPPM and Universität Bonn and fabricated using the BiCMOS process of AMS. The front-end of FE-A was based upon bipolar transistors although a 100% CMOS version (called FE-C) was later produced. The design of the other chip, FE-B, was developed at the Lawrence Berkeley Laboratory and this was manufactured by HP. The group at INFN, Genova were mostly responsible for the synthesis of the MCC design which was also fabricated at AMS.

To date more than 60 single-chip assemblies and 10 electrically-functional modules have been constructed using this first wave of electronics chips. These have been studied extensively in the laboratories of several collaborating institutes and during seven testbeam periods at CERN's SPS facility. All of the ATLAS specification issues (which are applicable to radiation-soft electronics) have been addressed with highly encouraging results. A number of the single-chip devices were equipped with irradiated sensors in order to study the effects of worst-case leakage-current for example on aspects of the front-end performance.

The two front-end design efforts later joined forces to combine all of the experience gained with radiation-soft chips into a common layout which is currently being realised in Temic's radiation-hard DMILL process, with the first wafers expected in the middle of October '99.

4. MODULE CONTROLLER CHIP (MCC)

Figure 3 shows the basic block diagram of the MCC. A Front-End Port consists of the drivers for all of the digital signals which configure and operate the FE chips along with sixteen receivers for the returning data streams.

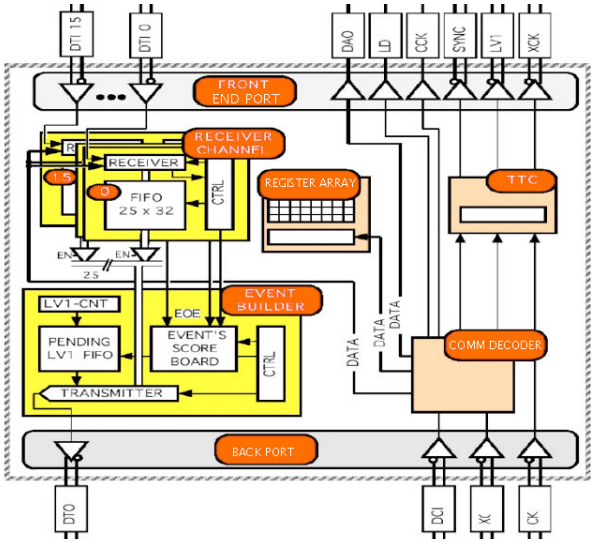

Figure 4: MCC block diagram.

For each FE chip there is a 25-bit-wide FIFO which buffers up to 32 hit words at a time. The event builder samples these FIFOs, one level-1 trigger at a time and builds up a score-board of hits for the whole module. All of the data for the trigger is then serialised off the chip as an integrated `event'. The other blocks shown in the diagram are the register array which stores the configuration information for the MCC and the command decoder which samples the input data line and distinguishes *fast* commands such as triggers from *slow* configuration-type commands. The chip is also designed to seek certain errors associated with the FE data and transmit the information as part of the general output-data protocol. The current MCC incarnation also operates in a *transparent mode* which enables individual FE chips to be read-out in direct stand-alone mode, i.e. not relying on the MCC event-building machinery.

5 DEMONSTRATOR FRONT-END CHIPS

5.1 Requirements

Potential sources of hit-inefficiencies in the Pixel System include bump-bond defects, timewalk, deadtime, charge loss through sharing and crosstalk, along with general electronics channel failures etc. Taking all of these into account, an overall hit-efficiency of better than 97% is specified. The false-occupancy is not to exceed 10^{-5} channel^{-1} trigger^{-1}.

Following 10-years of operation, it is anticipated that the Inner Layer will have been subjected to a hadronic fluence which, in terms of NIEL, is equivalent to 10^{15} 1MeV neutrons cm^{-2}. The consequence of this for the sensors is that at the design operation-bias-voltage of 600V, the expected energy-deposition for 1MIP will be significantly reduced compared with the non-irradiated case. The electronics chips, themselves compromised by an ionising-radiation dose of 250kGy, must maintain sensitivity to these smaller signals whilst being immune to increases in leakage currents of up to 30nA per pixel implant. The spatial resolution in $r\phi$ is to be as high as possible given the constraints arising from bump-bonding and electronics-layout issues. The power consumption is not to exceed 40μW per pixel.

5.2 Design Features

In each FE-chip, 2880 channels are arranged into 18 column by 160 rows. The input receivers and output drivers are LVDS for all of the digital signals. Serial 5MHz-configuration-command and 40MHz output-data protocols are implemented in order to minimise the number of required connections.

The chips have integrated DACs providing the necessary biases for the analogue front-end circuitry. Each channel is equipped with its own 3-bit DAC for channel-to-channel threshold adjustments, thus a means of overall dispersion reduction is provided. All of the demonstrator chips have 7-bit charge measurement capability using time-over-threshold (TOT), taking advantage of the available deadtime per pixel (~2μs excepting the B-layer). Also featured is a global hit-OR (*hitbus*) which provides for a means of self-triggering operation. This is particularly useful when using γ–sources for absolute calibration determination.

A 2880-bit pixel register plus one corresponding latch per channel enable individual pixels to be masked-off for (independently) calibration-strobing and readout.

The charge-sensitive preamplifiers of both FE-A/C and FE-B feature a DC feedback scheme with a tuneable current providing control over the shaping-time for a given input charge.

The front-end of FE-B differs from FE-A/C in that it features a dual-threshold discriminator. In operation the thresholds are set such that the faster of the two, (the *time*-discriminator), is lowest and is used to define the timestamps for the leading and trailing pulse-edges. For a hit to be tagged, the pulse must cross through the upper *level*-threshold, (which is optimised for noise occupancy and efficiency), before registering a trailing edge through the time-threshold. This scheme also provides improved crosstalk performance since the level-discriminator may be operated more slowly than in a single-discriminator design.

The readout-architecture implementations are also markedly different for the two designs. In FE-A/C each column-pair is served by an 80-bit 40MHz shift register to clock leading-edge (LE) and trailing-edge (TE) hit-information towards the end-of-column (EOC) circuitry. There the timestamps of the hits are determined from the row-number information along with the time-of-arrival at the EOC. Since the length of the shift registers is 80-bits only one LE or TE from a 4-pixel cell may be introduced for a given BCO. If extra hits are registered in a particular crossing then their information is held until the next available crossing and a 2-bit *late-field* is used to indicate the required correction to the hit age at the EOC.

In FE-B the global time information is distributed throughout the array to every pixel as 7-bit Gray-code. When a hit is tagged in a pixel cell the timestamps for the LE and TE are stored locally. Meanwhile a continuous *vertical-sparse-scan* operates along the column pairs seeking tagged hits. As soon as such a hit is seen, the geographical and timing information is sent directly to the 20 buffer-sets at the end of each column-pair.

In the EOC buffers any hits which match the present latency-corrected timestamp are deleted unless a corresponding trigger has been received. Received level-1 triggers are buffered in a 16-deep trigger FIFO. The presence of a record at the top of this FIFO initiates a two-dimensional *horizontal-sparse-scan* which looks through the EOC buffers for hits which are then serially transmitted from the chip at 40MHz. The TOT is calculated for each hit as the TE-LE time-difference prior to this, resulting in a 7-bit charge field in each 26-bit hit-word.

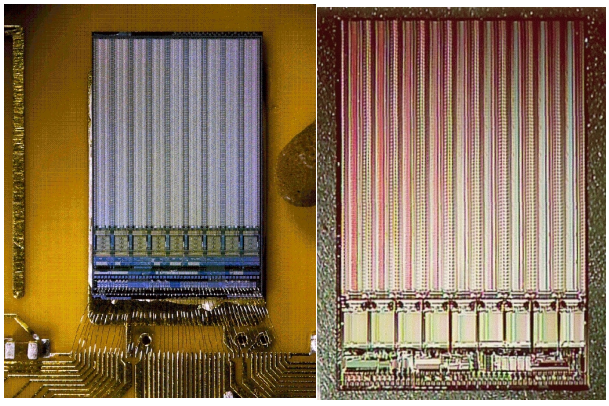

Figure 5: Photographs of FE-A (left) and FE-B.

6: LABORATORY STUDIES

6.1 Threshold-Dispersion and Noise

A standard assembly test procedure is to perform a scan of calibration-pulse amplitudes for all channels. Error-function fits to the derived *s-curve* histograms of efficiency versus charge yield estimates of the threshold and equivalent noise charge (ENC) when combined with the magnitude of the calibration capacitance.

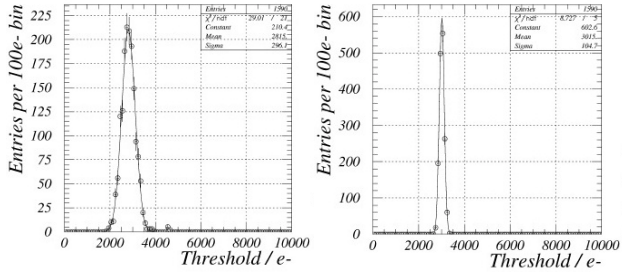

Figure 6: Effect of TDAC tuning on threshold dispersion.

In Figure 6 distributions of thresholds are shown before and after the 3-bit trim-DACs (TDACs) for each channel have been tuned in order to minimise the dispersion. An initial dispersion of 296e- for this single-chip assembly is reduced to 105e-. The mean threshold is around 3ke-

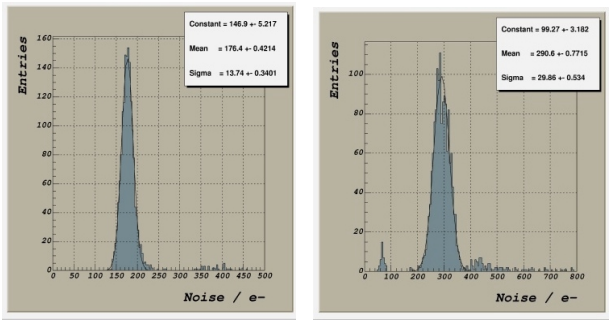

Figure 7: ENC for assemblies incorporating a non-irradiated baseline sensor(left) and an irradiated sensor.

which is a standard operating point for most of the laboratory and testbeam operations. Typically the initial dispersion for the demonstrator chips is in the range 250e- to 450e- when bump-bonded to the prototype sensors [3].
The leftmost plot in Figure 7 shows the distribution of ENC for an assembly incorporating the base-line sensor design. A mean value of 176e- is recorded. The other plot shows the same distribution for a FE-chip bonded to a sensor which has been irradiated to $1.0X10^{15}$ 1MeV neutrons per cm^2 NIEL-equivalent dose (i.e. 10-years inner-layer hadronic fluence). The ENC, now dominated by the sensor leakage current, is measured to be 291e-.

6.2 Timing-Dispersion and Timewalk

Many studies of the timing performance of the demonstrator chips have been performed in the laboratory. The lower plot in figure 8 shows three distributions of time for all channels of a single-chip assembly for injected charges of 5,000, 10,000 and 100,000e-. The

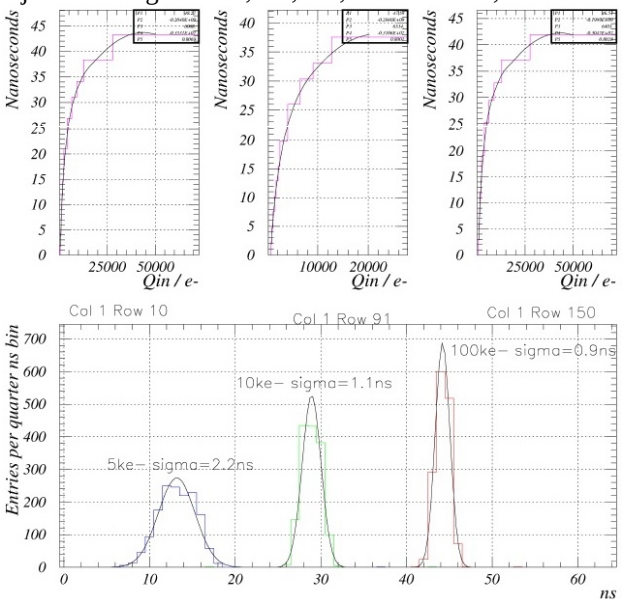

Figure 8: Time performance of a single-chip device.

width of the distribution at 10ke- is 1.1ns whilst that at 5ke- is 2.2ns. The relative position of the distributions on the x-axis illustrates the degree of timewalk over this range of input charge. The upper three plots show the timewalk curves (time vs. charge) for three individual channels. Overall the charge for which the timewalk is measured to be 20ns relative to 50,000e- is around 7ke- at 3ke- threshold.

6.3 Crosstalk

The crosstalk between neighbouring channels within a column is measured by injecting a very large range of charge into a particular channel whilst reading out only its two neighbours. An error function is fit to the resulting hit-count vs. charge histogram and the median value is used along with the known threshold of the particular channel to estimate the percentage charge loss. In figure 9 the crosstalk for a single-chip assembly incorporating the baseline sensor design is shown to be 2.0% which compares well with the 5% ATLAS specification.

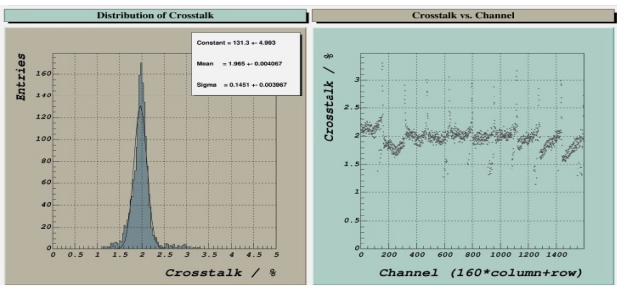

Figure 9: Crosstalk evaluation.

7. TESTBEAM EVALUATION

Detailed evaluation of demonstrator assemblies with irradiated and non-irradiated sensors [3] has been carried out during 7 running periods of the H8 testbeam at CERNs SPS facility. Efficiencies of 99% are typically recorded for the non-irradiated cases whilst a device with a sensor irradiated to the maximum 10-year fluence (for the inner layer) yielded 98.2% at a threshold of 3300e-. The charge measurement capability has enabled comparative studies of charge-collection efficiency (CCE) vs. position within a pixel cell to be performed for 2 generations of prototype sensor layouts. Figure 10 shows such a map of CCE for the baseline sensor design. The uniformity is excellent with only a very slight dip at the inter-pixel position corresponding to the location of the reach-through bias grid structure.

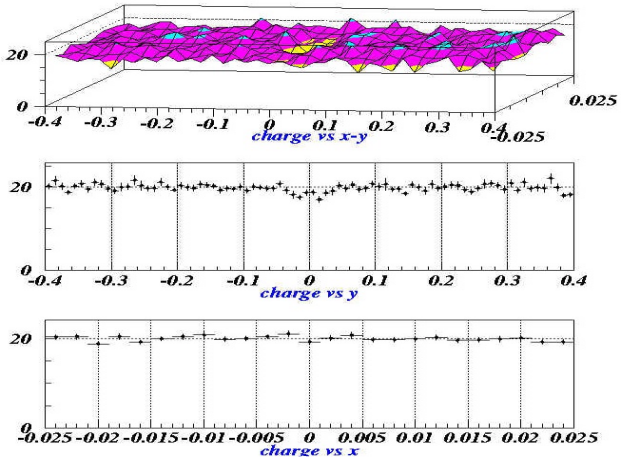

Figure 10: CCE for the baseline sensor design.

8. 16-CHIP MODULE EXPERIENCE

Figure 11 shows distributions of threshold and noise for a 16-chip module assembled using a first-prototype flex-

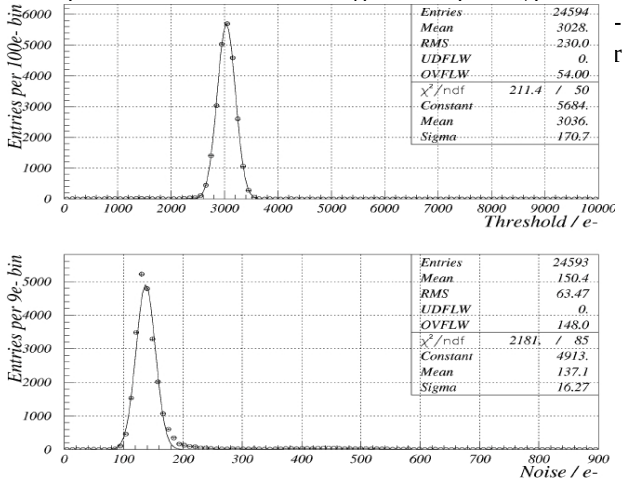

Figure 11: Threshold and noise distributions for a full 16-chip module.

noise performance than the baseline design. A threshold dispersion of 171e- is recorded, the ENC peaks at 136e-.
In figure 12 the efficiency for the 16-chips superimposed is plotted as a function of time. An overall efficiency of 99% is extracted from this.

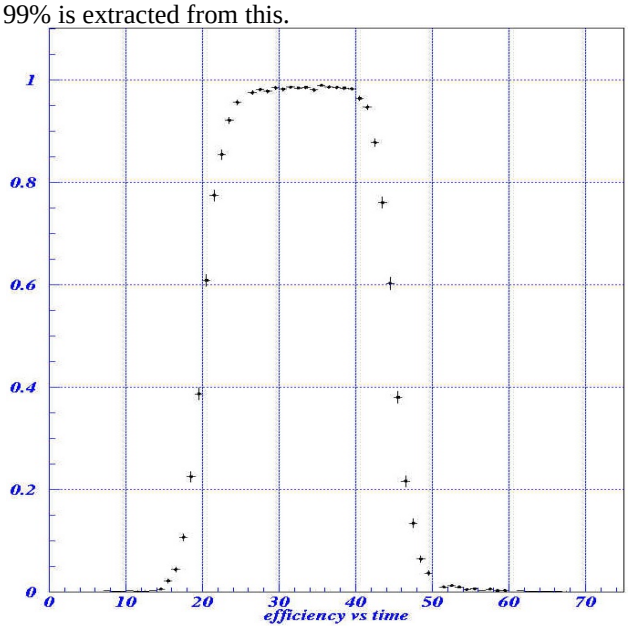

Figure 12: Efficiency vs. time for 16-chip module.

9. RADIATION HARD FE DESIGNS

The first radiation-hard design (FE-D) maintains the spirit of the demonstrator programme (i.e. pin-compatibility, same pitches etc.) and combines features of both FE-A/C and FE-B. The front-end design is based on that of FE-C. Constraints in pixel-cell space introduced by the DMILL process ruled out the possibility of the BiCMOS FE-A front-end being used along with that of FE-B. The digital readout architecture is derived from FE-B with some refinements, e.g. low-voltage swing signals for the column-pair readout bus' with sense amps at the EOC, (for reduced digital cross-coupling). The DACs are now formed from a 2D array of current mirrors for radiation tolerance. Plans are underway for a new system which will enable testing of digital operation at speeds of up to 100MHz in anticipation of the expected slowing of the logic arising from radiation exposure.

A design for the Honeywell SOI process (called FE-H) is also in preparation.

10. REFERENCES

[1] ATLAS Technical Proposal, *The ATLAS Collaboration.* **CERN/LHCC/94-43**

[2] Inner Detector Technical Design Report, *The ATLAS collaboration.* **CERN/LHCC/97-17**

[3] The ATLAS Silicon Pixel Sensors, *The ATLAS Pixel Collaboration.* **ATL-INDET-99-012** and submitted to **Nuc. Inst. Meth.**