RECENT DEVELOPMENTS ON THE SILICON DRIFT DETECTOR READOUT SCHEME FOR ALICE INNER TRACKING SYSTEM

G. Mazza, INFN Sez. di Torino, Italy (email: mazza@to.infn.it)
G. Alberici, INFN Sez. di Torino, Italy (email: alberici@to.infn.it)
G.C. Bonazzola, Università di Torino, Italy (email: bonazzola@to.infn.it)
V. Bonvicini, INFN Sez. di Trieste, Italy (email: bonvicini@tr.infn.it)
D. Cavagnino, Università di Torino, Italy (email: davide@di.unito.it)
P.G. Cerello, INFN Sez. di Torino, Italy (email: cerello@to.infn.it)
P. De Remigis, INFN Sez. di Torino, Italy (email: deremigi@to.infn.it)
D. Falchieri, INFN Sez. di Bologna, Italy (email: falchieri@bo.infn.it)
A. Gabrielli, INFN Sez. di Bologna, Italy (email: gabrielli@bo.infn.it)
E. Gandolfi, INFN Sez. di Bologna, Italy (email: gandolfi@bo.infn.it)
P. Giubellino, INFN Sez. di Torino, Italy (email: giubellino@to.infn.it)
R. Hernandez, INFN Sez. di Torino, Italy (email: hernandez@to.infn.it)
M. Masetti, INFN Sez. di Bologna, Italy (email: masetti@bo.infn.it)
L.M. Montano, INFN Sez. di Torino, Italy (email: montano@to.infn.it)
D.Nouais, INFN Sez. di Torino, Italy (email: nouais@to.infn.it)
A. Rashevsky, INFN Sez. di Trieste, Italy (email: rashevsky@tr.infn.it)
A. Rivetti, CERN, Switzerland (email: angelo.rivetti@cern.ch)
F.Tosello, INFN Sez. di Torino, Italy (email: tosello@to.infn.it)
A. Vacchi, INFN Sez. di Trieste, Italy (email: vacchi@tr.infn.it)
A. Werbrouck, Università di Torino, Italy (email: albert@di.unito.it)
for the ALICE Collaboration

Abstract

Recent developments of the Silicon Drift Detector (~SDD~) readout system for the ALICE experiment are presented. The foreseen readout scheme is based on 2 main units. The first unit consists of a low noise preamplifier, an analog memory which continuously samples the amplifier output, an A/D converter and a digital memory. When the trigger signal validates the analog data, the ADCs convert the samples into a digital form and store them into the digital memory. The second unit performs the zero suppression/data compression operations. In this paper the status of the design is presented, together with the test results of the A/D converter, the multi−event buffer and the compression unit prototype.

1. INTRODUCTION

The Silicon Drift Detectors are expected to provide high detection efficiency over the whole detector surface, a spatial precision of the order of 30 μm, a two−track separation down to O(600) μm. In addition the detector should provide a charge resolution such that the dE/dx resolution is dominated by Landau fluctation, from which the truncated mean of the four ITS dE/dx samples is around 10% for M.I.P.

A M.I.P. releases about 4 *fC* in the SDD. For hits far from the anode pads the charge collected by one is typically one−third to one−half of the 4 *fC*; thus the tails of the hit signal, essential for the position determination, will consist of less than 1 *fC*. The range of useful signals is limited between the noise level (250 e^-) and 28−32 *fC*, but higher signals (up to 160 *fC*) are possible.

The charge generated by a particle crossing the detector, depending on the crossing point and therefore on the drift time, can be collected by one anode as a fast gaussian signal (σ = 5 *ns*) or by several anodes (up to five) as a slower gaussian signal (σ = 30 *ns)*, due to the diffusion during the charge drift through the detector.

In order to obtain the required precision the signal has to be sampled at quite high frequency (around 40 *MHz*); the dynamic range is 10 bits while an 8 bit resolution is sufficient if a non linear readout is adopted.

Due to the high sensitivity of the SDD to temperature variations and the very stringent requirement on the material budget which does not allow a very massive cooling system, the allowed power consumption for the electronic readout is very low (below 5 *mW/channel*).

2. SYSTEM ARCHITECTURE

In order to minimize the power consumption, the signals coming from the detector are not immediatly digitalized after the low noise preamplifier. Instead, they are continuously stored into an analog memory; only when the trigger signal is received the memory content is frozen and the data are converted and sent to a digital event buffer. In this way the most power demanding components work for a reduced percentage of the time (below 10%) greatly reducing the power consumption. After a local digital storage, which de−randomizes data for a lower transmission speed, the data have to be transferred to the acquisition system. Since the amount of data is very large (around 32.5 *MBytes/event*) and more than 95% of these data are zero, a data reduction is performed. In order to minimize information losses an Huffman encoder has been used, togheter with tunable filter functions which allow to reach the required compression factor in the presence of noise.

Figure 1 shows the full readout architecture.

3. THE FRONT END READOUT SYSTEM

In the Inner Tracking System of the ALICE experiment the SDDs are placed on linear support structures called ladders. The front−end modules are placed on the ladders, near the detectors, and are based on two functional modules, named PASCAL and AMBRA architectures.

3.1 The PASCAL architecture

The PASCAL architecture performs the low noise preamplification, analog storage and A/D conversion. A fully CMOS, low noise transimpedance amplifier continuously write the SDD signals into a switched capacitor analog memory at 40 *MHz*. When the trigger signal is received, the memory cells contents are converted in digital through a charge redistribution successive approximation A/D converter.

Current prototypes of the PASCAL architecture are designed as separate ASICs in standard technologies

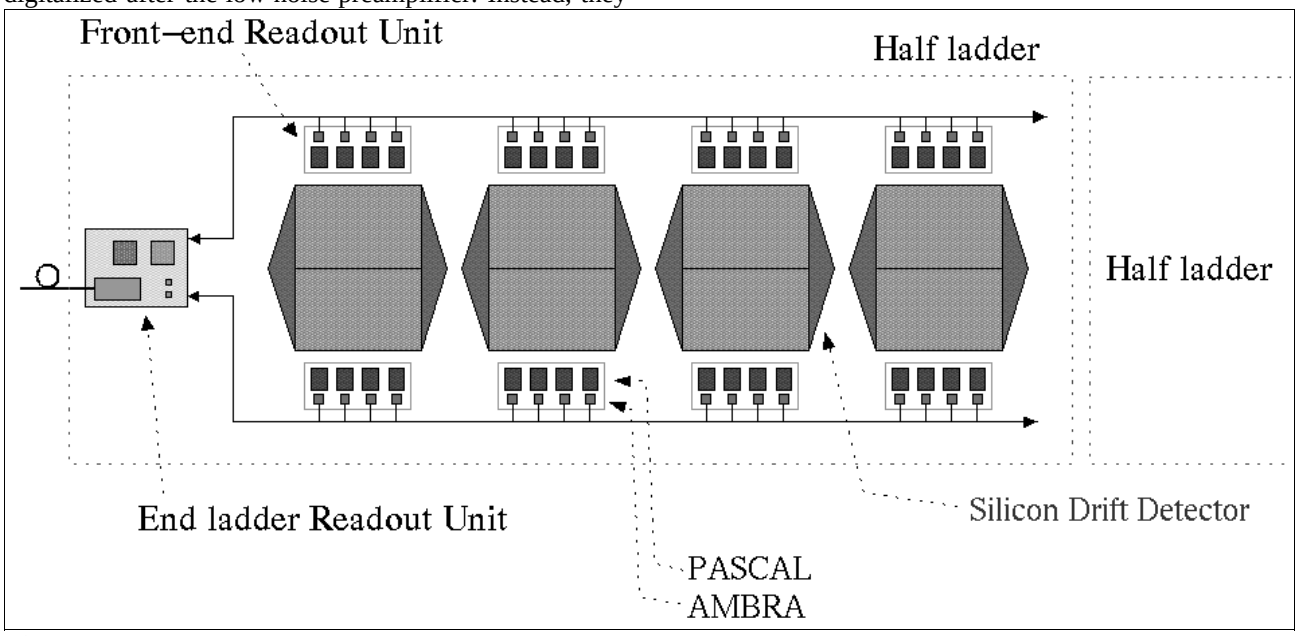

Figure 1

(0.7−0.8 μm); the A/D prototype fulfils the specifications while the preamplifier, which has been succesfully tested in beam tests, has to be improved in term of dynamic range. Promising results has been obtained also with the analog memory.

The final goal is to design the full architecture as a single chip using the new deep submicron technologies (0.25−0.35 μm).

3.2 The AMBRA architecture

In order to decrease the number of transmission wires from the detectors to the end ladder to a manageable number an event buffer strategy has been adopted. The events are temporarly stored in local digital buffers near the detectors; in this way the analog memory can restart the write mode faster thus reducing the dead time. It has been shown [1] that with only two event buffer the dead time due to event buffer overflow is around 0.1%.

The current prototype of the AMBRA architecture is a single ASIC designed in 0.35 μm technology

3.3 Front−end prototype results

The non linear preamplifier prototype. In order to study the feasibility of a signal compression at the preamplifier level, a prototype of a non linear transimpedance amplifier has been developed and tested [4].

The chip was designed to meet the following requirements:

- Maximum input signal: 32 fC
- Equivalent input noise charge: <500 e^-
- Total input current noise: <2 nA r.m.s.
- Power consumption: <1 mW.

The developed prototype is a two stage system in which a non linear transimpedance amplifier is followed by a voltage differential amplifier.

The non linear input−output relationship is obtained using a MOS device as the feedback element around a cascode stage, as proposed in [7].

This architecture has two interesting features:

- It implements in a very small area a second order small signal transfer function already at the preamplifier level
- The non linear large signal behaviour relies on the I−V characteristics of a MOS device, which is mathematically very well modeled.

In the present design, the properties of the feedback branch have been adjusted so that the equivalent small signal gain is of the order of 500 $k\Omega$.

This value has been chosen as a trade−off between noise, speed and power consumption. The peaking time of the preamplifier is 25 ns.

A voltage differential amplifier has been used as second stage, in order to have a total gain of 2 $M\Omega$ when the output is read−out in a single ended configuration and 4 $M\Omega$ when the output is read−out in a differential manner. Since the aim was to study the basic properties of the non linear signal processing performed by the preamplifier, the second stage has a wide bandwidth in order to avoid any additional shaping.

The amplifier has been designed to work with power supply down to 3.3 V and a power consumption (excluding the output drivers) of 0.6 mW.

The lab measurements show the amplifier is within the specification for both power consumption and noise. In fact, the measured power consumption is 0.66 mW with a 3.3 V power supply and the noise is less than 2 nA r.m.s, which is an upper limit dictated by the experimental setup.

The large signal transfer function was fitted with a parabola ($y=ax^2 + bx + c$, where y is the input current and x is the output voltage). The result are summarized in figure 2 and 3.

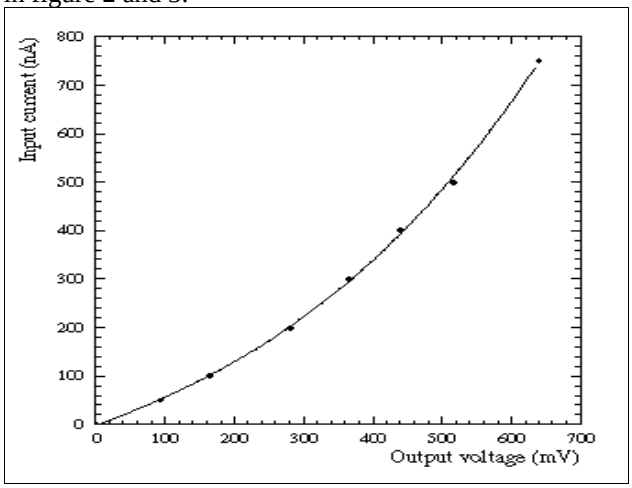

Figure 2

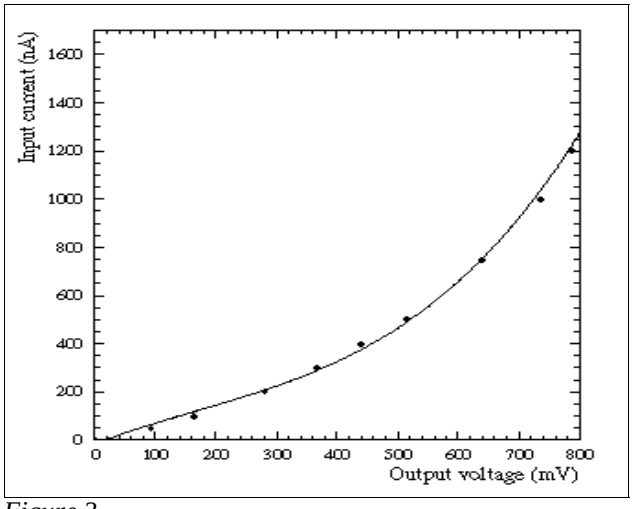

Figure 3

From these plots, it can be seen that the parabola is a very good approximation for input current up to 700 nA, which in the case of ALICE SDD corresponds to a maximum input charge of about 20 fC.

For higher input signal the input−output relationship is best fitted by a third order curve. This is due to a distortion in the voltage amplifier.

In the beam test conditions, only minimum ionizing particles were present (pions of momentum of 375 *GeV/c*). This means that with the beam test data, the lower region of the dynamic range could be studied. Drift detector equipped with this prototype preamplifier was successfully tested with particles.

The A/D converter prototypes. The analog to digital converter foreseen in the front−end module has to perform a complete conversion in 500 *ns*, with a average power consumption of 1 *mW/anode*. Since the A/D is used for less than 10% of the time, the the power consumption during conversion should be less than 10 *mW/anode*. When moderate speed and low power are required, successive approximation converters based on charge redistribution DACs are a very attractive approach, because with this technique resolution of 8−10 bits can be implemented in a silicon area small enough for multi−channel integration.

In a charge redistribution converter, an array of binary weighted capacitors is used to generate fractions of a reference voltage, V_{ref}, which are compared with the input voltage to be converted.

A prototype chip has been developed in order to meet the following goals:

- Identify an architecture that can satisfy the SDD requirements in term of power budget, speed and resolution.
- Study the problems arising from the parallel operation on the same chip of several ADCs (cross talk, loading on the reference voltage, etc.)
- Test the digital circuitry which controls the operation of the converters

The prototype chip containing sixteen A/D converters of the charge redistribution type has been fabricated in a 0.7 *μm* commercial CMOS technology. The architecture of the converters is the same that was used in the CRIAD ADC [8] and consists of a 8 bit DAC and a very sensitive offset compensated comparator.

The chip also contains a digital buffer and multiplexer and a digital control unit.

In figure 5 the FFT test shows a THD (Total Harmonic Distortion) below 55 dB, while the histogram tests gives a DNL (Differential Non−Linearity) between −0.4/+0.4 LSBs and no missing codes, and a INL (Integral Non−Linearity) between −0.2/+0.5 LSBs.

DNL and INL are shown in figure 4. FFT, DNL and INL has been measured on a 1 V_{pp} sinewave at 5.5 *kHz*. For FFT 4075 samples has been used while DNL and INL are calculated with 20375 samples.

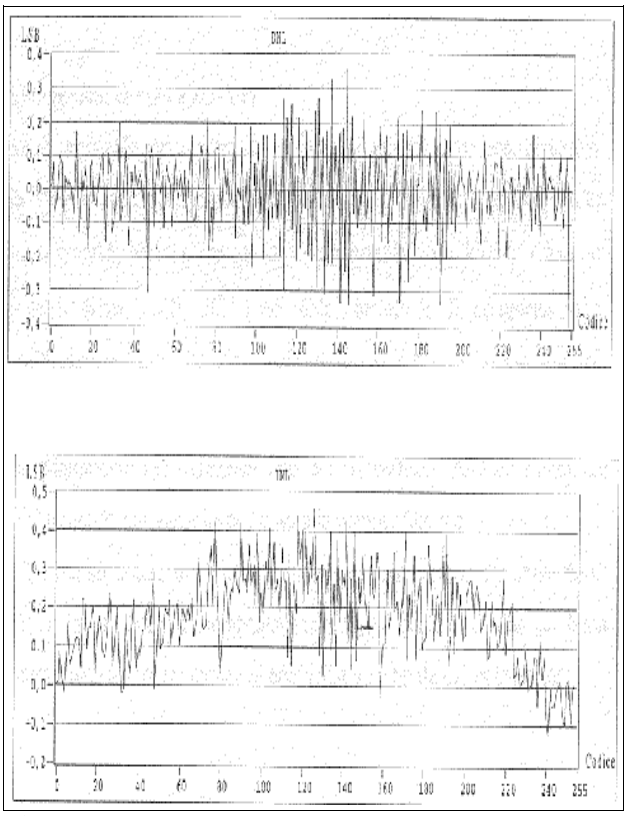

Figure 4

Due to the measurement setup the sampling frequency is only 156.25 *kHz*, however the conversion time is 500 *ns* (the rest of the time is lost in the instruments startup).

The power consumption is below 4 *mW*/ADC, including the digital control unit.

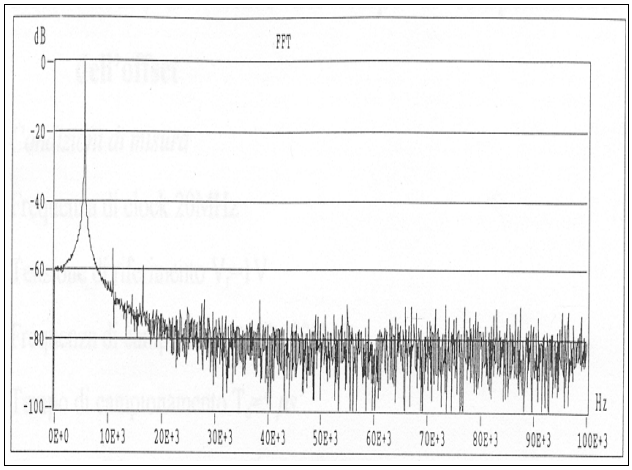

Figure 5

The AMBRA_01 chip. The first version of the AMBRA chip has been designed and sent to the foundry.

Table 1 summarize its characteristics.

The AMBRA_01 is designed for an 8 bit ADC but it can be easily redesigned for 10 bit with some area penalty.

Global	Technology	Alcatel 0.35 μm
	Size	3809x4456 μm²
	Number of cells	1100
	Number of I/O pads	87
	Max clock frequency	50 MHz
	Total power consumption	468.52 mW
	Power consumption/chan	7.3 mW
Memory	Words	4096
	Bits per word	32
	Size	3649x1347 μm²
	Power consumption	135.7 mW
Logic	Size	141.138 μm²
	Power consumption	< 72.6 mW

Table 1

The main sources of power consumption are the event memories and the output buffers. Table 1 reports the power consumption of the circuit during operations, while the idle consumption is negligible; therefore the average power consumption is much less. The memory buffer peak consumption of 2.15 *mW/channel* decrease to an average of less than 0.2 *mW/channel*, since the memories are used less than 10% of the time and the output drivers consumption of 1.9 *mW/channel* decrease to a negligible 32 *μW/channel* since the output buffers are used only around 1.6% of the time.

4. THE END LADDER READOUT UNIT

The end ladder modules are placed at both ends of the ladders, and contains the compression circuit, the optical interface to the data acquisition system and the control system.

The most important functional module is the CARLOS architecture. Its purpose is to compress the signals coming from the front−end readout units to a size compatible with the requirements by the ALICE data acquisition system.

4.1 Data compression

The amount of data generated by the SDDs is 32.5 MBytes/event. Most of these data are zeroes, therefore a data compression is required in order to save space on tape. Since a simple zero suppression leads to an unacceptable information loss, several compression algorithms have been studied :

- Zero sequence encoding : sequences of zeroes are transmitted as a zero code followed by the number of consecutive zeroes. Since the occupancy is quite low, long zero sequences are highly probable.
- Simple threshold zero suppression : the data below a certain threshold, which takes into account noise and pedestal, are set to zero. This technique is very easy to implement and increases the number of zeroes by cutting non zero values due to the noise. Unfortunately this results in information loss.
- Differential encoding : instead of the samples, the difference between consecutive samples is transmitted. In this way any channel baseline value is translated into a zero sequence. On the other hand a differential encoding scheme is more sensitive on sample errors during transmission.
- Simple threshold tolerance : it is a simple threshold zero suppression applied after the differential encoding. It reduces the noise variations over a baseline, at the expense of information loss.
- Huffman encoding : since the probability of lower codes is much higher than the higher ones, using a variable length encoding leads to a lossless data reduction. This reduction depends on the sample statistics; the implementations is quite heavy in terms of hardware requirements.
- Multithreshold zero suppression : a sample is set to zero depending on its value and on the value of neighbour samples. In this way the information loss can be greatly reduced with respect to single threshold zero suppression.

An FPGA−based prototype of the first 5 algorithms, with software tunable parameters, has been realized and is currently under test with the data taken from the ALICE SDD beam tests [5]. The sixth algorithm is currently under evaluation. A detailed description of this alghoritm can be found in [6].

5. REFERENCES

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