RECENT DEVELOPMENTS AND RESULTS ON APV(DMILL) CIRCUITS FOR SILICON AND MSGC DETECTORS

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Abstract

For the analogue read-out of the CMS tracking system several variants of the APV design have been developed in DMILL technology: the APVD_AC and APVD_DC for AC and DC-coupled silicon detectors, respectively, and a rapid front-end amplifier with 25 ns peaking time based on a bipolar transistor for the possible use of MSGC or silicon detectors. This paper introduces these circuits developed in the DMILL technology and focuses then on experimental results obtained with prototypes on silicon and MSGC detectors in a 200 GeV pion beam.

1. INTRODUCTION

Based on experience with the APV6 circuit[1] developed in the HARRIS AVLSIRA bulk CMOS technology and on a circuit of similar architecture FILTRES[2] in the radiation hard technology DMILL[3], the work on the APVD circuit for the CMS tracker was started in the beginning of 1998 by a Franco-British collaboration. The architecture and the schematics of the APVD are essentially identical to the APV6 and consist of 128 analogue channels, each composed of a low noise preamplifier, a CR-RC shaper with 50 ns shaping time, a 160 cell deep analogue pipeline operated at 40 MHz and an analogue signal processing stage (a deconvolution filter) which recuperates the initial fast response of a silicon detector and confines it to one LHC bunch crossing. One amplitude per trigger of each of the 128 channels is read-out serially via a high-speed 20 MHz multiplexer. Slow control is implemented on the chip using an I2C serial bus which allows to configure and to bias the circuit and to run the internal calibration system. For the most technology dependant part, the preamplifier and shaper, a design was adapted and modified from the schematics of the FILTRES amplifier. We have reported at previous conferences on the design and on measurements of this circuit[4,5,6].

2. THE APVD CIRCUIT

2.1 Translation of APV circuit

The APVD represents the first experience of translating a complete large mixed analogue-digital chip from one technology to another. Its immediate complete functionality can be regarded as a success of this translation. However, we also had to report on an instability problem of the analogue base line which was observed in all versions of the circuit up to now and which limits partially its use for detector tests. Numerous investigations of the circuit using various simulation tools and micro interventions on the chip itself revealed that these instabilities or oscillations are a collective phenomenon which only occurs if a minimum number of channels are active, the critical parameter being the total current drawn in the bias lines. Under these conditions the unavoidable common resistances in the ground and bias lines will establish various loops which couple in particular the source follower which drives the capacitive load of the pipeline, back to the preamplifier input. The phase shifts in the amplifier structure are crucially influenced by the parasitic capacitances which are specific in each technology. Eventually a resonance pole can appear within the bandwidth of the amplifier.

Consequently, the schematic and the layout of the amplifier have been revised rigorously to eliminate all possibly occurring couplings. In contrast to other circuit designs in DMILL technology which reported also stability problems in the past[7], and who use bi-polar input transistors, we have found only very weak evidence for capacitive feedback problems related to the back-plane of the SOI substrate in our circuit. However, precautions were taken in the last submission to avoid capacitive feed-back. For more details see reference[8] in these proceedings.

2.2 APVD_DC circuit

DC-coupled silicon microstrip detectors have significant advantages compared to AC-coupled devices due to their less complex fabrication process and

consequently better yield. The price to pay is the necessity to sink the after several years of LHC significant leakage currents at the preamplifier level. A current compensation circuit was added in front of each preamplifier. Good performance of the circuit has been measured on prototypes for leakage currents between 0 and 10 μA. A complete 128 channel circuit has been submitted and is expected to return in the next weeks. For more details see again reference[8]. Tests are being performed to evaluate the option of using DC-coupled silicon detectors in the CMS tracker.

3. OPTIONS FOR MSGCS

MSGC detectors will contribute to about one half of the over 10 million analogue read-out channels of the CMS tracker. Although not dissimilar to silicon microstrip detectors with respect to the total charge collected, a number of significant differences have to be accounted for. In particular, the signal formation time is determined by the ca. 60 ns long drift time and by statistical event-to-event fluctuations of the primary ionisation charge along the particles path in the sensitive gas volume of the detector. They lead to important variations of the signal peaking time and amplitude. This prevents the unique association of the measured amplitude to the bunch crossing (bco) in which the event was generated. The precision cannot be much better than 2-3 bco.

3.2 Simulations

Numerous filtering algorithms employing different weights and different samples of the pipeline spaced by 25 or 50 ns have been evaluated in rather detailed simulations of the MSGC and the associated electronics[9]. Although significant differences between various signal processing methods occur, in general algorithms which optimise the amplitude or the detector efficiency lead to an analogue response spread over several bunch crossings. On the other hand the signal can be confined to a narrower time interval at the cost of some amplitude. In the end an optimum has to be found which will also depend on the precise operation parameters at which the MSGC will eventually be run.

In these studies the possible use of a faster shaping of the order of 25 ns at the input stage of the circuit has been proposed to improve the timing precision.

3.2 Bipolar Amplifier

Two test circuits have been designed and submitted. One using only CMOS elements, increasing size and power of the input transistor to obtain the required speed and low noise performance. Tests of the fabricated circuit achieved good but not quite the anticipated values.

A second circuit was designed on the base of a bipolar NPN transistor embedded in a folded cascode topology. The preamplifier feedback loop provides already a sufficient short time constant, so no further shaping is required. A second stage is used as an active filter to eliminate noise outside the useful bandwidth. At a power consumption of 1.4 mW/channel a peaking time of 25 ns and a gain of 90 mV/MIP with a non-linearity of less than 5% over ±6 MIPs dynamical range was measured. Its noise performance of 1000 electrons ENC was obtained for a detector capacity of 12 pF. For further details see reference[10] in these proceedings.

4. OPERATION OF THE APVD_AC ON MICRO-STRIP DETECTORS

In September 1998 APVD_AC circuits where mounted on small 6 cm long silicon micro-strip detectors with 64 active read-out strips at 50 μm pitch. One circuit was connected to a MSGC detector of ca 230 μm pitch via 400 Ohm serial resistors implemented on the pitch-adapter in order to better protect the circuit against discharges. Both types of detectors were installed at CERN in a 200 GeV pion beam of the SPS accelerator. A high precision silicon telescope of 1-2 micron spatial resolution allowed precise track reconstruction to evaluate detector efficiencies and resolutions.

Problems occurred during these tests due to the instability of the APVD baseline discussed above. Although a large part of these oscillations could be corrected for by a common mode baseline correction, the remaining electronic noise was by about a factor of two higher than the values observed on our electronics test bench. This high level of noise affected the efficiency measurement as well the measurement of the delay curve in regions where the amplitude is very small. Nevertheless encouraging results were obtained.

4.1 Results from Silicon Detectors

In Fig. 1ab we present the delay curve measuring the analogue response of the circuit and the track reconstruction efficiency as a function of time and in Fig. 1c the obtained spatial resolution on the peak. The results are shown for peak- and deconvolution-mode operation of the circuit on the left and right hand side of the figure, respectively. Operating the circuit in peak-mode we obtain an excellent efficiency of 99% and resolution of 7 μm despite a signal to noise ratio of only 12 due to increased noise. The timing curve does not coincide with a ideal CR-RC shaper, however is being reproduced by the in the laboratory measured response function with the actual bias settings during the beam-test, in particular the shaper feedback transistor.

In deconvolution mode the efficiency is reduced to 93% by the decreased signal to noise ratio of only 7 at the peak of the timing curve, but the measured spatial resolution of 11 μm is still good. We note that the delay scan in this mode is not being reproduced by the electronic response to an injected very short test pulse. The profile observed with particles in the beam is wider. This could be caused

by tails in the charge collection of the silicon detectors; however, a remaining effect from the large base-line oscillations cannot be ruled out.

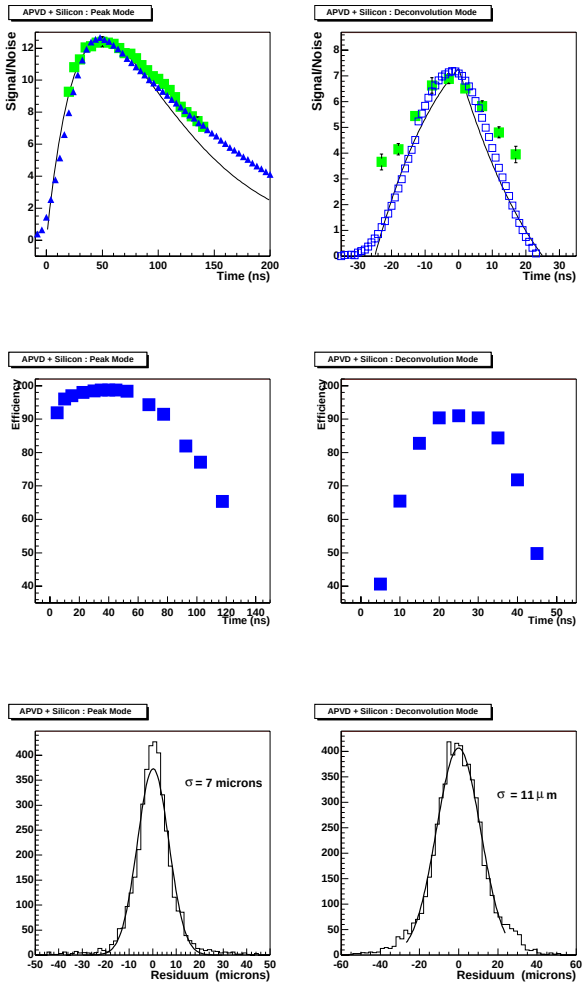

Fig. 1abc: Results for silicon detectors: Delay scan of signal shape (a) and reconstruction efficiency (b) together with the obtained spatial resolution (c) in peak and deconvolution mode on the left and right hand side, respectively.

4.2 Results with a MSGC Detector

Operating the MSGC at a moderate cathode bias of 520-530 Volts and a drift field of 2900 Volt per 3 mm gap in a 60/40 DME/Ne gas mixture a peak efficiency of 97% was obtained for tracks traversing the chamber perpendicularly with a signal to cluster-noise ratio of 17.

In Fig. 2 we show a delay-scan of the MSGC signals operating the circuit in peak-mode. The measurements are compared with two simulations, one using an ideal CR-RC amplifier response which falls faster than our data, and one folding the measured transfer function of the chip at the actual bias settings with the MSGC signal simulation. The latter curve reproduces very well the timing curve over the measured range. This agreement supports confidence in the use of simulations to optimize the signal processing algorithms.

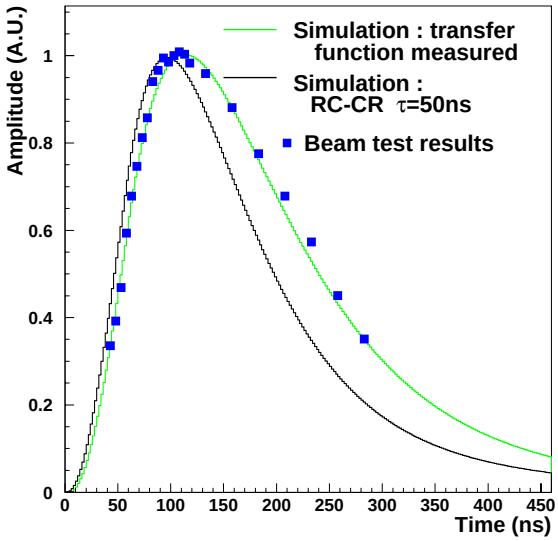

Fig. 2: Pulse shape of a MSGC detector signal optained by a delay scan with the APVD compared to a detector and electronics simulation using an ideal CR-RC and the real shaper transfer function.

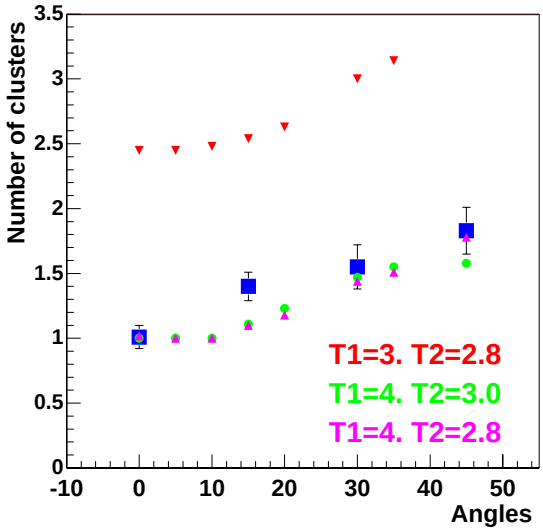

Fig. 3: Number of reconstructed clusters per incoming track as a function of angle compared to simulations with equivalent cuts.

The number of reconstructed clusters per single incoming track is compared in Fig. 3 to simulations as a function of the incident angle of the particle. As expected, the number of clusters increases as the track inside the MSGC is spread over several strips. The low average number of primary ionization clusters of about 12 and their fluctuations will lead occasionally to cluster

splitting and thus increase their average number per track. Choosing appropriate cuts in analysis and simulation the trend of the data is very well reproduced.

Similarly we observe an increase of the cluster width at larger incident angles. Also the spatial resolution changes from 40 μm to 1 mm for incident angles between 0^o and 45^o, respectively.

5. PRELIMINARY RESULTS OF IRRADIATION STUDIES

5.1 X-Ray Irradiation of the APVD_AC Chip

A separate paper[11] in these proceedings describes first irradiation results of a complete APVD circuit. A 10 keV X-ray beam available at CERN was used to irradiate a circuit at a dose-rate of 15 krad/minute up to 20 Mrad. Important effects were observed concerning the linearity of the DAC converters in the bias generator block. As described in the paper, a modified layout has been implemented in the last submission of the APVD chip to correct for this

The pulse shape changes slightly (-25% in amplitude and +10 ns in peaking time) if measured during irradiation at the nominal I2C bias settings. This change is partially due to the simultaneous changes of the bias settings. A good fraction of the pulse shape distortions are recovered some hours after irradiation. Running the CMS experiment, the shape could be retuned continuously.

During irradiation the noise increases at a rate of about 30-40 ENC/Mrad and recovers after 24h to a level about 250 ENC above its initial value.

5.2 High Intensity Pion Irradiation of the BiCMOS Front-End Amplifier

As the radiation hardness of DMILL bipolar transistors has been a crucial issue in the past we irradiated our BiCMOS amplifier in an intensive pion beam of PSI with an integrated flux of 10^{14} particles/cm^2, corresponding to about 10 years of LHC operation. Small changes in gain and speed were measured several days after irradiation. A change of beta from initially 200 down to 30 can be deduced from these changes. Nevertheless the circuit demonstrates full satisfactory functionality after irradiation.

6. PERSPECTIVES AND CONCLUSIONS

The APVD circuits provide the first LHC-radiation hard front-end chip to the CMS tracker. After the circuit had been translated into the DMILL process, the development has been severely delayed by the unforeseen occurrence of subtle feed-back loops within the amplifier architecture. We are confident that the modifications implemented for the last submission will overcome this problem.

In addition, a specific adaptation to DC coupled silicon detectors has been developed which will work up to leakage currents of at least 10 μA per channel. This option will allow more flexibility in the choice of detectors.

In the context of optimising the bunch identification capability of the MSGC detectors a fast 25 ns shaping front-end amplifier was designed and tested which may find also applications for other detectors.

Several evolutions in CMS have taken place during the last 10 month and will possibly modify the input for our further work: the CMS Tracker detector technology is under review to overcome possible weaknesses at high particle fluxes. The introduction of a GEM gas amplification plane in the MSGC detectors could affect the time development of the signal if the chamber is not operated at identical drift fields. Alternatively a “silicon only” tracker is being considered. - Certainly, optimisation of efficiency at relatively low gain operation has taken priority over timing precision. A possible submission of a DMILL MSGC circuit by the end of 1999 based on a 50 ns shaping time and containing also other important adaptations to MSGCs similar to the APV6_M[12] will be prepared. However its execution will depend on decisions taken by CMS during the next months.

Secondly, a further translation of the APV design into a 0.25 μm process is being attempted[13]. Although this technology is not qualified for a high irradiation environement, possibly it is proven to be so if certain precautions are respected in the layout[14].

Therefore, on the long term the further development of the APVD family will depend on the choice of detectors for the CMS tracker and also, much more important on the choice of technology for the tracker front-end electronics.

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