

The Development of a Rad-Hard CMOS Chip for the Binary Readout of the ATLAS Semiconductor Tracker

D. Campbell, N. Falconer, M. French, W. Gannon, M. Morrissey, P.W. Phillips, M. Tyndel
Rutherford Appleton Laboratory, Didcot, UK

A.A. Carter, T. Pritchard

Queen Mary and Westfield College, University of London, UK

A. Ciocio, M.G. Gilchriese, C. Haber, G. Meddeler, O. Milgrome, H. Niggli, H. Spieler
Lawrence Berkeley National Laboratory, Berkeley, CA, USA

J. DeWitt, D. Dorfan, T. Dubbs, A.A. Grillo, E. Spencer

Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA, USA

F. Anghinolfi, P. Jarron, J. Kaplon, C. Lacasta, P. Weilhammer
CERN, Geneva, Switzerland

W. Dabrowski

Faculty of Physics and Nuclear Techniques, UMM, Cracow, Poland

M. Wolter, R. Szczygiel

Institute of Nuclear Physics, Cracow, Poland

A.Clark, D. LaMarra, D. Macina, A. Zsenei
University of Geneva, Switzerland

Abstract

A new version of the ABC (Atlas Binary Chip) has been submitted to Honeywell. The design contains many enhancements over the original ABC: new DAC circuitry for improved radiation hardness, faster and more robust logic parts and new interface elements to the CAFE chip. Each of these design elements will be described in detail as well as the status of the ongoing test program. Additionally, plans for production testing of ABC's will be presented.

1. INTRODUCTION

The ABC is an integrated circuit developed for the Honeywell rad-hard CMOS process to provide data buffering and data compression for the binary readout architecture used for the silicon strip detectors in the ATLAS Semiconductor Tracker (ATLAS SCT) [1]. This chip was developed to operate in the extremely harsh environment of the Large Hadron Collider (LHC) and meet the ATLAS requirements of low power, low noise and high efficiency. The chip is designed to be used in conjunction with a front-end IC which is being developed for the Maxim bipolar process, and it is functionally compatible with another technology option being pursued on the DMILL biCMOS process [2].

The chip includes the following features:

- 128 independent input channels with fast low power, level translators to accept signals from the bipolar front-end chip.
- 128 channel by 132 deep pipeline buffer constructed as a fully dual-ported memory.
- De-randomizing buffer to stage data for output processing
- Data compression to suppress output from non-hit channels and compact data from hit clusters to reduce data transmission time.
- Serialized LVDS output
- Token passing scheme to allow multiple chips to operate in a chain with minimal interconnects
- Redundancy schemes to allow continued operation when some chips in the chain become non-operational
- Error reporting of some faulting conditions in trigger processing
- DACs for control of analogue functions on the bipolar chip.
- Testability features to allow chip functionality to be tested at wafer probe as well as in situ.

The binary readout architecture includes an amplifier-discriminator chip, named CAFE, which amplifies raw signals from the sensor strips and uses a single threshold discriminator to distinguish hit from non-hit channels. These discriminated signals are then fed to the ABC chip for buffering and data processing. The main purpose of the ABC is to provide pipelined data buffering until a

decision can be made by the ATLAS Level 1 trigger as to whether the data is sufficiently interesting to be read out. Upon receipt of such a trigger signal, the ABC must compress the data and serialize it for output through the optical transmission system of the ATLAS SCT. Data compression is required to meet the limits of the transmission system along with the expected trigger rate

serialize data into two optical links. In order to accomplish this with a minimum number of interconnections on the interconnect hybrid, a token passing scheme was implemented. One design goal was to minimize the use of parallel busses because they complicate the interconnect layout and also because single chip failures can often disable the entire buss.

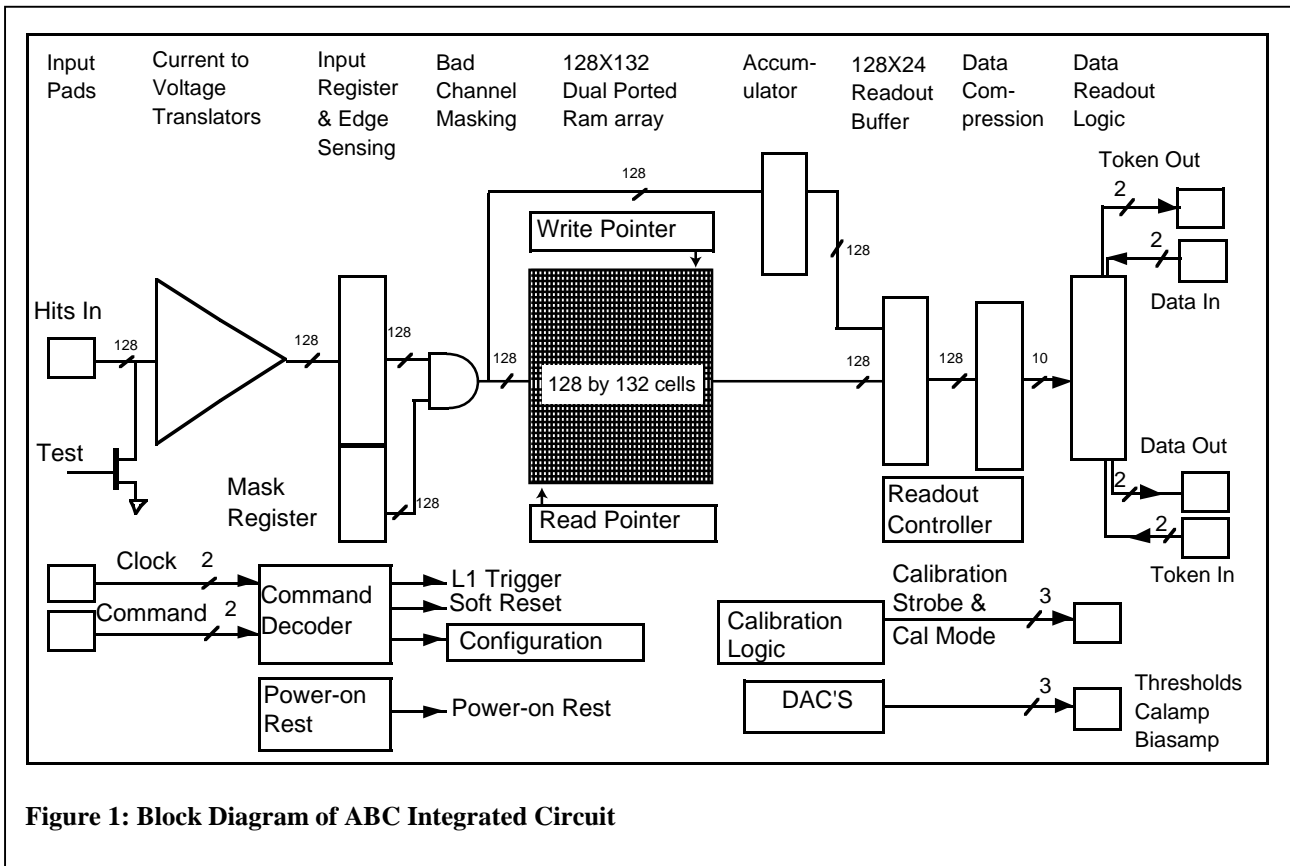


Figure 1: Block Diagram of ABC Integrated Circuit

and occupancy. Likewise, an output or de-randomizing buffer is included to smooth out the fluctuations in the instantaneous trigger rate.

Since the accompanying CAFE chip does not have any digital circuitry to communicate with the control system, the ABC must provide various control signals to it when instructed to do so by the SCT control system. These include three DACs to control bias current, discriminator threshold level and calibration pulse amplitude. There are also signals to control the timing and addressing of calibration pulses inside the CAFE. All these control interfaces to the CAFE as well as the data exchange signals themselves must be designed to minimize any coupling of clock or other digital noise into the sensitive front-end circuitry. Care was also taken to make the interfaces self-correcting for variations in characteristics of the individual bipolar and CMOS chips.

The ATLAS SCT detector module contains 1536 sensor strips. These will be readout via 12 chip sets of 128 channels each. This group of 12 ABC chips must

Furthermore, three redundancy features have been included. One allows the chain of readout chips to operate even if one of the chips in the chain should become faulty by having the token and data chain bypass the faulty chip. The second feature allows the readout chain to shift all of its data to one of the two normally operating optical links should one become faulty, and the third redundancy feature provides two independent clock and command inputs so that the backup one can be used should the primary fail. All these features were included in the design to increase reliability of the SCT where maintenance will be difficult. A block diagram of the chip is shown in Figure 1.

The first iteration of this chip was fabricated on Honeywell's rad-hard bulk CMOS process, RICMOS-IV. Testing of the circuit revealed an error in the clock receiver circuit which prevented proper functioning. Using focused ion beam repair processing, the faulty circuit was bypassed on a few chips so that the rest of the circuitry could be tested. Following extensive tests, a

redesign of the clock receiver circuit and further optimization of other circuit blocks, a second iteration was fabricated. Early test results of the second iteration will be presented.

2. TWO VERSIONS OF THE ABC

2.1 The first ABC

The prototype ABC was submitted to Honeywell in 1997. The first wafers were received November of that year. Some processing problems with the metalisation were identified by the foundry prior to shipping the wafers. Early tests of a few die confirmed that the ABC chips were not working. A follow-up lot was then processed and received February of 1998. Although largely functional there were a number of design problems discovered. These were then resolved and a second version (ABCH2) submitted. This has now been received and the results of preliminary tests with the new chip are presented below.

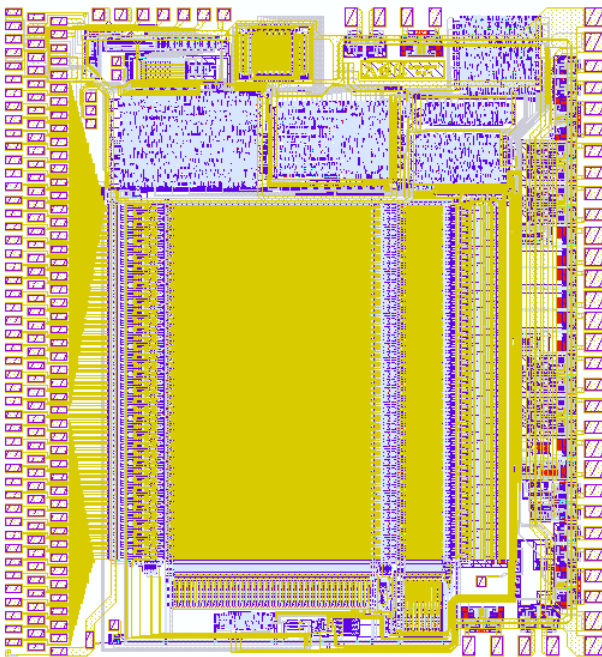


Figure 2: ABC version 1

The first ABC version is shown in Figure 2. Note that the standard cell blocks are separated into different regions and wired together at the 'top-level'. This method was found to be very labour intensive and all the standard cell logic was combined into one larger region on the second version. Examples of design problems encountered were incorrect function of the Power-on-reset circuit and LVDS inputs as well as changes to the reset configuration of the chip to conform to the ABC specification.

2.2 The second ABC

In all, around 30 changes were made. Each was tracked with exhaustive design review procedures to ensure all were implemented correctly. Not all changes were due to design problems but rather improvements to the power routing and increasing the robustness of the input level translators and the introduction of power saving features. The ABCH2 chip is shown in Figure 3.

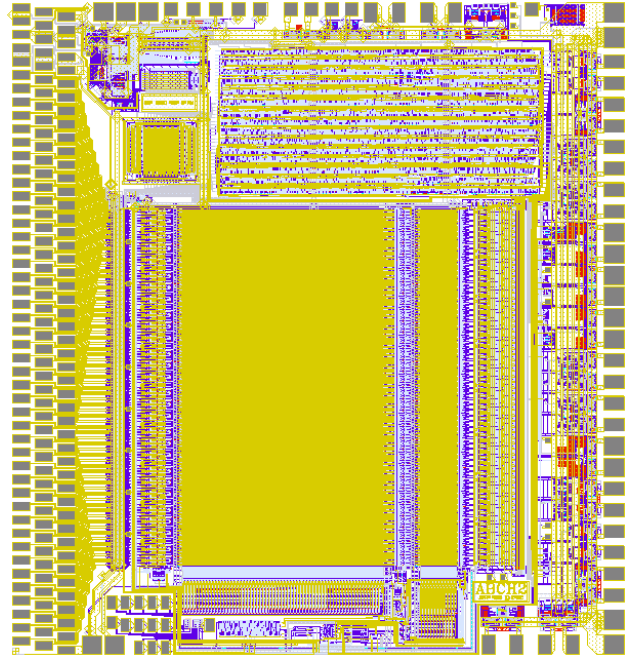


Figure 3: ABC Version 2

3. NEW DESIGN FEATURES

3.1 Test Port

Following the problems encountered in testing the first ABC a new test feature was incorporated into the ABCH2 design. It consists of a 128 input test multiplexer that gives access to 128 selected internal nets. These were then chosen carefully so that key timing signals and logic nodes were accessible. In the initial tests of the ABCH2 die this feature was then used to prove the functionality of the chip (see below). The multiplexer is controlled by a binary counter that is clocked from a dedicated input to a value that decodes the net of interest. That signal is then available at the 'test out' pin for observation. The full list of available signals is described in the chip specification document [3].

4. TEST RESULTS

4.1 Logic testing

The ABCH2 chips have been analysed with an IMS ASIC test system and have been proven to conform logically to the model of the circuit. The analogue parts of the ABC, however, require independent study and all cases so far have proven to be within specification. Examples are listed below.

4.2 POR circuit

By using the test multiplexer it is possible to measure the voltages at which the ABCH2 switches as the power supply is applied to the circuit. Results of a test sequence to switch between supply voltages of 2V and 4V are shown in Figure 4 and Figure 5. This method only tests the circuit response to slow edges but this is well within the ABC specification.

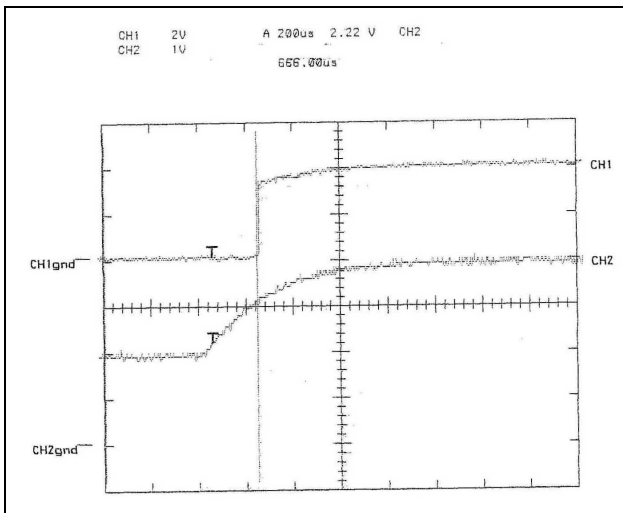


Figure 4: POR circuit switching from 2 to 4 volts

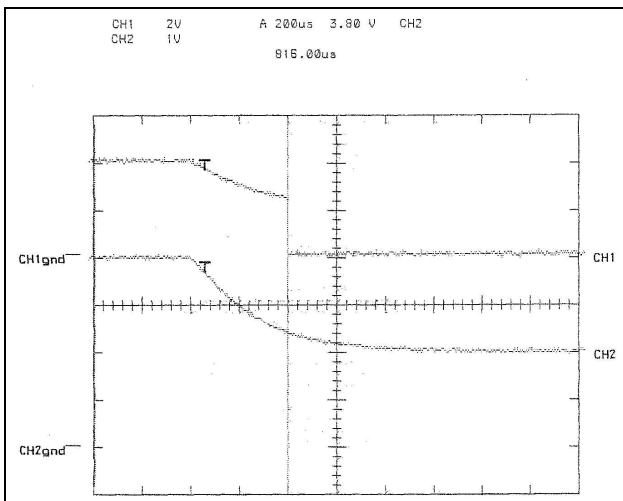


Figure 5: POR circuit switching from 4 to 2V

4.3 The Data Compression Logic

One of the critical timing issues for the ABC's internal logic is how fast the Data Compression Logic can scan through the 128 channels looking for data, one of the worst cases is when there is no hit at all. In this case a token has to 'ripple' through 128 gates. The important timing criterion is that this must happen in at least 200ns. Great care was taken in the design to optimise this. Simulations predicted a typical delay per channel of 0.55ns or 70.4ns for the full 128 channels.

Using the test multiplexer the point where the ripple starts and finishes can be measured. A measurement showing the traces overlayed is shown in Figure 6 below. This demonstrates a total delay of 85ns which is well within the 200ns limit and close to the simulator's expected value. Further tests are necessary on more samples as well as some post radiation measurements to identify the circuit's performance in such conditions.

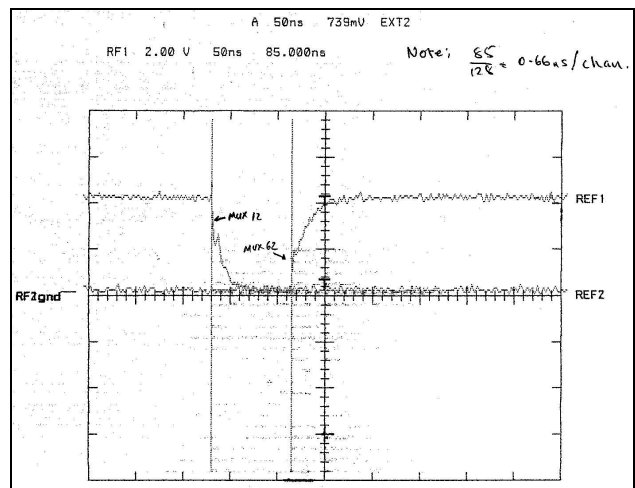


Figure 6: Oscilloscope trace showing DCL timing

The slow edges shown on the oscilloscope traces are predominately due to large capacitive loading caused by the scope probes and deliberately weak driving of the ABC test output. The measurements are taken at the beginning of the signal switch to minimise the errors caused by these effects.

4.4 LVDS IO Cells

In the ABCH2 chip, a simplified output circuit was implemented. Instead of using on chip band-gap type references, the IO levels are defined by 'H' network resistors which define the output levels based on resistor ratios and supply voltage. This method has proven extremely successful. We measure IO voltages matching those expected to a few milli-Volt. Another advantage was that such circuits are easy to shut down when not required (by switching all power branches off). This function was successfully implemented and the expected power savings achieved.

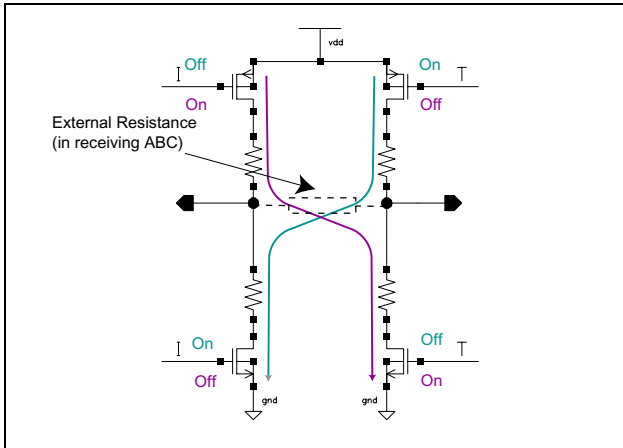


Figure 7: Chip to Chip token output circuit

4.5 Power Measurements

At wafer test each die will be measured for power in differing configurations. So far only preliminary figures exist. One die on a test card was measured at 1, 10, 20, 30, 40 and 50 MHz in both Master and Slave modes. The results of those measurements (calculated in mW per channel) are shown in Figure 8. A constant difference of 0.14mW is shown between Master and Slave modes. This corresponds to an additional DC current of 4.7mA and is as expected due to the datalink output circuit that is enabled in Master Mode.

The Slave configuration slope corresponds to 363uW plus 11uW per MHz.

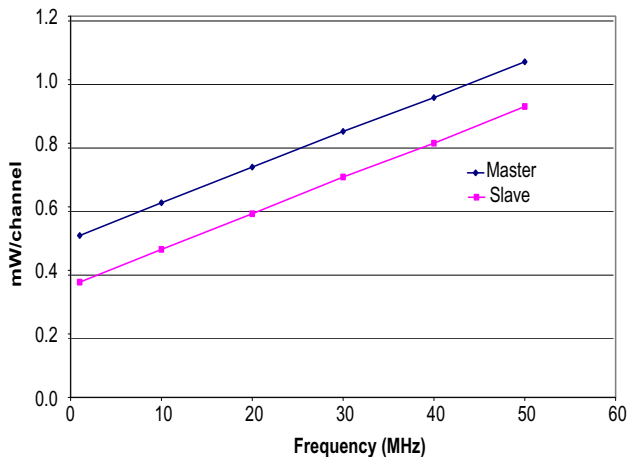


Figure 8: ABC Power (mW/Channel)

4.6 Logic test summary

So far detailed tests have been performed on 12 die of which 10 appear to work correctly. Testing at wafer level is just starting and many die will shortly be available to the collaboration.

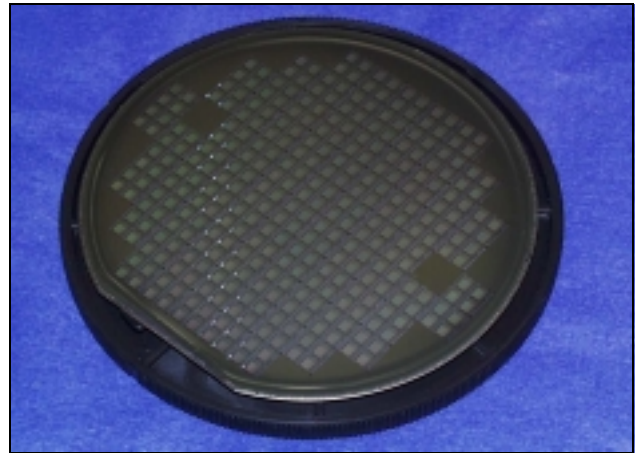


Figure 9: Picture of an ABC wafer

5. OUTSTANDING ISSUES

Following submission of the ABCH2 a further problem with the protocol engine was identified in the design. This, although not fatal, is important to correct prior to production for the Atlas SCT. The required changes have been executed and a new layout generated in preparation.

The DACs have not yet been studied in detail at RAL so no data was available for this paper. It is known, however, that there is a slight problem that results in failure to achieve true 8-bit precision throughout the DAC range. This is still under study and it is not yet known if changes will be required to remedy the problem.

ACKNOWLEDGEMENTS

We would like to acknowledge the help of Jeff Bizzell who assisted in the assembly of the evaluation cards as well as Richard Matson who helped in the driving of the IMS test system.

REFERENCES

1. ATLAS TDR 5, Inner Detector Technical Design Report, Vol. II, CERN/LHCC/97-17 (1997).
2. W. Dabrowski, et al., "A Single Chip Implementation of the Binary Readout Architecture for Silicon Strip Detectors in the ATLAS Silicon Tracker", Proc. of the Third Workshop on Electronics for LHC Experiments, London, CERN/LHCC/97-60 (1997), pp. 153-157.
3. Project Specification: ATLAS Binary Chip (ABC) Version: 5.01