PERFORMANCE AND RADIATION TOLERANCE OF THE HELIX128-2.2 AND 3.0 READOUT CHIPS FOR THE HERA-*B* MICROSTRIP DETECTORS

Christian Bauer, Wolfgang Fallot-Burghardt,* Karl-Tasso Knöpfle,
Valery Pugatch,† Bernhard Schwingenheuer, Edgar Sexauer,
Ulrich Trunk‡
Max-Planck-Institut für Kernphysik, Heidelberg
Martin Feuerstack-Raible, Boris Glass,§ Sebastian Hausmann,
Sven Löchner, Katharina Müller, Ulrich Straumann¶
Universität Heidelberg

Ruud Kluit   Harald Deppe, Ulrich Kötz
NIKHEF, Amsterdam   *DESY, Hamburg*
Roberto Carlin   Roberto Sacchi
Universitá di Padova   *Universitá di Torino*

ABSTRACT

This paper presents a description of the HELIX128 frontend chip family installed in the HERA-*B* silicon vertex detector and the microstrip gaseous chambers of the HERA-*B* inner tracking detector. Also the ZEUS and HERMES experiments use these chips. Results from performance evaluation, radiation tests and series wafer testing are reported. Furthermore, experience gained in over 1.5 years of detector operation is given.

1 THE HELIX128-2.2 AND -3.0 CHIPS

HELIX128-2.2 and -3.0 are 128 channel pipelined readout chips [1] [2] [3] installed in the HERA-*B* Silicon Vertex Detector and the microstrip gaseous chambers (*MSGC*s) of the HERA-*B* Inner Tracking Detector. The ZEUS Experiment uses the HELIX128-3.0 in its Microvertex Detector and the HERMES experiment uses HELIX128-2.2 chips in a vertex detector upgrade. Furthermore a version with only direct binary readout (called *CIPix*) was derived for H1's Central Inner Proportional Chamber upgrade. The chips are manufactured in AMS' CYE (0.8 µm bulk CMOS) process and have the same architectural concept as the FElix
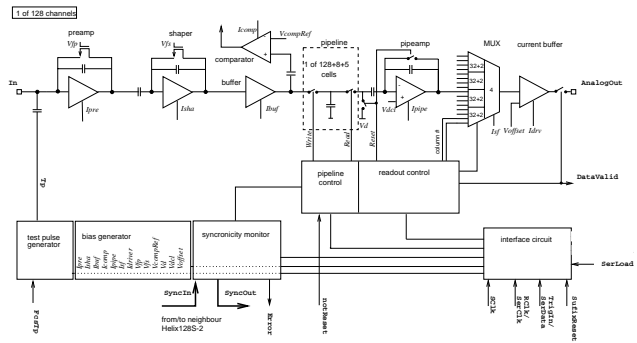
Figure 1: Schematic of the HELIX128 and HELIX128-3.0 chips

chip [4] developed by the RD20 collaboration.

As depicted in fig. 1, each input channel features a low-noise, low-power charge sensitive preamplifier (*CSA*) frontend and a shaper. These folded cascode [5] designs are optimized for 96 ns fall time to comply with the HERA bunch-crossing clock of 10.4 MHz. The output of each frontend channel feeds its signal into a capacitor array (*pipeline*) and into an AC-coupled differential amplifier type comparator circuit with a common reference voltage for all 128 channels. The outputs of these comparators are ORed together in groups of 4 channels, latched and brought off-chip via open drain pads to derive a level-1 trigger signal.

The pipeline consists of 141 cells per channel, which allows a maximum trigger latency of 128 samples and implements a derandomizing buffer for 8 triggered events. The oldest triggered event is read out of the pipeline via a resetable CSA (*pipeamp*). The signals are then serialized and

brought off-chip by means of a 2-stage multiplexer and a current driver. The output stages operate at up to 40 MHz readout clock frequency.

To control the pipeline operation, the HELIX128 uses a FIFO based circuit instead of the shift register implementations known from other readout chips [6]. It was synthesized from a functional description (written in *Verilog*), which besides scalability and portability is much smaller (wrt. chip area) than a shift-register solution. Furthermore, when implemented with standard cells, the circuit only grows $\propto \ln(n) \times m$ where n is the latency and m the number of derandomizer buffers, which store triggered events.
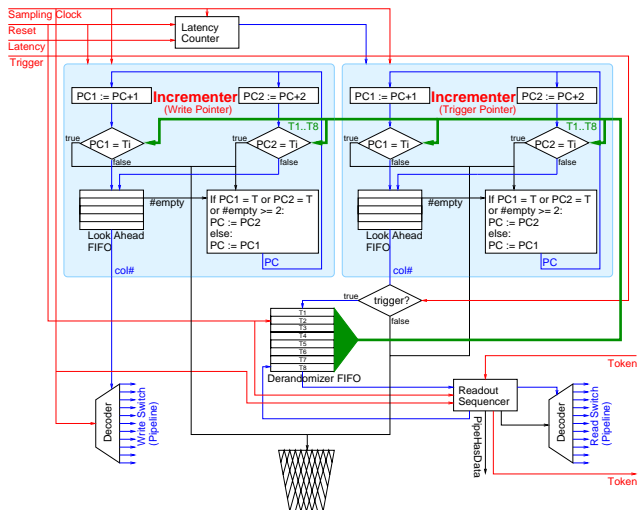

Figure 2: FIFO based algorithm of the HELIX128's pipeline control circuit

The algorithm of the pipeline control circuit is depicted in fig. 2. It mainly consists of the derandomizer buffer FIFO, and two *Incrementers*, which calculate the pipeline addresses to be overwritten or triggered respectively. The address to be overwritten is decoded to operate the pipelines write switches, and the address to be triggered is only written to a derandomizer buffer if a trigger signal is present and a free slot in the FIFO is available. Each clock cycle, the *Incrementer* compares two subsequent pipeline addresses with the contents of the derandomizer buffer FIFO. If an address is not marked for readout, it is stored into a *lookAhead FIFO*, if there is enough space. Also the pipeline addresses compared in the next clock cycle depend on the number of free buffers in the *lookAhead FIFO*. The oldest entry in the *lookAhead FIFO* is the output of the *Incrementer*.

It is obvious that in worst case this algorithm has to handle m subsequent triggered pipeline addresses, where $m = 8$ is the depth of the HELIX' derandomizer FIFO. To prevent the *lookAhead FIFO*s from underrun they have to be at least $= m/2 + 1 = 5$ buffers deep.

All amplifier stages feature forced bias currents to ensure sufficient radiation tolerance. These currents, as well as the voltages that adjust the feedback resistances of CSA, shaper, and the comparator threshold, are generated with on-chip digital-to-analog converters (8 bit resolution). The DACs, together with digital circuits adjusting the trigger latency or the pause between the readout of two triggered events, are programmed via a serial interface using the trigger line for data input.

The clock inputs for readout, sampling and the comparator circuits as well as the trigger inputs use LVDS signals to minimize crosstalk.

Pads for token and monitoring signals allow the daisy-chained readout of two or more chips and the monitoring of their synchronous operation. The HELIX128-3.0 chip also implements a fail safe token scheme, that overcomes (non-adjacent) dead chips in a readout daisy-chain. Figure 3 shows the layout of the chip. The die size is $14.4 \times 6.2 \, \text{mm}^2$.
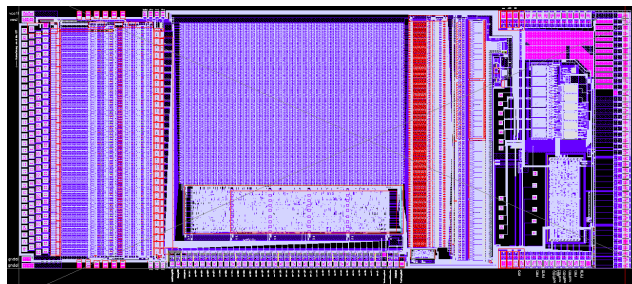

Figure 3: Layout of the HELIX128-2.2 chip

2 PROVEN RADIATION TOLERANCE AND ANALOGUE PERFORMANCE

A sample of chips was irradiated with a ^{137}Cs source up to 5.2 kGy. All chips were fully functional after accumulation of their target dose, though the high dose rate of 180 Gy/h induced a temporary failure of the digital circuits after 3 kGy from which the chips recoverd after about 210 h under normal operation conditions (i.e. T$\approx$55 °C).

Noise measurements show (fig. 4, 5) an increase from $438 \, \text{e}^- + 38.6 \, \text{e}^-/\text{pF}$ (which is in good agreement with the theoretical value of $287 \text{e}^- + 35 \text{e}^-/\text{pF}$ [2]) for unirradiated chips to $751 \, \text{e}^- + 52.0 \, \text{e}^-/\text{pF}$ after 4 kGy. No significant change of the pulse shape was found after irradiation (fig. 6). Also the power consumption of the chips was found to increase linearly with the accumulated dose from 1.8mW/Ch before irradiation to 2.6mW/Ch at 2.7kGy as shown in fig 7. The discharge of the pipeline storage capacitors due to leakage currents was found to be unaffected by irradiation up to 4 kGy for observation times in the millisecond region.

The analogue performance fully complies with HERA-*B* requirements: An undershoot-free pulse with 96 ns fall time
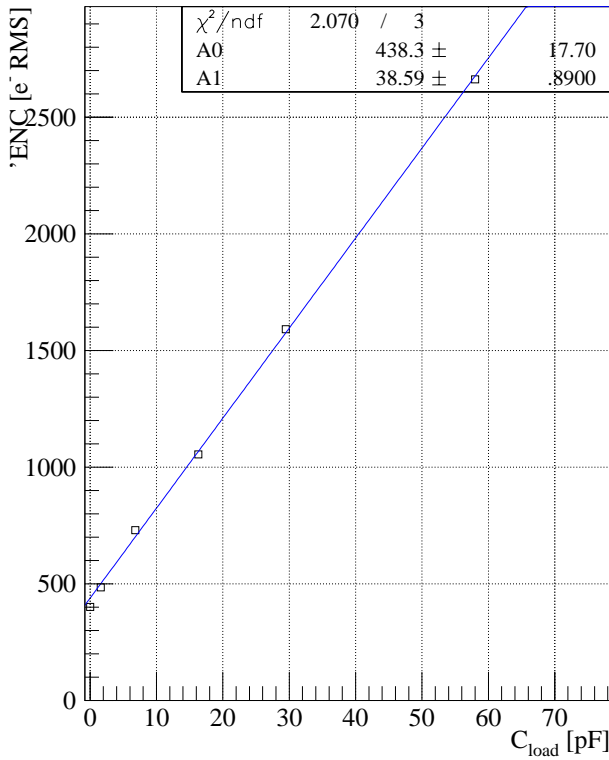
Figure 4: The equivalent noise charge (*ENC*) of a non-irradiated HELIX128-2.2. The bias settings chosen ($I_{pre} = 350\,\mu A$, $V_{fs} = 1.5\,V$) correspond to a HERA-*B*-compliant signal at 20 pF strip capacitance

Figure 5: Equivalent noise charge (*ENC*) of the HELIX128-2.2 chip for indicated input loads as a function of accumulated dose

can be achieved for input capacitances up to 30 pF, which gives a 50% safety margin. With the recommended receiver circuit, the gain of the chip was measured to be $110\,mV/MIP$ ($1\,MIP = 24000\,e^-$) without load, dropping to $80\,mV/MIP$ for 16 pF input load, both measured with fall time adjusted to $\approx 100\,ns$.

The comparator circuits exhibit a measured sensitivity of $267\,e^-$ [7]. By choosing the correct phase of the comparator- and sampling clocks, the switching noise of the comparators can be vastly suppressed on the HELIX128-3.0, where coupling via the substrate has been reduced wrt. HELIX128-2.2.

3 SERIES WAFER TESTING AND YIELD

For series testing of HELIX128 chips a setup based on a Suss PA200 semi automatic wafer prober and a digitizing HERA-*B Front end Driver* (*FED*) module was used. By employing parts of the HERA-*B* DAQ system it is possible to characterize every pipeline cell wrt. offset and gain, to store the results in a database and automatically generate test reports. The probecard (with ≈ 100 needles) restricted the sampling and readout speeds to 10 MHz, which resulted
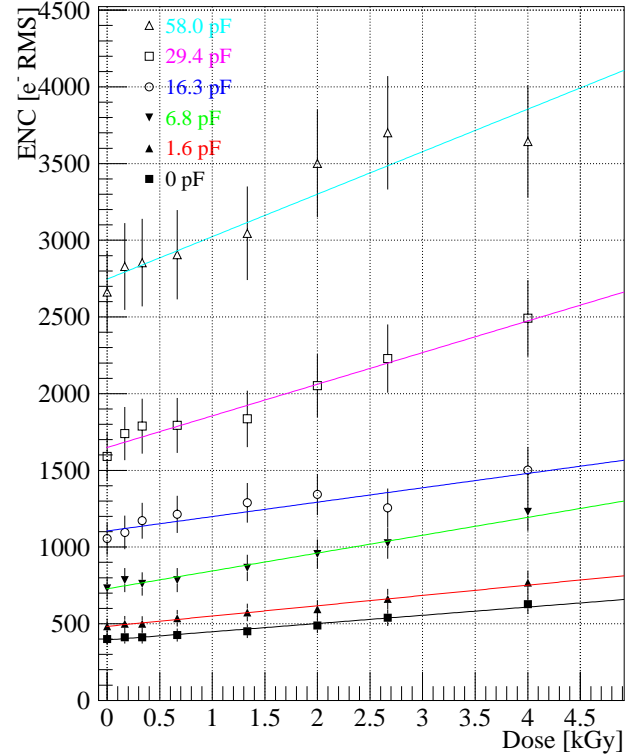
in test times of $\leq 30\,min/wafer$ (w/o loading) — much faster than 5 min/chip achieved with a HP 82000 chiptester. Up to now 107 wafers with 60 HELIX128 chips each have been tested. The yield was found to be 47% for perfect chips, which is higher than expected from process parameters.

4 EXPERIENCE FROM LARGE SCALE DETECTOR OPERATION

HERA-*B*'s Silicon vertex detector consists of 8 superlayers, each made up of 8 double sided silicon strip detector modules. The $50 \times 70\,mm^2$ detectors are segmented into 1280 strips on the *n*-side and 1024 on the *p*-side. The 7 superlayers close to the target are mounted in roman pots, that are inserted into the 2.5 m long conical shaped vertex vessel. The vessel itself is part of the HERA proton ring and also houses the wire target. Targets and roman pots can be retracted from the beam axis to avoid damages when filling the proton ring. Fig. 8 shows a roman pot, carrying one quadrant of the first three superlayers. The shielding caps covering the detectors are removed.

The first parts of this detector system went into operation in May '98. Since then an increasing number of modules have been installed. At present 44 detector modules are
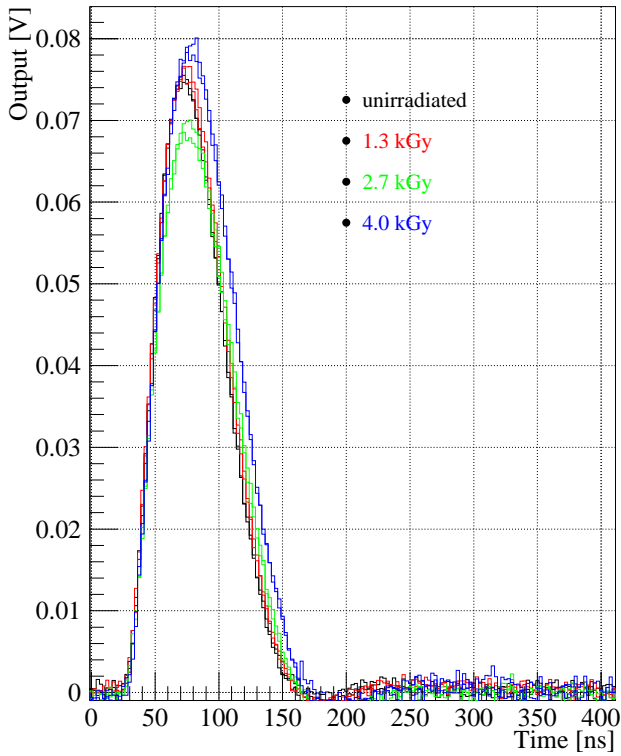
Figure 6: Pulse shapes of HELIX128-2.2 at 16.3 pF input capacitance, fixed bias conditions (I_{pre} = 350 µA, V_{fs} = 1.5 V) and indicated doses. The injected charge was $24000\,e^-$ ($\equiv$ 1 MIP in 300 µm Si)
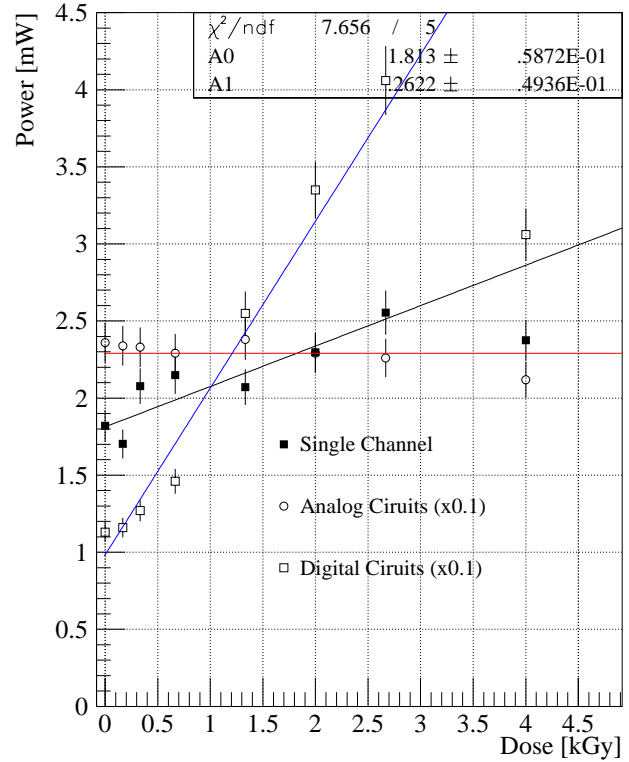

Figure 7: Power consumption of different parts of a HELIX128-2.2 chip as a function of dose. The last irradiation step to 4 kGy was performed 8 weeks after the previous irradiation step (see text). The drop between 2.7 kGy and 4 kGy indicates the dependence of the power consumption on the dose rate

installed, which equates to about 700 (of 1152) installed chips. As depicted in fig. 9 the newer detector modules nearly reach the theoretical limits for the signal-to-noise (*S/N*) ratio of 27 for n-sides and 19 for p-sides. The S/N ratio for all installed chips is shown in fig. 10.

The Inner Tracker of the HERA-*B* experiment is a large system of Microstrip Gaseous Chambers/Gas Electron Multipliers (*MSGC-GEM*), which is read out with the HELIX128-2.2 and -3.0 chips. The system is organized into ten superlayers, each superlayer consists of 8 to 24 chambers. In total about 150,000 electronic channels have to be read out.

An MSGC-GEM [8] [9] is a flat gas-tight chamber, measuring $30\times30\times1.5\,cm^3$ (w×h×d) where the rear plate is made of 400 µm thick glass with photolithographic applied anode and cathode strips at an anode pitch of 300 µm. Two G10 frames with integrated gas supply fix an intermediate double sided copper plated foil with small holes at a pitch of 140 µm between the front and rear plate of the chamber. Filled with a chamber gas the high voltage applied to anodes and cathodes as well as to both sides of the GEM foil causes electron multiplication in the respective parts of the chamber. A superimposed drift field causes the electrons generated by ionizing particles to drift via the GEM foil to the anodes on the rear plate. The Signal of such a detector,

which has a strip capacitance of 20 pF is $50,000\,e^-$ for a minimum ionizing particle.

Each chamber is read out by 6 HELIX128 chips, directly mounted in pairs on three multi-layer PCBs. The anode strips are DC-coupled to the HELIX128 chips via flexible Kapton bridges which are *z-axis glued* (i.e. the connection is established by a special glue with anisotropic conductivity) on both ends and a ceramic thin film substrate, which is also mounted on the PCB. This ceramic substrate not only acts as a pitch adapter, it also integrates resistors which are needed for high voltage spark protection.

Operation of first HELIX128 equipped chambers at HERA-*B* started in spring1999.

The only failure of the complete system encountered up to now was the malfunction of some digital optical receivers (Hirschmann OEDH 50M2) mounted $\approx$2 m from the beam axis. They turned out to act as silicon detectors for ionizing particles themselves and were replaced by analogue ones with adjustable discriminators to overcome this.

References

[1] W. Fallot-Burghardt, M. Feuerstack-Raible, B. Glass, U. Trunk, HELIX128S-2 Users Manual, HD-
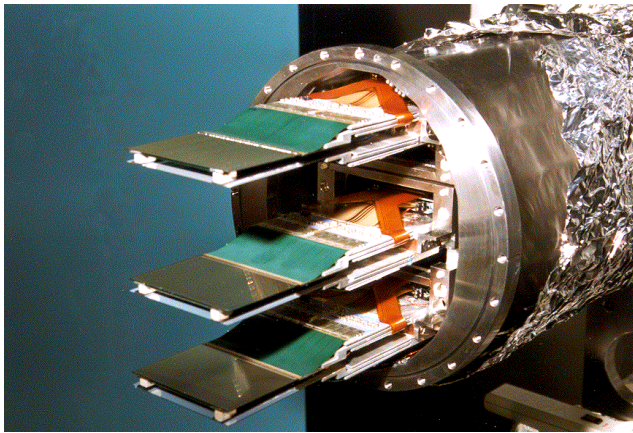
Figure 8: Detector modules covering one quadrant of the first three superlayers. The Al caps separating primary and secondary vacuum are removed to reveal (from left to right) the detector wafers, Kapton flex jumpers and the hybrids with the HELIX128 chips

ASIC-33-0697

[2] W. Fallot-Burghardt, A CMOS Mixed Signal Readout Chip for the Microstrip Detectors of HERA-*B* Doctoral Thesis, Heidelberg 1998

[3] U. Trunk et al., The HELIX128S Readout Chip Family for Silicon Microstrip Detectors and Microstrip Gaseous Chambers, CERN/LHCC/98-36 (1998) 538–542

[4] S. Brenner et al., Nucl. Instr. Methods A339 (1994) 477 and Nucl. Instr. Methods A339 (1994) 564

[5] Y. Hu, E. Nygård, Nucl. Instr. Methods A365 (1995) 193–197

[6] M. French et al., APV6-RH A 128 Channel Readout Chip for Silicon Trackers in CMS, CERN/LHCC/96-39 (1996)

[7] B. Glass, Analoge Auslese- und Triggerelektronik für Mikrostreifen-Gaszähler, Diploma Thesis, Heidelberg 1998

[8] M. Hildebrandt, Entwicklung und Bau der Detektoren für das Innere Spurkammersystem bei HERA-*B*, Doctoral Thesis, Heidelberg 1999

[9] C. Richter, MSGCs for HERA-*B*, Micro-Pattern Gas Detectors Workshop, Orsay 1999, http://www.physi.uni-heidelberg.de/groups /herab/notes.html
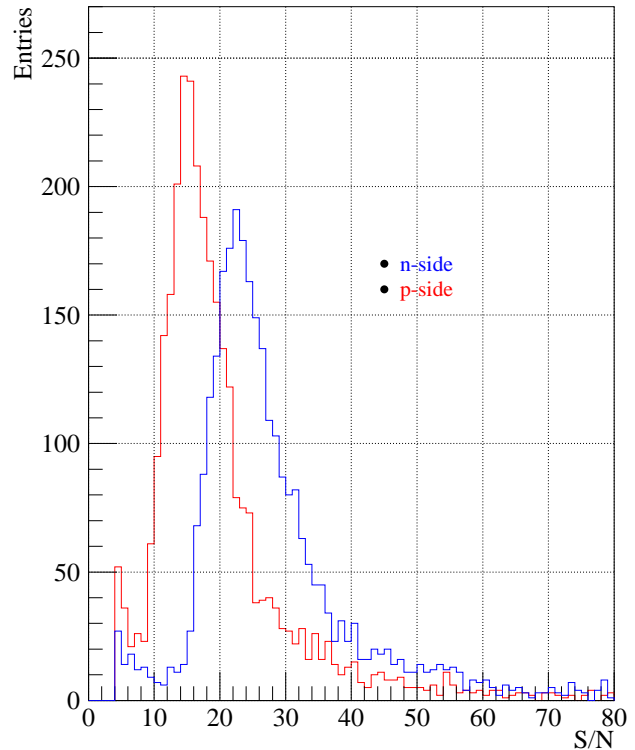
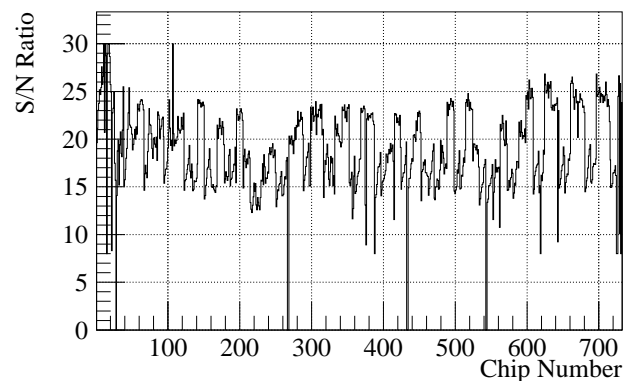Figure 9: S/N histogram for a double sided strip detector module

Figure 10: Signal-to-Noise ratio for all chips of the HERA-*B* vertex detector. The structure in the data arises from the p-n-n-p sequence of the detector sides and their different strip capacitances