The ATLAS Level-1 Calorimeter Trigger Pre-Processor

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Abstract

At the input to the calorimeter part of the Level-1 Trigger a Pre-Processor system performs the preprocessing of about 7200 analogue trigger-tower signals. The preprocessing includes digitisation, identification of the corresponding bunch-crossing in time (BCID), calibration of the transverse energy, rate monitoring, readout of raw trigger data, and high-speed data transmission to the following processors. The preprocessing of a large number of analogue signals requires a compact Pre-Processor system with fast hard-wired algorithms implemented in application-specific integrated circuits (ASICs). In this paper we present the tasks of the Pre-Processor, measurement results, and advanced technologies used for the preprocessing of about 7200 analogue signals.

1 Introduction

The ATLAS Level-1 Trigger is a fast pipelined system for the selection of rare physics processes. Its selectivity achieves an event rate reduction from the 40 MHz LHC bunch-crossing rate down to the first level accept rate of 75 kHz. The Level-1 Trigger searches for isolated electrons and photons, hadrons, jets of particles, muons, and it calculates calorimeter global energy sums within 2.0 μs latency. Hence, fast hardwired algorithms implemented in application-specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs) are required. For that reason the Level-1 Trigger is also referred to as 'hardware' trigger.

The Level-1 Trigger is divided into three subsystems, the Calorimeter Trigger, the Muon Trigger and the Central Trigger Processor (CTP). The Calorimeter Trigger gets analogue input signals from the electromagnetic and the hadronic calorimeters. These signals are summed separately in order to form trigger tower signals with a granularity of 0.1 x 0.1 in the η and ϕ directions. All in all the Calorimeter Trigger has about 7200 analogue input signals, which are transmitted electrically via twisted-pair cables from the detector to the Level-1 Trigger electronics, located in the trigger cavern. The maximum cable length for trigger input signals is 60 m. Based on these input signals the Calorimeter Trigger performs the following tasks:

- preprocessing of input signals;
- an electron/photon trigger algorithm;
- a hadron/tau trigger algorithm;
- a jet trigger algorithm;
- calculation of global trigger quantities (E_T-miss and sum-E_T).

The results from the Calorimeter Trigger are the multiplicity of showers passing transverse-energy thresholds, and the coordinates of regions of interrest (RoI). The multiplicity information is sent to the Central Trigger Processor (CTP) and the RoI data is sent

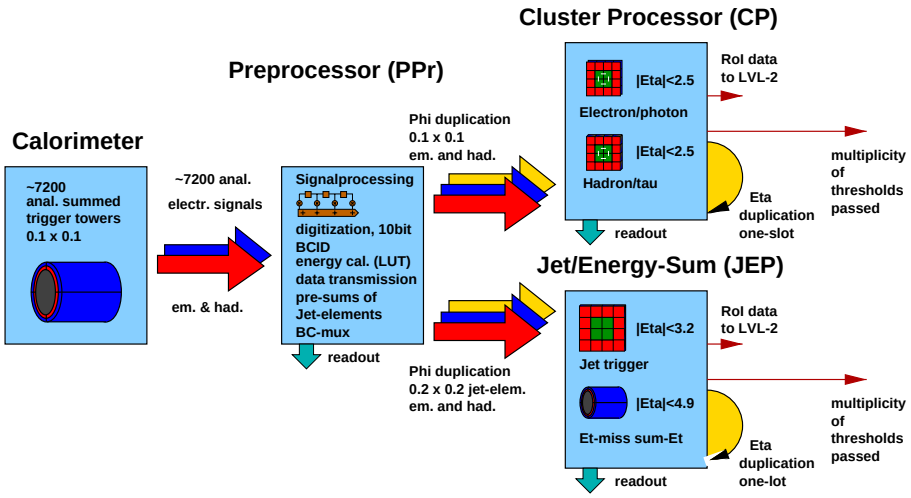

Figure 1: Overall architecture of the Atlas Level-1 Calorimeter Trigger

to the Level-2 Trigger. See Figure 1 for the overall architecture of the Atlas Level-1 Calorimeter Trigger.

A Pre-Processor Module (PPM) has 64 analogue line receivers to receive the trigger tower signals from the calorimeter. The signals are processed by commercial integrated circuits (ICs) and application specific ICs (ASICs), most of which are located on 16 Multi-Chip Modules (MCMs). A MCM combines different IC technologies, e.g. analogue and digital components to increase the die to package-area ratio. Inside each MCM, four ADCs digitise the analogue signals to 10-bits. Two Pre-Processor ASICs (PPrAsics) perform the BCID algorithm, the transverse-energy calibration to 8-bits in a look-up table, and the pre-summing of jet elements. It also contains pipeline memories to store trigger data up to 2 μs, until a level-1 accept signal arrives from the CTP initiating the readout. Codes for the detection of transmission errors are generated before trigger tower data are serialised to 800 Mbit/s using gigabit links manufactured by Hewlett Packard (G-links). LVDS links from National Semiconductor may be used instead. A bunch-crossing multiplexing scheme, which doubles the effective bandwidth of the high-speed serial link, is used for the transmission of preprocessed trigger towers to the CP. Pre-summed jet elements are serialised on the MCM and linked to the JEP with 9-bit resolution. The ϕ-duplication of links at quadrant boundaries is fanned out to cable drivers. The readout data from all PPrAsics are collected by one Readout Merger ASIC (RemAsic). This ASIC interfaces to a custom ring-like bus on the backplane (PipelineBus), which shifts readout data via a readout driver board to the readout buffers. Slow control is used to set up the configuration and to load test data.

2 Tasks of the Pre-Processor

The Pre-Processor is of importance for the running of the ATLAS experiment, because all the Level-1 Calorimeter Trigger input data have to pass through it. The tasks that the Pre-Processor system has to perform, based on its input signals can be summarised as follows:

- **Preprocessing:** Provide the trigger processors downstream with digital data containing the transverse energy deposited, identified with the corresponding bunch-crossing. For the Cluster Processor (CP) the granularity is 0.1×0.1 for $|\eta| < 2.5$ and for the Jet/Energy-Sum Processor (JEP) the granularity is 0.2×0.2 for $|\eta| < 4.9$. In both cases the input data are separate for the electromagnetic and the hadronic calorimeters.

- **Readout of event data:** Raw trigger data from the Pre-Processor are needed to tell what has caused a trigger and to allow monitoring of the performance of the trigger system.

2.1 Preprocessing tasks

The preprocessing tasks are illustrated in Figure 2 for the processing of one trigger tower signal. The prepro-

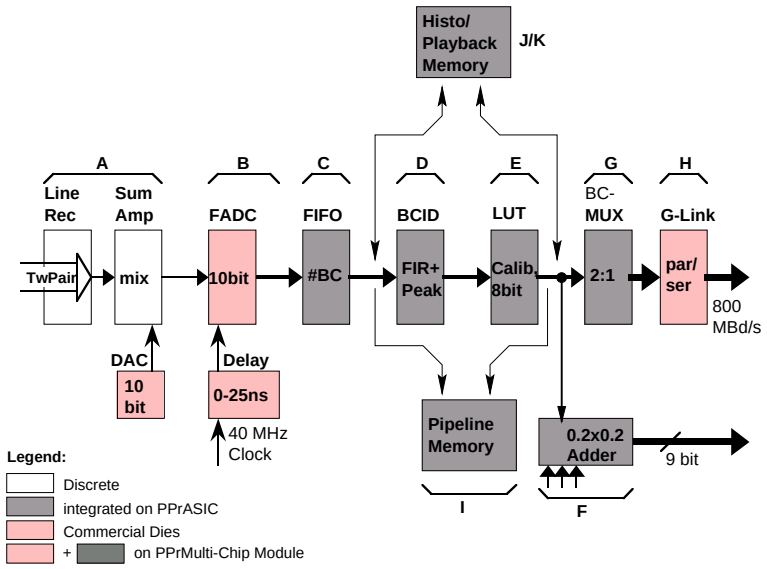

Figure 2: Preprocessing of one trigger tower signal by the Pre-Processor [TDR98].

cessing steps are marked as **A** to **H** and are described as follows:

A: Reception of analogue trigger tower signals: The differential analogue trigger tower signals are received by a differential line receiver circuit. The input voltage range is linearly mapped, with 0–2.5 V representing 0–250 GeV. A programmable DAC with 10-bit resolution is used to adjust the zero baseline for each input signal.

B: Digitisation and phase adjustment: Each analogue input signal will be digitised by a flash analogue-to-digital converter (FADC) with 10-bit resolution. The time position of the sampling strobe with respect to the analogue input signal can be adjusted in steps of 1 ns within a range of 25 ns. This is required to perform the fine synchronisation of each trigger tower signal and to sample each pulse at its maximum. An ASIC (Phos4) developed by the CERN Microelectronics group will be used for this time adjustment.

C: Synchronisation: The digitised data needs to be synchronised to the same bunch-crossing, because of different time-of-flight for particles from the interaction point to the calorimeter and the different cable lengths from the calorimeter to the trigger cavern (USA15). Synchronisation is done in steps of 25 ns by a FIFO with a programmable depth of 16 bunch-crossings. Assuming a cable propagation delay of 5 ns/m, this corresponds to the delay of an 80 m long cable. This includes enough contingency because the actual cables are not going to be longer than 60 m.

D: Bunch-crossing identification (BCID): This circuit consists of two algorithms to identify the transverse energy deposition represented by a trigger tower signal, and the corresponding bunch-crossing in time. One algorithm is applied to non-saturated signals and one is applied to saturated signals.

E: Lookup table: A lookup table is used to fine-calibrate the digitised data to the deposited transverse energy E_T. It maps the 10-bit data after BCID to 8-bit, with a least significant bit (LSB) of 1 GeV. In addition, it can be used to subtract a pedestal and it can apply a minimum threshold to suppress noise.

F: Formation of jet elements: The Pre-Processor pre-sums four 8-bit trigger towers to coarser jet elements with a size of 0.2×0.2. The summing is done separately for the electromagnetic and the hadronic calorimetry, leaving the option to apply separate jet thresholds for electromagnetic and hadronic clusters in the Jet/Energy-Sum Processor. The summing tree in the Pre-Processor requires all four inputs for a jet element to be in adjacent trigger tower channels. The resolution

for the jet elements is reduced to 9-bit accuracy, with a least count of 1 GeV, before transmission.

G: Bunch-crossing multiplexing: This transmission scheme (BC-mux) doubles the effective bandwidth of the serial links to the Cluster Processor. In case of a G-link transmitter/receiver chip-set the number of links is only 2166 instead of 4332, with each G-link carrying four trigger-tower signals. This BC-mux scheme can not be used for the transmission of jet elements to the Jet/Energy-Sum Processor because the presumming removes empty bunch-crossings.

H: Serial data transmission: Preprocessing results are sent to the downstream processors via high-speed serial links. A high-speed serial transmission is required to keep the number of data links to an acceptable value. The feasibility of a serial data rate of 800 MBd was demonstrated using the G-link chip-set. Because of the high power dissipation of G-links, LVDS links will probably be used for the final system.

2.2 Readout tasks

The Pre-Processor provides pipelined readout of raw trigger input data as well as E_T values after the lookup table in order to tell what has caused a trigger and to provide diagnostic information. It allows the monitoring of the performance of the trigger system and the injection of test data for trigger system tests. These tasks are marked as **I** to **K** in Figure 2 and are described as follows:

I: Pipelined readout: The function of the readout pipelines in the Pre-Processor is equivalent, but independent of those of the detector readout. The Level-1 Trigger captures its own event data as soon as it has triggered. Two sets of pipeline memories capture event data in the Pre-Processor. One records the raw FADC data at the Pre-Processor input and one records after the lookup table and BCID. The number of time slices around an accepted event can be preset to read up to 128 time slices. Without introducing deadtime to the readout, the identified bunch-crossing and two time slices around can be read out.

J: Data playback: The Pre-Processor, comprising 7296 input channels, can inject data for technical tests of the Level-1 Trigger system. This allows testing the functioning of the trigger processors and the relative timing of the processors and the input channels.

K: Histogramming: This is a useful feature for monitoring of the trigger performance. Two modes of 'online' trigger monitoring are foreseen for each trigger tower input at the Pre-Processor. The first mode is *rate monitoring*, where entries in a histogram above a programable threshold are counted for a given time duration. The second mode is used for monitoring of the *transverse energy spectrum* of either the raw FADC data or the energy calibrated output after the lookup table and BCID. The latter mode allows the monitoring of a 'bunch window' out of the 2961 LHC bunches in one turn.

3 Measurement results

This section describes measurement results as part of a modular Pre-Processor test system. The aim was to demonstrate the functioning of the demonstrator MCM, with all its real time preprocessing and its high-speed serial data transmission of trigger tower data. The MCM test set-up consists of two VME motherboards, each equipped with a CMC daughter card. One Motherboard carries a Pre-Processor CMC card and the other one carries a G-link receiver CMC card. As input to the Pre-Processor card, a liquid argon-shaped calorimeter signal was generated by an Arbitrary Function Generator (AFG).

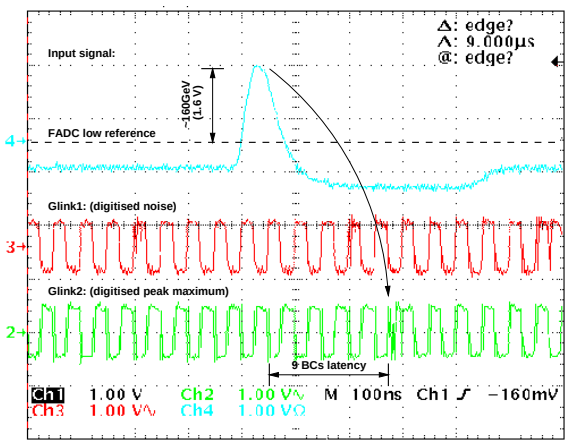

Figure 3: Correlation of the analogue input signal with the high-speed serial bit-stream (G-link signal).

The input signal is processed by MCM components in the following way: first it is digitised to 8-bit pre-

cision, next, a Pre-Processor ASIC prototype (FeAsic) performs BCID for non-saturated trigger-tower signals, and then a Finco ASIC converts logic levels from TTL to PECL before the data are serialised at 800 MBd by the G-link transmitter chip. The G-link output signals from the Pre-Processor CMC card were connected via a 1 m long coax cable to the G-link receiver CMC card. The G-link receiver decodes the serial bit-stream and provides the parallel output data to a motherboard FPGA. The FPGA latches the G-link data from two G-links (2×16 bits) and writes the data to the motherboard dual-port memory. This is done at a speed of 40 MHz.

Figure 3 shows the correlation of the analogue input signal with the high-speed serial bit-stream. The bunch-crossing-identified data occurs after a latency of 9 bunch-crossings (225 ns) in one G-link bit-stream. This latency attributed as follows: one tick from the FADC, seven ticks from the FeAsic, and one tick from the G-link.

4 Multi-Chip Module technology

A demonstrator Multi-Chip Module (PPrD-MCM) was successfully designed and built (See Figure 4 for a picture). It includes most of the final preprocessing and the readout of the Calorimeter Trigger, for four trigger tower signals. The preprocessing includes digitisation to 8-bit precision, identification of the corresponding bunch-crossing in time (BCID), calibration of the transverse energy, readout of raw trigger data, and high-speed serial data transmission to the Calorimeter Trigger processors.

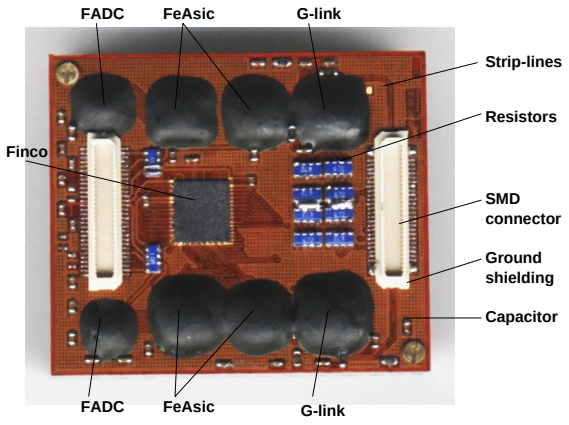

Figure 4: Demonstarator MCM picture.

The MCM has a size of 4.3×3.7 cm^2 and it consists of 9 dies. The MCM was designed with a smallest feature size of 100 μm and it was fabricated in a laminated MCM-L process. It was tested as part of a modular Pre-Processor test system, where transmission and readout tests have shown the feasibility of building a compact Pre-Processor system. Reliability and temperature aspects have been investigated. The clocked MCM temperature is about 42.5 °C, with variations from chip to chip. The un-clocked MCM mean temperature is 34.6 ±1.5 °C (See Figure 5).

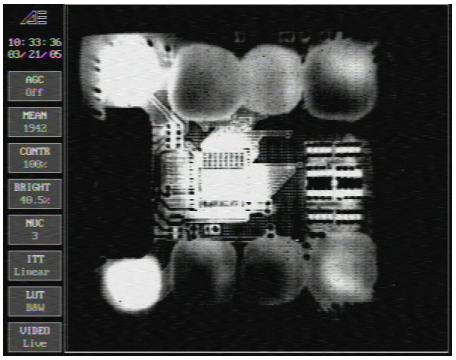

Figure 5: Infrared picture used for temperature measurements.

5 Conclusions

The measurement results described here have demonstrated the functioning of the demonstrator MCM. For one analogue trigger-tower signal, most of the preprocessing has been shown. This includes all the preprocessing from the analogue line receiver circuit up to the reception of high-speed serial data at 800 MBd. The established MCM design technique and experience will now be used for the final Pre-Processor Multi-Chip Module. All Details about the final MCM will be specified and then the MCM size can be optimised to fit 16 PPr-MCMs on a VME board aimed to process 64 trigger tower signals.

References

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