The Electronic calibration of the ECAL-CMS

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Abstract

We present a calibration system developped at LAPP (Annecy-le-Vieux, France) for the electronics of the CMS electromagnetic calorimeter. The system, remotely controled from the control room, produces a current pulse at the input of the preamplifiers of the read out chain. The pulse amplitude is fixed by a 10 bits DAC and its shape has an exponential decay. It has been founded in DMILL 0.8μm technology. For the injection part, no shift is measurable up to 10^{14} neutrons/cm^2 and 400 krad in γ irradiation. We describe here the system, the different chips that have been founded and the results of the measurements.

1 Introduction

The CMS electromagnetic calorimeter has been designed in such a way that both the front end electronic and the digitization be close to the $PbWO_4$ crystals. This strategic choice imposes the electronics to be radiation hard. The chip we have developped is able to build individual calibration pulses at the input of each amplifier. This calibration will be used during data taking in order to correct eventual drifts in the read out chain due to radiation damages, temperature hazards etc...The chip is composed of 3 parts: the command (Test Pulse Logical System (TPLS), the DAC and the injector.

2 The TPLS

2.1 Functionnality

The TPLS selects the orders for calibration, charges the amplitude of the DAC and triggers the injector. Its functionnality has been described in Verilog language and synthetised with the DMILL library.

2.2 Foundry and measurements

The first prototyte has been submitted in February 1999 and tested in July. A specific VME card has been developped, controlled by a PC and LabView. The output were transmitted to a logical analyser HP1662C. The result is shown on figure 1 and 2.

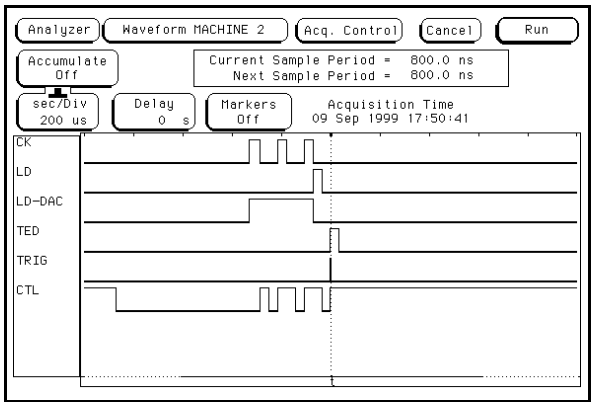

Figure 1: TPLS analyser results.

The TPLS reacts in 3 steps to orders:

- Coding of the amplitude for the DAC.
- On reception of a specific bit (LD), it loads the

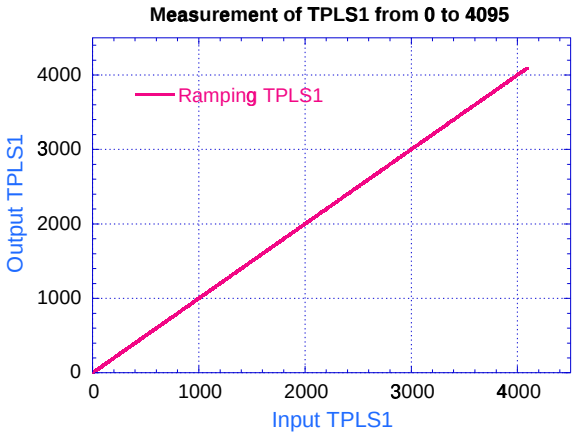

Figure 2: TPLS ramping: output code vs input code

DAC and unset the LD-DAC bit.

- On reception of a bit (TED) a 428 ns window triggers the injector.

In the preceeding prototype, an error bit was set in case of error in the received protocol. This was removed in the present one due to the fact that this information could not be sent back to the control room. In case of error, the maximum amplitude is loaded whatever the received order, and a trigger is sent to the injector.

3 The DAC

In order to determine the amplitude of the pulse, a 10 bit DAC has been designed at LAPP and sent to foundry in August 1999. The aim was to obtain:

- 10 bits resolution
- A 10^{-4} precision in a range 0 to 1 V.
- a maximum output current of 20μA.

The DAC is composed of a band gap voltage that produces a stabilized voltage and a R-2R network.

3.1 The Band-Gap

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For the band-gap (see figure 3), we started from a scheme previously developped by CERN for the

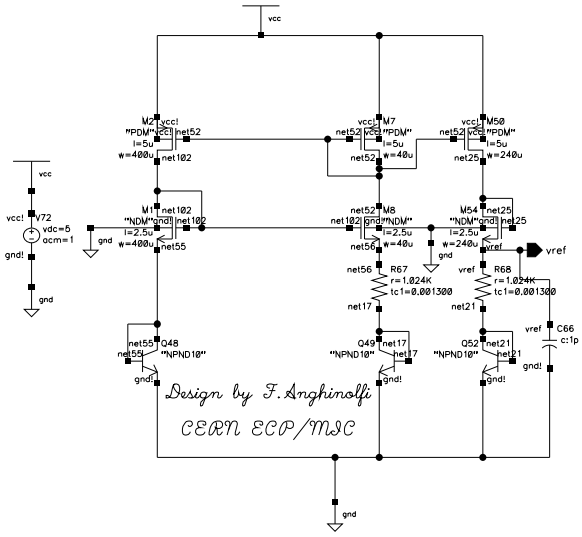

Figure 3: Band-gap scheme.

ATLAS tracker which was modified in order to increase the output current. For this purpose, we added a follower stage with the eventual drawback of an offset drift with temperature. The drift temperature of this new setup is $250\mu V/^0C$, constant from 20 to 75^0C.

3.2 The R-2R network

For the divider part, because of known instabilities under irradiation of current mirrors structures, we have choosen a R-2R network (figures 4 and 5).

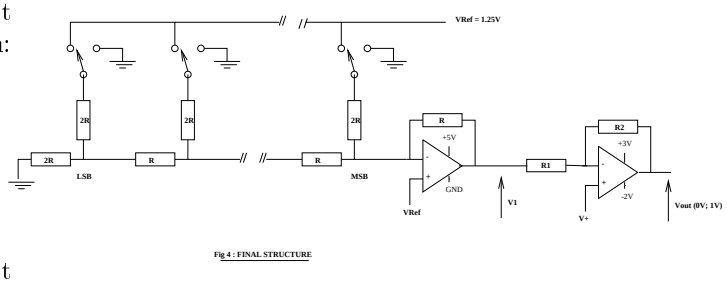

Figure 4: R-2R structure.

We had to face 2 problems:

- The stability of the system around 0 V (due to the fact that we had a 0-5V power supply). It was thus impossible to implement a common

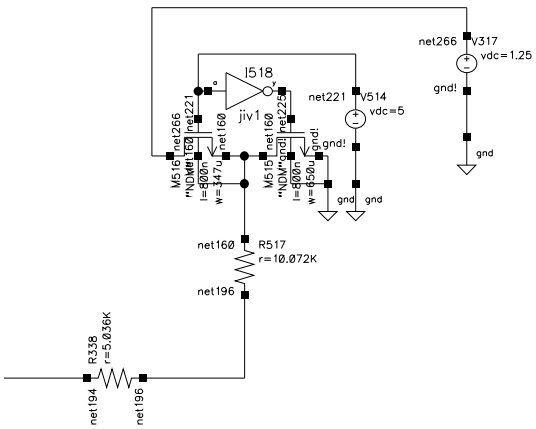

Figure 5: R-2R cell.

R-2R network with a $-V_{cc}$, $+V_{cc}$ supply current amplifier. This required a modification to run in linear mode far from the middle of its power supply range.

- The existing architecture did not fulfill our precision requirements in the low output range and we had to add a -2 V power supply which was anyway required by some other chips developped in HARRIS technology. Finally, the circuit is supplied with a -2 +3V.

Identical resistors were used to compensate the dispersion, on the other hand the Ron switch was modified in order to minimize the bulk effect. With a zero offset ideal amplifier, the simulation results are:

- An accuracy of 10^{-5} up to bit 6 , 10^{-4} for bits 6 to 9 and 10^{-3} for bit 10.
- The integral linearity error (greatest difference between the code value multiplied by the step and the output voltage) is $72\mu V$ between codes 255 and 256.
- The differential linearity error (difference between 2 consecutive steps) is 1.034 mV (1.034 LSB).

The DAC response is monoteous, its gain 1 in respect with its accuracy. The rise time from 1 to 1023 is 5 ns.

Several sources of drift have been simulated with no measurable effects: 5% in Rsquare values, resistors voltage drifts (2200ppm/V for $\Delta V = 800mV$), resistor temperature drifts (1300 ppm/K).

3.3 The amplifier.

The original circuit was based on a bipolar Darlington as input stage with an operationnal point at 2.5V. We implemented a PMOS input stage to lower the operational point at 1.25 V, suppressed the now useless Darlington structure and modified the compensations in order to stabilize it at gain 1. The results of simulation (see figure 6) are :

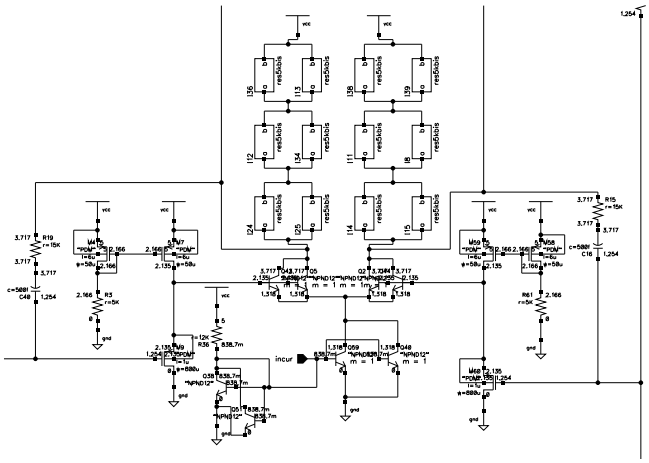

Figure 6: Amplifier.

- The gain 1 is obtained for 38 MHz, with a 100^0 phase, so that it is a first order circuit till the unit gain that insures a good stability.
- The open-loop gain is 39000.
- The offset is $4\mu V$.
- The band width is 1 MHz.
- the Power Supply Rejection Ratio (PSRR) goes from -123 dB to -18.43 dB (1/10 of the signal at 10 MHz).

3.4 Layout report

It is a 12220 full custom components circuit. Its size is 1.1 mm^2 (core size). Special care has been taken in the implementation of the R-2R network.

In order to reduce dispersions, we designed a very symmetrical network, including dummy resistors around it, and we calculated very precisely the ratio R-2R, including the metallic connections of the resistances.

3.5 The simulated characteristics

- Accuracy and linearity : the amplification stages do not lower the R-2R network performances.
- The DAC is monotonous
- Technological dispersions : The non linearity goes from .05% in worse cases to .024% in best cases.
- The power consumption is about 70mV.
- The noise is $65\mu V$ on 1 MHz band width
- Signal to Noise ratio : 15 for LSB
- Power Supply Rejection Ratio : from -88.5 dB to -17. dB at 10 MHz.
- Output Voltage 0 to 1 Volt.
- Output current $20\mu A$.

4 The Injector.

The injector produces a current pulse, with an amplitude determined by the DAC and has an exponential decay shape. A first prototype in AMS $0.8\mu m$ technology has been founded in September 1998 to validate the principle; then a first prototype in DMILL technology has been founded in October 1998, a second prototype in February 1999 and a last prototype in August 1999. In it's final version, it triggers at the same time the 5 channels of the same front-end card, with the same amplitude.

4.1 Principle

The scheme of the circuit is shown in fig 7.
The chip is composed of 3 parts:

- The input operational amplifier isolates the injector from the V_{DAC} input. It copies precisely V_{DAC} on R_{ref}.

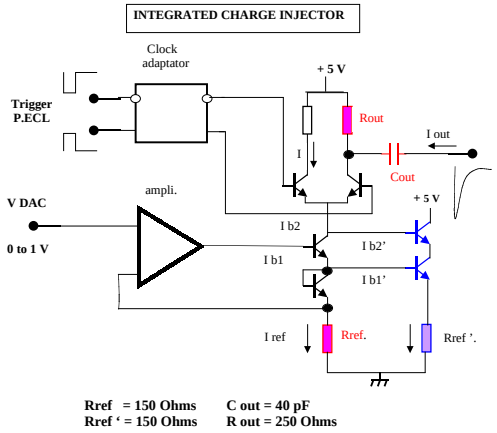

Figure 7: Principle of the injector.

- The command stage is designed in PECL logic. It is mainly a clock adaptation of the logical levels to the output differential commutator and an isolation from the input stage command.
- The output stage, when triggered, topple the conduction from the left to the right branch and the capacity C_{out} is charged through R_{out} and the preamplifier. The shape of the signal (fig. 8) is close to the one produced by the APD reading the PbWO4 crystal. The branch at the left hand (with R'_{ref}) compensates the base leak currents I_{b1} and I_{b2} so that I_{out}=I_{ref}.

4.2 Measured characteristics

The deviation to linearity of Q_{out} versus V_{in} (output charge vs command voltage) is better than 210^{-3} up to V_{in} = 1 V, corresponding to a physics dynamic range up to 3 TeV.

- Q_{out} excursion : 0 to -70 pC.
- V_{in} excursion : 0 to +1 Volt.

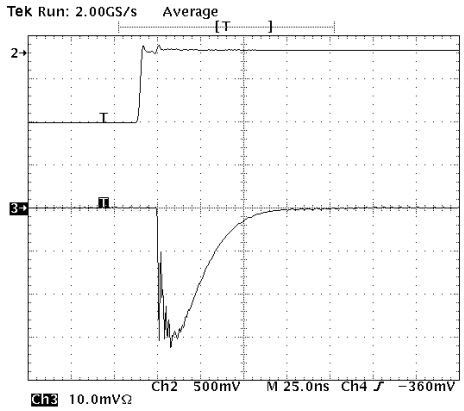

Figure 8: Output signal.

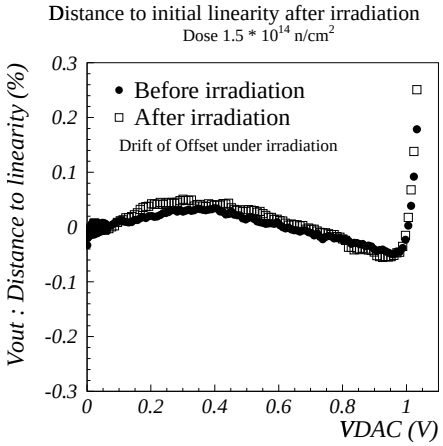

Figure 9: Deviation from linearity versus radiation dose.

- Voltage supply : 0, +5Volts.
- Power dissipated = 22mW.
- Noise output: $10\mu V$ RMS, 2.5 nV/Hz max.
- Linearity : $\pm 0.2\%$ from 2 GeV to 3 TeV equivalent.

Extensive irradiation tests have been performed on several neutron beams and gamma sources (SARA, Grenoble, France; CERI, Orleans, France and PSI, Villigen, Switzerland). The variation of the parameters of a linear fit on ramping during irradiation are shown in figures 9, 10 and 11.

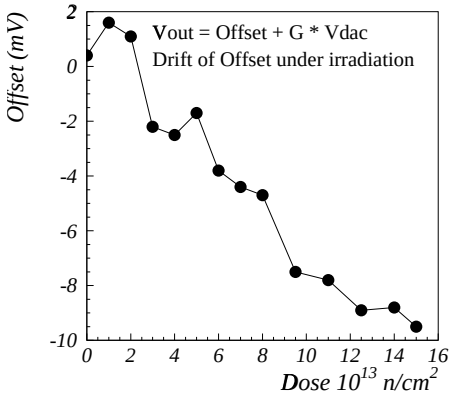

Figure 10: V_{out} offset versus radiation dose.

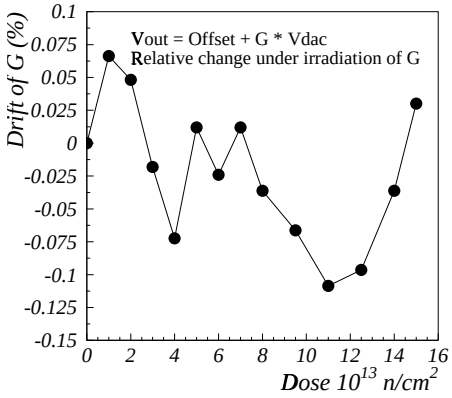

Figure 11: V_{out} gain versus radiation dose.

5 Conclusions

The CMS ECAL requirements have never been achieved on any calorimeter. The calibration will be a long and complex process. Our calibration system by charge injection will help to insure the precision of the read out chain during data taking and to debug the detector at the first stages of the installation.

The challenge to be reached by this system is to be more precise and more stable in time than the read out chain with adding a minimum noise to the data read out.

6 Acknowledgements :

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