FPGA Design in the Presence of Single Event Upsets

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Abstract

We have developed a prototype data link board in order to test Single Event Upset mitigation techniques in a programmable logic device and to investigate the adequacy of the selected devices for the ATLAS Front-End links. We used only commercial off the shelf (COTS) devices on which radiation tolerance data was available. Different digital design methods for transient error elimination in an FPGA will be compared and radiation tolerance of the serialiser and media interface will be tested. Our card can also be used as a simplex S-LINK Link Source Card using G-LINK as physical layer with optical or electrical media.

1. INTRODUCTION

In recent years great advances have been made in the field of programmable logic technology. While once Programmable Devices (PLD) were mostly applied to prototyping, logic emulation systems and extremely low volume applications, they now are used in a number of high volume devices, and in exotic applications in hostile environments like radiation or high temperature.

Front-end links are used to transfer data from electronics systems placed on detector to off-detector read-out drivers. Some functions, like high speed serialising can not be implemented in PLDs due to speed limitations. It is probable that the detectors will use commercially available or ASIC devices for such functions. Calorimeters and Muon Detector could use programmable devices as gluelogic devices which interface between standard components and detector specific interfaces.

Some programmable logic devices, like most antifuse based FPGAs, are tolerant to the low or moderate radiation dose rates which are present at calorimeters and Muon Detector ATLAS Front-End link locations. However, these chips may have transient errors termed Single Event Upsets (SEU) caused by energetic particles.

2. SEU IN DIGITAL LOGIC CIRCUITS

A Single Event Effect (SEE) is defined as any measurable effect to a circuit due to a nuclear particle strike.

A Single Event Upset corresponds to a soft error (data corruption) appearing in a device due to the energy deposited in silicon by an ionising particle. High energy protons and neutrons are also known to produce ionisation effects indirectly through nuclear reactions within the silicon [1].

SEU is a non-destructive phenomenon, which concerns in general every memory element temporarily storing a logic state. Typical examples of circuits affected by SEU are random access memories, registers, microprocessors, programmable logic devices, digital signal processors, etc (Figure 1).

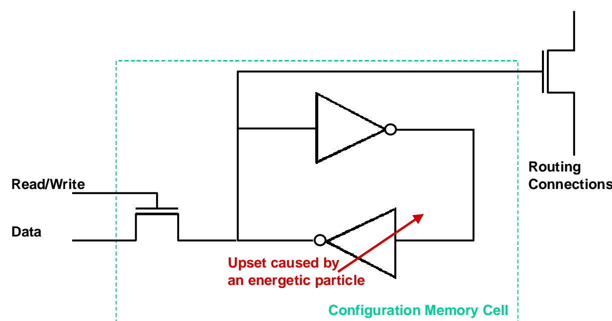

Figure 1: An SRAM configuration element (switch) in a programmable device

3. SEU MITIGATION METHODS

System-level SEE requirements based on functional impact may be fulfilled through a variety of mitigation techniques, including the use of hardware, software and device tolerance requirements. All of the potential SEE mitigation methods may require that either additional hardware or software be added to the system design.

Hardware or software design may serve as effective mitigation, but design complexity may present a problem. The most cost efficient approach of meeting a SEE requirement may be an appropriate combination of SEE-hard devices and other mitigation.

It is convenient to classify system level SEE effects into two general categories: those that affect data responses of a device, and those that affect control of a device or system. When using programmable or semi-custom circuits it is not evident how to divide devices into categories like data or control related units. Today's complex FPGAs allow a whole system to be implemented within a single chip, including data related

subcircuits like RAM, FIFO, encoding or decoding circuits and control related functions like signal processors, state machines or counters. This means that different mitigation technologies have to be used within the same device.

3.1 SEE Propagation Analysis

A SEE may propagate through a circuit, subsystem and system, thus making system-level impacts an important consideration. SEE propagation analysis is the science of determining the effect and potential risk that the occurrence of a SEE has on the device where the event occurs, on its associated circuitry and subsystem. For example, a SEU occurs in a serialiser of a data link causing a single flip in a data bit. This "invalid" data sample may provide a false observation of an event, which may significantly modify the results of the data, analysis.

3.2 Mitigation of Memories and Data-Related Devices

Error detection and correction (EDAC) offers a method for trading bandwidth for error rate. Incorporating EDAC in a link adds logical complexity and a certain amount of latency to the system. Replacement of failed memory parts with scrubbing is an other emerging technique.

The simplest, but "detect only" EDAC method is the use of parity checks. Another common error detection method is called cyclic redundancy check (CRC). CRC detects if one or more errors are occurred in a given data structure. Hamming code is a simple block encoding that will detect the position of a single error and the existence of more than one error in a data structure. Reed-Solomon codes are capable of correcting consecutive and multiple erroneous bytes. Convolutional codes can correct isolated burst noise in a data stream [2].

3.3 Mitigation of Control-related Devices

The techniques described in the previous section are useful for data SEUs. They may also be applicable to some types of control SEUs. A memory that stores program or configuration data for a microprocessor can be an example.

Watchdog timers may be implemented in both hardware and software and are used to indicate the health of the devices by sending a message from one system location to another. If the message is not received by the next location within a set time period, a time-out occurs and an action is launched to repair or replace the faulty block.

Redundancy between circuits or subsystems is an effective method on both flip-flop and system level. Switching between redundant subcircuits can be done by voting or by a higher level intervention. In some reprogrammable FPGAs a redundant system may be implemented with a very low overhead by reserving free resources. A place and route tool would be invoked to search for a new placement for the failed parts [3].

4. A PROTOTYPE DATALINK CARD

Our card (Figures 2, 4) can be used as a Test Data Generator for on-line radiation testing or as a simplex S-LINK [4] Link Source Card using the HP G-Link [5] as physical layer. The circuit's actual function depends on the configuration of the FPGA. The aim of this project was to develop a circuit board in order to test a candidate programmable logic device (PLD) for implementing a radiation tolerant digital datalink.

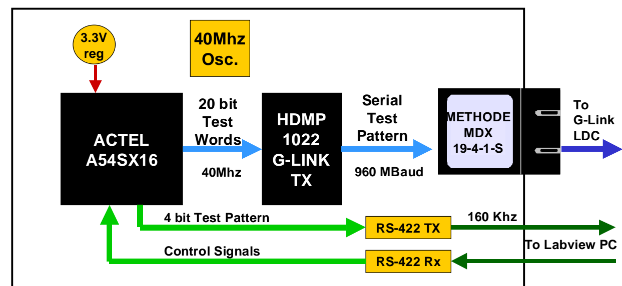

Figure 2: Block diagram of the test card

4.1 Test Data Generator Mode

If the FPGA is configured as test data generator (Figure 3), two independent data paths can be used to check the correct functioning of the card. With this configuration the card requires three control signals on its differential (RS-422) inputs which select test patterns or reset the card.

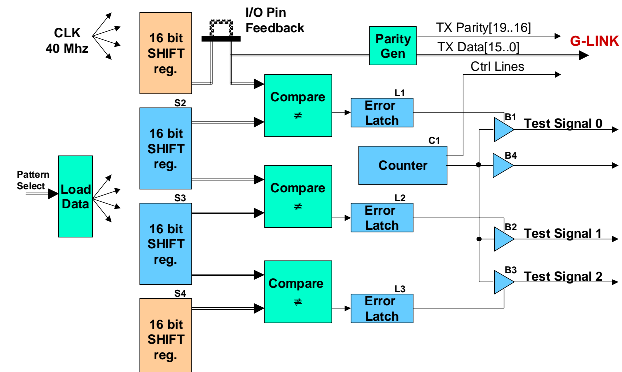

Figure 3: Test Data Generator Configuration

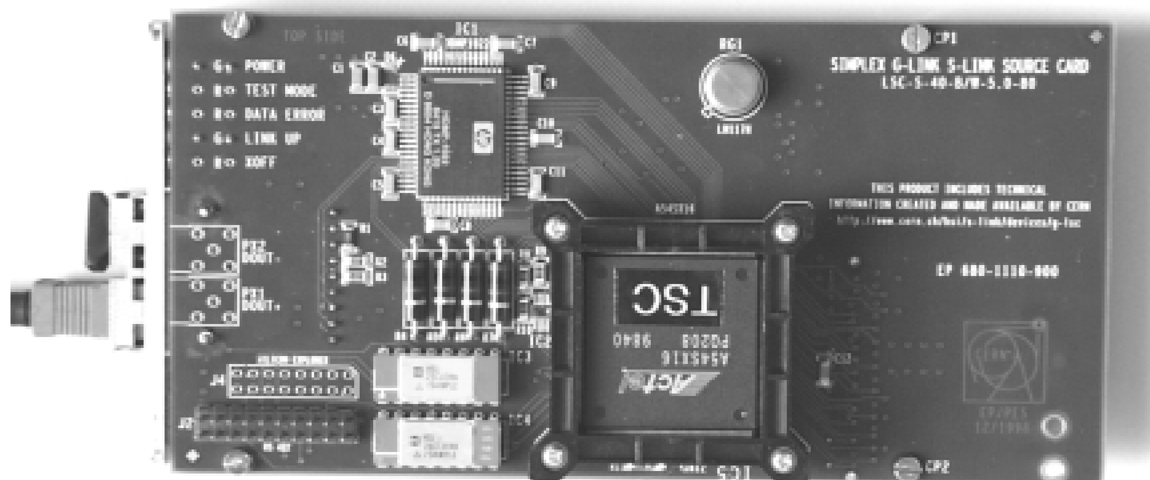

Figure 4: Test Data Generator / G-Link Based S-LINK Link Source Card

Four different test patterns can be generated by the loadable circular shift registers. To test the internal functioning of the PLD, four shift registers are implemented. Two of them are made from triple modular redundant (TMR) flip-flops to reduce SEU probability. We chose this mitigation method because TMR is an effective mitigation method on flip-flop level, the circuit operation does not stop temporarily in case of an error which is important in a data link application and this method is supported by some design tools. One data path is sent to and fed-back from device pins to test the I/O circuits as well. The data patterns at the outputs of the shift registers are compared in each clock cycle. If no errors have occurred, the comparison result will be true. If a SEU occurs in one of the shift registers, in the I/O feedback path or in the comparator, the result of the comparison will be false.

Since the signalling speed is limited on the twisted pairs going to the control room, multiple words are compared in one "test period" and a latch is toggled if one or more comparison errors occur during this time. The length of a test period is 6.4 µs. At the end of each test period a "control pulse" is sent from a counter on one twisted pair. Similar, "test" pulses are generated on the three other twisted pairs in case no comparison errors occurred during the test period. The theoretical error probability (the probability that the pulse is missing at the end of a test period) is different on each line. This method ensures a slow signalling rate on the twisted pairs and full speed operation of the internal logic circuits. The clock frequency is 40Mhz, which is the read-out frequency of most ATLAS Front-End links.

The second data path serves for monitoring the joint functioning of the FPGA, serialiser and media interface. The test pattern generated by the FPGA is framed into 224 word packets, which start and terminate with a control word and are sent to the G-Link serialiser with four parity bits. The serialised data is transmitted using optical (standard 9-pin transceiver) or electrical media (Lemo connector) to the receiver.

4.2 S-Link Source Card Operation Mode

In case the FPGA is configured for S-LINK Source, the card serialises the data on its FIFO-like 16- or 32-bit parallel interface and transmits it via electrical or optical media. The simplex G-LINK LDC can be used to receive the data.

This simplex S-LINK is capable of transferring 16-bit serial data continuously at a 40 MHz clock frequency using four parity bits and the G-Link coding scheme for error detection.

5. RADIATION TEST SETUP

The irradiation started on the 1st of June, 1999. The test zone is settled along a secondary beam line of the CERN Super Proton Synchrotron (SPS) accelerator, downstream of a particle-conversion target [6]. The radiation field is typical of a proton accelerator; it includes mainly gammas and neutrons, plus some high-energy particles.

5.1 FPGA Test Signals

The test signals are processed in the remote control room by a PC with a National Instruments PCI-DIO-32-HS high speed digital I/O module. Data acquisition and error detection is controlled from Labview. The error detection can detect if one or more (control or test) pulses are missing or if none of the pulses are received, as control pulses show up periodically. If the control pulse is missing, it is due to an error occurred in the pulse generator circuit. In case no pulses are received for

a longer period, permanent damage of the circuit is probable.

5.2 G-Link Test Signals

The G-LINK serialiser (HDMP-1022) sends serial data to the optical media interface. At the receiving side the simplex G-LINK LDC is used. The FPGA of this card includes an automatic data checker, which checks the data pattern, parity and packet length of the received packets. If an error occurs, an error code is generated and the erroneous data with the error code will be written into a log file on the host computer (PC, Linux).

6. RADIATION TEST RESULTS

On the first two weeks of the irradiation period the card was powered from the power supply of a VME Crate. A power MOSFET transistor was found to be extremely sensitive to radiation in the VME's power supply and three power supply units have died in a very short period, after a few Grays of radiation. The power supply was changed to an external one, which is placed to an area where the dose rate is relatively low.

The total accumulated dose between during the first two months was ~20Krad. The card stopped functioning after 9 weeks of operation. The problem was the degradation of the LM117H Linear Regulator chip which generates 3.3V supply voltage for the Actel chip from 5V. Its output voltage has dropped to 25% of its value measured before irradiation. The chip was replaced 3 weeks later.

The upset rate was in correlation with the dose rate (gamma). As on-line neutron fluence detection was not available we could not make a direct relation between radiation intensity and error rate. The error rate in the first month of irradiation was 2-15 bit flips and 1-4 synchronisation errors per day.

No errors were observed on the A54SX16 FPGA

7. CONCLUSIONS

We did not observe single event errors on the A54SX16 FPGA. Tests at NASA [7] show that this chip does not latch-up and its supply current is not increasing significantly until more than 50Krads. This makes this chip suitable for use in low dose rate environment. We are planning to test this chip in heavy ion radiation in order to investigate the effectiveness of the used SEU mitigation methods.

The LM117H voltage regulator chip proved to be rather sensitive to radiation. We are planning to test the HS-117RH radiation hardened voltage regulator.

It is necessary to find a radiation tolerant serialiser which does not loose synchronisation in radiation since it can take up to 600 microseconds while the link regains synchronisation and 48 Kbytes of data is lost during this time.

It would be essential to establish a reference radiation environment where neutron energy spectra is known and similar to that of the future LHC application in order to estimate the error rate in the real application.

Future investigations are necessary to prove the radiation tolerance of the laser transceiver.

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