RELATIVE ROBUSTNESS AGAINST PROCESS FLUCTUATIONS OF BASIC BUILDING BLOCKS FOR ANALOG FRONT-END OF PARTICLE DETECTORS

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Abstract

The large number of channels (15.7 millions), needed for the silicon pixel detector under development for the ALICE ITS, requires a careful study of the statistical fluctuations of the front-end electronics performance.

By means of classical techniques, such as the Principal Component Analysis, and of new ones used to perform a "realistic" worst case analysis, various configurations of basic CMOS amplifier stages have been compared to evaluate the relative robustness of their performance against manufacturing fluctuations.

To validate the simulated results on a significant statistical sample, a test pattern containing these basic building blocks has been designed and implemented in a 0.35μm process. In this work we present the theoretical results, achieved by applying the proposed Worst Case Analysis technique. The characterisation of the test chip prototypes is currently in progress.

1. INTRODUCTION

In the Alice Inner Tracking System (ITS) a very large number of pixel channels is required to ensure the needed resolution. As a consequence, a high degree of uniformity between pixel front-end cells is mandatory to reduce channel to channel threshold dispersion, optimise time-walk performance at the system level, and guarantee shaping time accuracy and an acceptable production yield. [1]

The non-uniformity of the performances of the front-end electronics blocks is basically due to technological process variations, such as fluctuations of the oxide thickness and of the charge trapped in the oxide. These process fluctuations induce corresponding variations in the device parameters.

A large amount of preliminary work is needed to perform any statistical analysis of a circuit.

Since the process fluctuations are described in terms of variations in the device parameters, the choice of the device model and of the parameter extraction procedure deeply affects the results of the analysis. We will use the Philips MOS Model 9 [2], which guarantees accurate modelling of transistors manufactured in recent sub-micron technologies, but involves many optimisation steps in the extraction process. These must be performed very carefully in order to obtain optimal extraction repeatability and have a good estimate of the physical parameter statistics [3].

Another issue to be addressed in the statistical characterisation of devices is the choice of the size of the MOSFETs to be measured to characterise the technology. In fact the extracted parameters accuracy often depends on the transistor dimensions [4]. A large number of both PMOS and NMOS devices must then be available in order to achieve statistically significant results, especially when studying the parameter correlation.

Finally a sensitivity study of the circuit performances to the varying model parameters should also be done, in order to choose the most significant parameters for the statistical analysis.

In our work, we focus on worst case analysis of basic building blocks for analogue front-end of particle detectors.

First a review and comparison of classical statistical techniques for worst case analysis is presented in order to assess the required computational effort and the impact of correlation between parameters on the results.

Then we describe a new technique for a "realistic" worst case analysis which preserves correlation between parameters and presents a limited computational complexity [5].

After validating the proposed technique by comparing its results with those provided by an extensive Monte Carlo analysis carried out on a digital inverter, we applied it on a set of basic amplifier stages such as a straight cascode, a folded cascode, and a simple OTA with active load, in order to compare the relative robustness of some of their performances, such as voltage gain and output offset.

Furthermore a test chip containing the whole set of the

considered building blocks has been designed and implemented in a 0.35μm CMOS process, to verify experimentally the results achieved.

2. STATISTICAL TECHNIQUES

2.1 Traditional Monte Carlo analysis

The first step is to consider the traditional Monte Carlo analysis. In this technique, a set of NMOS and PMOS parameters is calculated for each iteration, on the basis of their mean value and standard deviations, by using a unit normal random number generator. A circuit simulation follows. Repeating this procedure a statistically meaningful number of times, the statistical description of the circuit performances is obtained. The variability range of each parameter is fixed to $\pm 3\sigma$ with respect to its mean value.

The major problem connected to this procedure is that correlation between parameters is not taken into account and this causes the performance worst case estimation to be too pessimistic.

Furthermore when only a worst case analysis is required, this technique is too computationally expensive and time-consuming.

2.2 Principal Components Analysis

In order to preserve correlation between device parameters both of the same and of the different channel kind, the well-known Principal Component Analysis has to be carried out. It consists in finding a set of linear equations that express the normalised model parameters as a combination of independent unit normal random numbers (Principal Components) [6,7]:

$$P' = U \Lambda^{0.5} C \qquad (1)$$

where P' is the normalised model parameter vector, C is the principal component vector, while Λ and U are respectively the eigenvalues and the eigenvectors matrices of the parameter correlation matrix.

The variability of each parameter is expressed through the well known statistical model, presented in eq. 2 [6,7]:

$$P = \mu_{process}(P) + \sigma_{inter}(P) R_{inter}(P) \qquad (2)$$

Eq. 2 expresses the inter-die variability of the generic parameter P. The unit normal random number R_{inter} is obtained from equation (1) and preserve correlation between parameters. The principal components can be generated independently by a random number generator, and by using eq. (1) and (2), a set of device parameters can be obtained for each iteration.

Monte Carlo analysis following this scheme (PCA Monte Carlo) yields more realistic results than the traditional Monte Carlo, but is still too complex a way to obtain a worst case estimation.

In fig. 1 a comparison between traditional and PCA Monte Carlo analysis is shown for a CMOS inverter, while table 1 and table 2 reports respectively the average value and the standard deviations used for the parameters and their correlation coefficients. In this case only the threshold voltages and the transconductance parameters for NMOS and PMOS transistors have been considered.

Table 1. Statistical properties of the parameters employed in the Monte Carlo analysis of a CMOS inverter.

Parameter	Mean	St. Dev.
Vtp	-0.789	1.54 E-2
Vtn	0.672	3.40 E-3
βp	392 E-6	4.18 E-7
βn	567 E-6	1.25 E-6

Table 2. Parameter correlation matrix.

	Vtp	Vtn	βp	βn
Vtp	1	-0.2	0.9	0.3
Vtn	-0.2	1	-0.3	-0.1
βp	0.9	-0.3	1	0.4
βn	0.3	-0.1	0.4	1

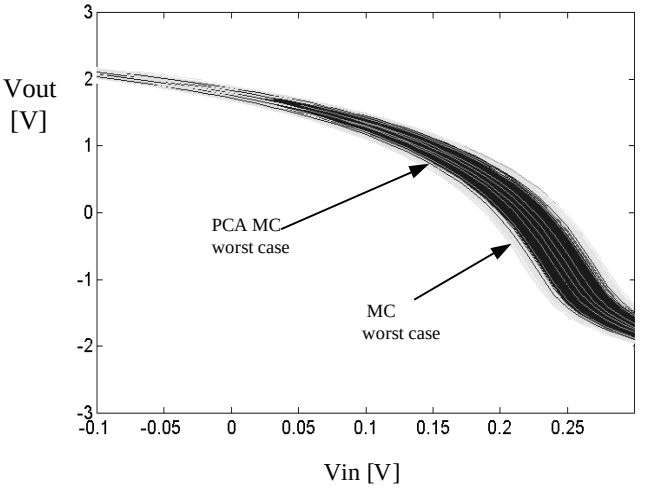

Fig. 1. DC characteristics for a CMOS inverter: traditional Monte Carlo curves (grey lines) and PCA Monte Carlo curves (black lines).

It is clear from fig. 1 that the DC characteristics spread is reduced by the correlation between parameters, and that the traditional Monte Carlo Analysis provides pessimistic and meaningless worst case results.

2.3 Traditional Worst Case Analysis

Accurate worst case analysis can, of course, be performed by an extensive (more than 2000 simulations) Monte Carlo analysis. It is sufficient to calculate, for each circuit performance, its ± 3σ values with respect to its mean value. But for a simple worst case analysis, a complete Monte Carlo simulation is too time-consuming. It would be better to find directly the "corner points" in the parameter space that correspond to the performance worst case values. A very simple way to try to do this is to run circuit simulations with all the device parameters set to their ± 3σ values, including all the possible combinations.

This procedure is based on the assumption that the function that maps the device parameters space to the circuit response space must be approximately monotonic, otherwise it is not possible to find the performance corner points starting from the device parameter ones [8].

"Approximately monotonic" means that the mapping functions can have some ripples, but such ripples must be small respect to the full range of variability [8]. A study of the circuit performance sensitivity to the device parameters can be performed to verify this assumption, and to determine the worst case directions for each parameter [9].

The worst case analysis carried out with this simple procedure leads to very pessimistic estimation of the circuit performance corner points. This happens because correlation between parameters is not taken into account so that the corner points chosen in the device parameter space are not physically meaningful.

3. PROPOSED WORST CASE TECHNIQUE

3.1 PCA Worst Case Analysis

The technique we propose, which we call PCA worst case analysis, preserves correlation between parameters. The starting point is to perform a Principal Component Analysis, in order to relate the vector of the n normalised parameters to the unit normal random vector of principal components. Then one parameter is fixed at its upper or lower bound (± 3σ), and a set of principal components is calculated, which provides the chosen value of the parameter.

For instance, for the parameter P_1 set at its +3σ value, if the correspondent expression in function of the principal components is:

$$P_1 = A_1 C, \qquad (3)$$

where vector A_1 is the first row of the matrix $U\Lambda^{0.5}$.
We can write

$$C = (A_1)^{-1} 3\sigma \qquad (4)$$

The extraction of this vector C is performed by means of a least square method based on the pseudo-inversion of the matrix A_1 [10]: in this way the chosen vector of principal components C has minimum norm. This implies that the extracted vector is also the most likely to occur among the ones which provide $P_1=3\sigma$.

The values of the remaining parameters P_j, $j\neq1$, are then calculated on the basis of the chosen vector of principal components, through equation (1).

3.2 Example: comparison of different analysis methods for a CMOS inverter

In order to test the effectiveness of this technique an extensive PCA Monte Carlo simulation has been carried out for a simple CMOS inverter (2000 iterations). Then a worst case analysis has been implemented with both the traditional technique and the proposed one. Fig.2 and fig.3 represent respectively the input-output DC characteristics Vout – Vin and the supply current characteristics Id – Vin. In table 3 a comparison of the maximum relative dispersions provided by the three methods is reported for some of the main circuit performances, such as the input offset, the inversion voltage, the gain and the noise margins.

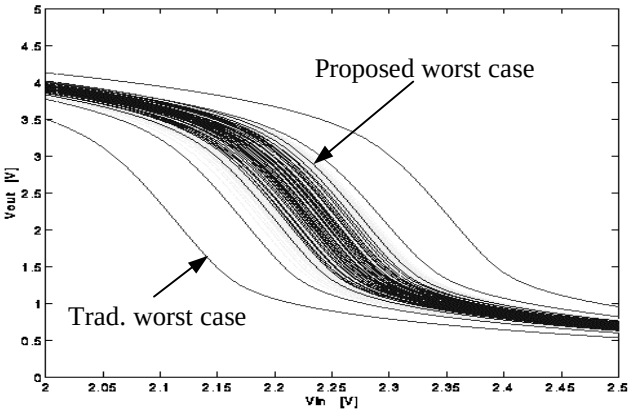

Fig. 2. DC Vout/Vin characteristics for a CMOS inverter

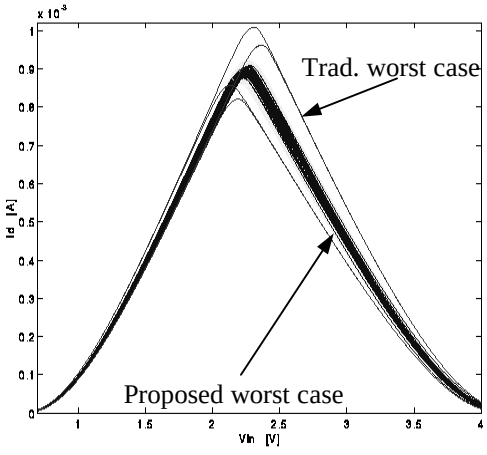

Fig. 3. DC Id/Vin characteristics for a CMOS inverter

Table 3. CMOS inverter: comparison between different analysis methods.

Performance relative variations [%]	PCA Monte Carlo	Proposed Worst Case	Traditional Worst Case
Input offset	4,96	3,60	7,66
Inversion voltage	4,48	3,13	7,61
Gain	5,38	4,03	7,29
High noise margin	9,81	7,93	15,45
Low noise margin	12,23	10,91	20,91

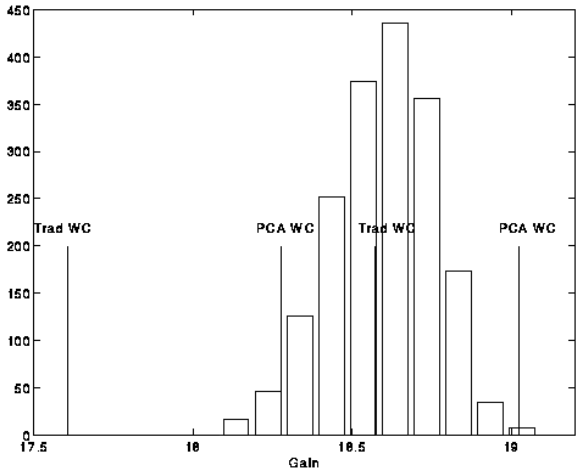

Fig. 4. Gain histogram of a CMOS inverter, obtained with 2000 PCA Monte Carlo simulations. The worst case limits, obtained with the proposed PCA worst case analysis (PCA WC) and with the simple worst case analysis (Trad WC) are also plotted.

In this example the Principal Component Analysis has been performed on a total of 20 parameters (10 for the NMOS and 10 for the PMOS device) and using 20 principal components. The Philips Model 9 parameters considered are: the threshold voltage V_{to}, the gain factor β, the mobility reduction coefficients θ_1, θ_2, θ_3, the body effect parameter k, the sub-threshold region parameters m_o, ζ_1, the output conductance related parameter γ_1, and the channel length modulation characteristic voltage V_p.

Since a traditional Worst Case Analysis with 20 varying parameters can not be performed because of the high number of possible combinations of parameters set to their $\pm 3\sigma$ values (2^{20}), in our analysis the number of parameter combinations has been reduced by means of a preliminary sensitivity study, whose main aim is to show which parameters the circuit performances are most sensitive to.

It is evident from table 3 that the circuit performance spreads evaluated by means of the proposed worst case analysis technique are closer to those obtained by a PCA Monte Carlo than the ones calculated with a traditional worst case analysis.

In fig. 4, a gain histogram obtained with the PCA Monte Carlo simulations is presented, together with the worst case limits obtained with both the traditional worst case technique and the proposed one. The performance limits provided by the PCA worst case analysis are estimated to be about a factor 2.5 the standard deviations foreseen by the PCA Monte Carlo, whereas the results of the traditional worst case technique are evidently unrealistic. Thus the estimation of the worst case circuit performances obtained from the proposed technique is just a little less conservative than the one provided by PCA Monte Carlo. This is caused by the use of the minimum norm vector of principal components which results from the above mentioned pseudo-inversion of the matrix $U\Lambda^{0.5}$ rows. In fact more vectors of principal components may exist which give the same $\pm 3\sigma$ value of the current parameter and have not negligible probability of occurrence, even though their norm is non-minimum. These vectors are neglected in our worst case analysis.

4. COMPARATIVE WORST CASE STUDY OF ANALOGUEBUILDING BLOCKS

After validating the proposed worst case technique on a CMOS inverter, we applied it to compare the performances of three basic amplifier stages: a straight cascode, a folded cascode, and an OTA with active load. All the circuits share the same nominal gain value.

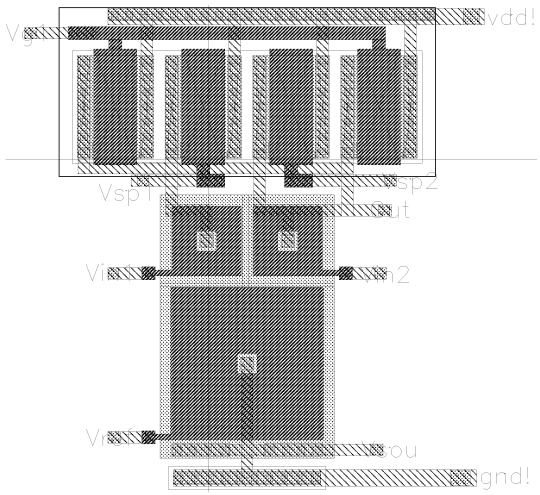

Fig. 5. Layout of the OTA stage, showing the NMOS transistors with enclosed structure.

Simulations on these basic analogue stages have been carried out considering the corner points in the device

parameter space found by means of the PCA worst case analysis, as described in the previous section.

Three performances have been chosen to compare these circuits: the output offset, the voltage gain and the bandwidth. In table 4 the simulation results have been reported.

The OTA with active load exhibits the best results for all the considered performances. This is due to the existence of an intrinsic feedback and to the balanced structure of the circuit. The current mirror used as active load tends to make equal the currents in the two branches of the circuit and improves the robustness of the stage against the inter-die parametric variations. The folded cascode shows better behaviour compared to the straight version of the circuit. This can be explained considering that in the folded structure the main performances of the circuit depend on parameters of MOSFETs of the same kind (NMOS or PMOS), whereas in the straight structure the same performances exhibit dependence on parameters of both NMOS and PMOS devices.

Table 4. Comparison of the performance relative variations for three basic amplifier stages.

Performance relative variations [%]	Straight Cascode	Folded Cascode	OTA
Output offset	54,01	47,71	32,31
Voltage gain	6,95	2,29	0,29
$\mathbf{f_{-3db}}$	34,20	11,15	5,63

It must be pointed out that in all the simulations of both versions of the cascode, the reference voltages have been implemented by means of simple CMOS biasing structures instead of ideal voltage sources, since in real circuits this is the most used solution. If the references were realised with independent voltage sources, the results reported in table 4 would be quite different.

5. CONCLUSIONS

A novel technique for a realistic worst case analysis of analogue building blocks has been presented. The proposed method preserves parameter correlation without requiring excessive computational effort. This makes it suitable to perform the statistical analysis of large circuits instead of a time-consuming Monte Carlo simulation carried out together with the Principal Components Analysis.

The technique has been applied to a set of basic CMOS building blocks, such as the straight cascode, the folded cascode, and the OTA with active load, to assess their relative robustness against the process induced parameter fluctuations. The results obtained are referred to a set of performances usually relevant in the design of front-end circuits. The relative degree of robustness of the examined stages is likely to hold even for different statistical input data, while this is not guaranteed if a different choice of the considered performances is made (noise, linearity, etc.). Therefore it is up to the designer the proper choice of the specs to be considered depending on the particular application. Here we intended to propose a technique to make viable the evaluation of the performance spread for circuits of relatively high complexity, such as those encountered in actual front-end channels.

6. REFERENCES

1. E. Cantatore, M. Campbell, et al., “Statistical analysis and optimization of delay line chains for pixel readout electronics”, Nucl. Instr. and Meth. in Phys. Res. A 395 (1997) pp. 318-323.
2. R.M.D.A. Velghe, D.B.M. Klaassen, F.M. Klaassen, “MOS Model 9”, Philips National Laboratory Unclassified Report NL-UR 003/94.
3. M. Bolt, E. Cantatore, M. Socha, C. Aussems and J. Solo, “Matching Properties of MOS Transistors and Delay Line Chains with Self-Aligned Source/Drain Contacts”, Proceedings of the ICMT’96, Trento – Italy (March 1996).
4. E.V. Saavedra Diaz, K.G. McCarthy, D.B.M. Klaassen and A. Mathewson, “Efficient parameter extraction and statistical analysis for a 0.25 micron low-power CMOS process”, Proceedings of the 27th European Solid-State Device Research Conference (ESSDERC’97), pp. 656-659, Edition Frontiers, 1997.
5. M. Bolt, M. Rocchi, and J. Engel, “Realistic Statistical Worst-Case Simulations of VLSI Circuits”, IEEE Trans. on Semiconductor Manufactoring, vol. 4, n. 3, August 1991, pp. 193-198.
6. C. Michael, M. Ismail, “Statistical modeling for computer–aided design of MOS VLSI circuits”, Kluwer Academic Publishers Boston/Dordrecht/ London.
7. C. Michael, M. Ismail, “Statistical modeling of device mismatch for analogueMOS integrated circuits”, IEEE Journal of Solid State Circuits, vol. SC-27, February 1992, pp. 154-166.
8. D. Stoneking, “Improving the manufacturability of electronic designs”, IEEE Spectrum, June 1999, pp. 70-76.
9. S. R. Nassif, A. J. Strojwas, and S. W. Director, “A Methodology for Worst-Case Analysis of Integrated Circuits”, IEEE Trans. on Computer-Aided Design, vol. cad-5, n. 1, January 1986, pp. 104-112.
10. D. Bini, M. Capovani, O. Menchi, “Metodi numerici per l’algebra lineare”, Zanichelli Bologna, 1988, pp. 456-462.