ANALOG SIGNAL SPLITTER

E.Atkin, Yu.Mishin, Yu.Volkov, Moscow Engineering Physics Institute, Russia
e-mail: atkin@eldep.mephi.ru

Abstract

The high-speed (wide-band) splitter circuit for reading out photomultiplier analog signals is described. The splitter can simultaneously drive loads of the type of CFD, LED, ADC, QDC, TDC and so on.

The photo of the manufactured prototype printed circuit unit (PCU), based on microwave transistors and fitted with LEMO connectors, is presented. The dimensions of the 4-channel PCU are 75*50 mm.sq. The splitter provides a high slew-rate of about 2000 V/us, large dynamic range up to 60 dB and low power consumption 250 mW.

1. INTRODUCTION

A number of LHC experiments (for instance, ones with time-of-flight detectors) require high-speed (wide-band) splitters of photomultiplier analog signals. The splitters should have a high slew-rate (up to 2000 V/us), large dynamic range (up to 60 dB) and low power consumption (tens of mW). The main destination of the splitters is to provide simultaneous parallel signal processing by amplitude, charge, time and so on. The splitter can drive loads of the types of CFD, LED, ADC, QDC, TDC and so on.

2. STRUCTURE AND SCHEMATICS

The most acceptable circuital solution in the case of both polarity pulses is the use of push-pull AB stages with complementary microwave bipolar transistors.

The elaborated splitter circuit contains an input section (core) and output buffer stages, as shown in Figure 1.

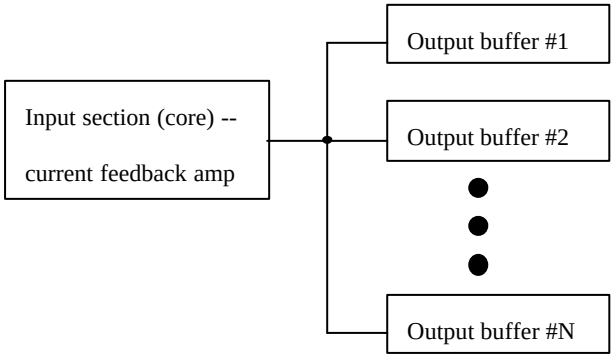

Figure 1. Structure of the splitter

The core is built according to the current feedback schematics. It is responsible for bandwidth, static parameters (input offset voltage and input currents). The latter set a limit to the dynamic range. Taking into account disturbances, cross-talks and the standard offset voltage for a pair of bipolar transistors to be ~1..2 mV, one should assume minimal input signals of ~5..10 mV. Therefore in order to provide 60 dB of dynamic range there must be ensured a maximal output amplitude not less than 5V.

Moreover the core provides the limitation of the output voltage swing by a value of about 6V, thereby protecting the output stages from burnout. This is provided by applying a nonlinear local feedback to the core.

The output buffer stages (compound voltage followers) provide driving low-ohmic loads (as typical – 50 Ohms each). The value of fan-out (number of output stages operating in parallel), can vary from 1 to 6 depending on the total load.

Simplified schematics of a single splitter channel is shown in Figure 2.

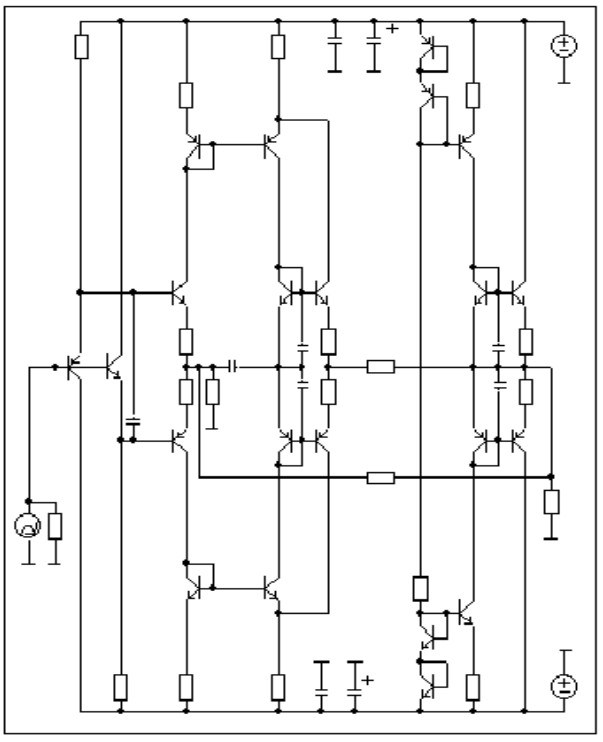

Figure 2. Simplified schematics of the splitter channel

3. IMPLEMENTATION AND LAB TESTS

3.1 Prototype Unit

The views of the manufactured prototype printed circuit unit (PCU), based on microwave transistors and fitted with LEMO connectors, are shown in Figure 3. The dimensions of the PCU are 75*50 mm.sq.

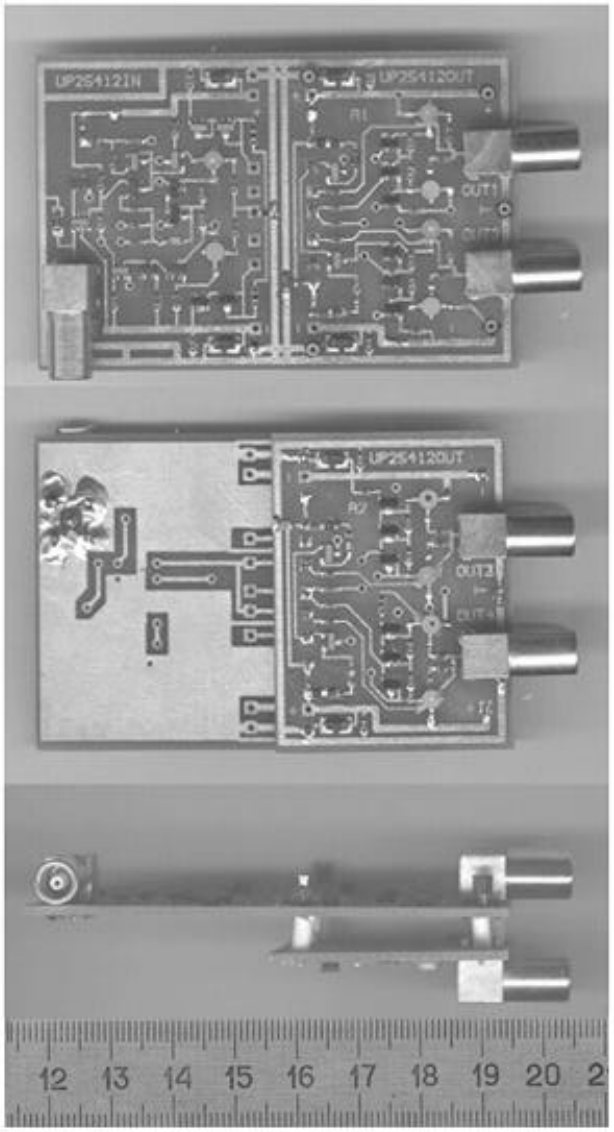

Figure 3. Views of the prototype splitter unit

The circuit indeed has determined the structure of the PCU as a multiboard one. The output sections thereat have been designed mechanically in the manner of a bookstand and connected by their input terminals as a wired-OR. This allows to extend simply the fan-out.

Two versions of boards have been elaborated:

- based on transistors, packed in SOT-23. Both transistor types (npn- KT3130 and pnp- KT3129 ones) have f_t somewhat above 300 MHz;
- based on caseless matched transistor pairs, having f_t exceeding 1 GHz for the npn-transistors KTC398 and exceeding 500 MHz for pnp- ones KTC393.

In the capacity of output transistors in both cases there have been used more powerful npn- transistors of the type KT642 (f_t~5 GHz at I_{max}=120 mA) and pn - ones of the type KT658 (f_t~3 GHz at I_{max}=100 mA).

3.2 Lab Test Results

The prototype PCU provides operation at a unity gain and a fan-out of 4 at load resistances of 50 Ohm each. The maximal output amplitude thereat makes up at least 5V. Rise/fall times are within 2.5 ns. Signal polarity can be any. The maximum rate is not less than 200 kHz. Offset voltage for each output does not exceed $\pm$3 mV. This is achieved at the expense of including trimmer potentiometers in the circuit at the stage of adjustment.

At supply voltages of $\pm$10V power consumption is 250 mW/channel.

Considering the high speed and bandwidth (above 100 MHz), along with circuital matters much attention should be paid to mechanical design implementation. Therefore circuit simulation and PCB routing were done taking into account the influence of the reactances of PCB conductors and pads on the electric parameters.

3.3 Outlooks for IC designing

At present the task of miniaturizing the splitter is being solved. It is expected to implement the tested circuitry in the form of a semicustom IC. It is planned to supplement the circuit with a gain control for separate splitter outputs and an electronic adjustment of DC output potentials, aimed at setting them as close to zero as possible.

4. ACKNOWLEDGEMENTS

We acknowledge the helpful discussions with Uli Thoering from Uni. Giessen and Romain Holzmann from GSI (Darmstadt), who gave the start of the splitter development.

Also we thank our colleagues from SRIPT (Moscow) for manufacture of the prototype boards.

The work is supported by the International Science and Technology Center (ISTC).