Scalable Test Solutions: A Means of Improving ASIC Performance and Time-to-Market in Mixed-Signal Engineering Test

Birger Schneider
microLEX Systems A/S
Dr. Neergaards Vej 5c
DK-2970 Hoersholm
Denmark

Tel.: +45-45 76 21 00
Fax: +45-45 76 22 00
*bsc@microlexsys.*com
www.microlexsys.com

Abstract

In a quest for shorter time-to-market and higher test quality of complex mixed-signal ICs, a novel approach for Mixed-Signal Engineering Test and Low Volume Production Test is devised. The approach builds upon making available to designers a scalable approach for engineering test of mixed-signal ASICs where the low cost entry starts at using standard off-the-shelves low-cost PC-plugin instrumentation and scales upwards to VXI based instrumentation, when performance demands increase in terms of test instrumentation fidelity and/or volume throughput requirements. The high end of the solution approach meets the demands of medium size production volume.

For the entire scalable range of test solutions there is a high level of portability to ensure that an optimum of test program efforts spent at one level can be ported to the next higher level at a minimum cost.

The software environment seen from the user's point of view offers the same look-and-feel for the scalable solutions, and a high level of generic instrumentation secures portability. The software tools available with the approach offer ease-of-use and fast test generation even for complex tasks. Furthermore, the tools lend themselves well for use by designers to promote a natural extension of ASIC design verification. Examples are given on the use of mixed-signal simulation results as the basis for test generation, and a comparison is shown for A/D converter performance based upon SPICE level simulation, VHDL-A level simulation and actual performance of a device under test.

1 Introduction

Mixed-signal ICs, and particularly the analog sub-circuits of such ICs, have become challenging bottlenecks in testing of many of today's high growth application domains such as mobile phones, telecommunications, automotive, datacoms, etc. Faced with demands for shorter design and manufacturing cycles, higher quality and an ever-increasing chip complexity and functionality, existing methods for mixed-signal engineering test have proven insufficient and cumbersome for most design and test engineers.

Over the last two decades many efforts have been employed to improve the general situation of time-to-market in the design and test domains. The world has seen several advances during this period, not least in the field of complex digital chip design. However, the progress in the analog design methodologies have progressed at a much lower degree..

The eightieths were the decade where test problems were solved as an afterthought by involving massive test engineering to compensate for chip designers' lack of knowledge in how to handle the test and quality issues of a given chip function. The design process itself typically was handled in a sequential manner where hardware design basically had to be completed before software design started, and then eventually test engineering started.

In the industry, a general consensus existed since the beginning of the ninetieth that the existing approaches of isolated hardware and software design paths were less than optimal. To bridge this, new approaches in digital design engineering like hardware-software co-design/co-verification, design reuse have emerged over the decade.

This has made it possible for the design community to meet the rapid escalating complexity of chips and still keep design resource employment almost constant or even reducing the total design time.

However, the mixed-signal EDA domain has not seen a similar development as that of the digital domain. Neither has the area of mixed-signal testing. Prototype validation and test in general of mixed-signal ICs are still to a large degree left as activities to be handled by test engineers as rather isolated approaches after completion of the chip design. Customers report that as much as 25-35% of the time and cost for getting an integrated circuit to the market is test related, with test of design and debugging taking a substantial share of this. Some advanced users estimate that verification and simulation problems take an even larger share. In general, the relative balance in designing a state-of-the-art mixed-signal ASIC is changing towards more verification/validation while the design process itself occupies a declining part of the entire cost of obtaining a mixed-signal ASIC.

Simulation of the functional performance plays an important role during a design of a mixed-signal ASIC. However, the simulation process remains a major challenge, and mixed-signal simulation is lagging the performance of digital counterparts. Many simulators for mixed-signal design are still based upon transistor level analog descriptions, e.g. SPICE based simulators that cannot handle more complex circuitry. For this reason, simulators are often applied to isolated problems only, where an analog simulator is employed to a limited domain of the circuitry in an “island-solution” approach, while a digital simulator is used for other domains of the design. However, such isolated approaches suffer from general applicability, and many problems remain in the interfaces between domains that are not covered by the simulators, hence left to show up in first silicon. Assembling the results of simulations typically prove a substantial problem. Add to this that analog simulations normally take a significant amount of time. Mixed-signal simulators are available, but normally only for limited functionality. Recently, new behaviour level simulators have started to emerge, and simulators such as HDL-A (Mentor Graphics), AHDL (Analogy) or VHDL-AMS promise well for the application of mixed-signal simulation to larger functional elements. While HDL-A suffer from lack of hierarchy, the most recent developments like VHDL-AMS seem to offer an improved performance, also for use in conjunction with mixed-signal test generation.

Simulation results are of growing importance for use as test stimuli in mixed-signal testing. Due to the increasing complexity of mixed-signal blocks, it is getting more and more cumbersome to generate functional tests using a black-box concept. To obtain an efficient test generation in a minimum of time, a mixed-signal test ought to be based upon a maximum knowledge of the ASIC block functionality itself. This means that the designer must take a lead role in the prototype evaluation process, utilising the knowledge available for the design already at the design level. Mixed-signal modelling based upon functional simulators like PowerMill ACE (Cadence), or the previously mentioned behavioural level simulators seem to promise a way forward. Such techniques are still in their infancy, but results from European R&D projects under the ESPRIT programme such as ESPRIT 24.268 “TACTIC” [Ref. 1], ESPRIT 26.877 “OPTIMISTIC” [Ref. 2], and ESPRIT 27.943 “SUPREME” [Ref. 3] have shown encouraging results in using such approaches. Later on in this paper, we will address some of the results obtained in these projects.

2 Technological Challenges

A highly real problem to anyone who plans a test strategy, let that be in digital testing, in analog testing or in mixed-signal testing, is what tomorrow's ASICs will bring of performance. Obviously, no one can answer such questions, but guidance can be found from several sources. One important source is “The National Technology Roadmap for Semiconductors” made by the US Semiconductor Industry Association (SIA). Key participants in this exercise are the Semiconductor Research Corporation (SRC) and SEMATEC. This roadmap, the most recent one is from 1997, estimates the trend in semiconductors up to 15 years ahead. Usually these roadmaps are rather realistic.

According to the 1997 roadmap, we should by year 2012 expect chips to have up to 100 M transitors/cm^2, the chip feature size will shrink to 50 nm, chips may comprise up to 13 cm^2 of real estate, and the power supply will drop to the vicinity 0,5-0,6 V of supply. ASICS are envisaged to grow also in number of pins from max 1.100 pins in 1997 to about 5.500 pins in 2012. Likewise, the analog performance is expected to grow from 25 GHz in 1997 to 120 GHz.

Although the number of transistors/chip will increase about 58%/year, the design productivity is only seen to grow 21%/year, thus creating a gap of 30%/year, which may prove critical.

A major element in future design will be increasingly adaptation of a reuse of designs made by others. System-on-a-chip will require employing large, pre-designed blocks, often made by third parties. Chips will predominantly be designed by teams. The EDA tool makers (electronic design automation) are making major efforts in providing tools that allow analysis already before silicon exists, but in mixed-signal the tools are lagging those of the digital domain, and mixed-signal designs keep demanding substantial human interaction.

The materials used on chip are gradually changing, and mixed-material structures will be more dominant. New dielectrics will be applied, and recent advances in copper metal layers combined with aluminium will se a more widespread use.

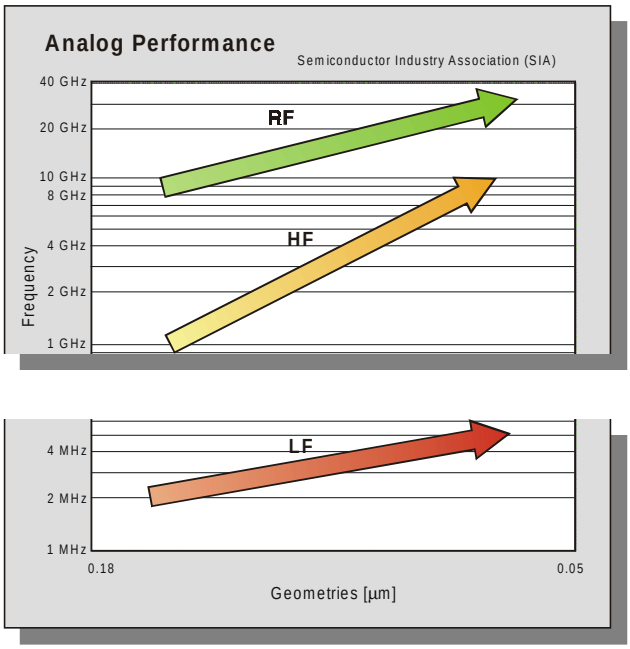


Fig. 1: The performance of CMOS analog is closing in on bipolar performance up to year 2012.

Interconnect delays on a chip are beginning to approach the delays of gates, hence requiring a change in the modelling strategy. In very deep sub-micron, the modelling of interconnect delays and capacitive coupling is insufficient using present days static wireload modelling, and even digital is becoming analog at the frequencies in question.

3 Trends in Design Technology

As stated above, reuse is becoming a time and performance critical parameter for many designs. Verification will become a mixture of verifying internally designed blocks with externally designed blocks. As a result, a major emphasis will be on handling the interfaces between blocks. It is envisaged by several that simulation/verification problems may soon comprise 30-65% of the cost and time for a complex mixed-signal design. We also see a clear trend in the change of the relative balance in design and verification with increasing activity in verification and a relative decrease in the design effort itself.

We envisage that the future designer will rely even more on the existence of capable and accurate simulation models. However, despite these the first-time correlation between theoretical performance and actual silicon will remain rare – especially in mixed-signal.

The process of back-end verification, as we know it today, will change. It will have to start concurrently with chip designs to support finding bugs early, since time-to-market is becoming even more mission critical. For this reason, we believe that it is imperative that the designer takes a lead role in back-end verification and characterisation process (engineering test). In the Ref. 1 and Ref. 2 project activities, such techniques are already successfully being applied to some of today's most advanced ASIC designs in mobile telephony applications.

Although the EDA tools are undergoing many improvements, we envisage that mixed-signal designs will continue to be a major challenge. Also in the next few years to come, we expect 1-2 redesigns on average for a typical mixed-signal application. Today, mixed-signal designs take considerably longer to complete than digital designs, because tools are lagging or are less mature than in the digital domain.

In today's applications we see that simulation tools are mostly applied to isolated domains, digital or analog. This creates a problem just to assemble the various simulation results. We expect that the advent of VHDL-AMS and similar simulation environments will ease the situation somewhat, but several challenges will remain to exist. In current activities, we are involved in the applications of such improved simulation approaches, or rather their application in test generation activities, and the results obtained up to now look encouraging.

4 The Problems of Non-Testable Mixed-signal ASICs

As a consequence of the growing complexity of mixed-signal circuits, testing becomes almost impossible, if the chip designers do not take a lead role in a test generation process. It no longer seems feasible to maintain yesterday's philosophy of test generation, where a test engineer solves all testing issues of an ASIC as an afterthought.

If a test generation is to be achieved in a minimum of time, at a moderate cost, yielding a high test coverage, and at the same time preferably offering high throughput in testing, the mixed-signal test must be planned early in the design process. If not, an ASIC may prove difficult or even impossible to test. The latter can be disastrous to an otherwise good design. Most test engineers have come across such problems, and many have faced situations where a mixed-signal circuit may take minutes to test, which alternatively could have been done in few seconds, if a well planned test strategy had been adopted already in the design process. We typically refer to such

designs as “non-testable”, because the resulting test time is exceedingly high, or in some cases certain characteristics are not possible to verify in a deterministic manner. Costs associated with such testing tend to become prohibitive.

As a result of this definition, test solutions may exist for “non-testable” parts, but the cost of testing can be high, e.g. exceeding the price of the silicon itself or more, and hence is unacceptable to most companies.

5 High Costs of Mixed-Signal-Testing

Another dilemma in mixed-signal testing is the high costs often associated with test equipment and test program generation in this area. Many automatic test equipment production testers (ATEs) like the Teradyne’s, Credence’s, HP’s and others exceed investments of 1 million US $. Such systems have optimised characteristics for high volume testing, and do a good job in that, but may not offer measurement characteristics that exceed what can be obtained using good standard instrumentation like GPIB based rack-&-stack test system solutions or, even better, VXI-based instrumentation.

In mixed-signal engineering testing, the expensive ATE systems, with all their “bells and whistles”, are usually prohibitive for use in engineering testing because of their high costs. As a result, many design engineers end up making their own mixed-signal test set-up, typically a lab instrument set-up, often based upon GPIB instruments or PC-plug-in instruments. However, modern mixed-signal ASICs are typically systems-on-a-chip, and the embedded system testing required is difficult or even impossible to obtain based upon discrete instrument solutions, although such instruments are physically present in a rack-and-stack instrument solution. A system solution requires a good deal more. For example, mixed-signal testing often demands coherent testing [Ref. 4], which is difficult to achieve, unless a system approach is made for this. A number of other requirements are obvious, including a system software environment that supports the system-like testing required in mixed-signal testing. A simple request of being able to perform reproducible tests, for example after a redesign, may be difficult to honour, if the instruments used are disassembled between test events.

Most professional approaches for mixed-signal testing usually end up being relatively complex simply to meet the requirements, since a simple rack-&-stack solution does not suffice. In conclusion, a mixed-signal test, e.g. engineering test performed by designers, may call upon a solution somewhere in-between a high-cost ATE solution and a simple rack-&-stack instrument cluster solution. This simplified picture is obviously often blurred by a number of other facts in a given mixed-signal test situation. A chip may for example offer a number of built-in-self-test features (BIST) and/or good testability approaches that changes the scope of the test strategy. But by and large, most users need professional solutions for mixed-signal testing, and solutions at affordable costs.

6 A Scalable Mixed-Signal Test System Solution

One set of solutions to modern mixed-signal ASIC testing is described in the following.

As a result of European Commission funded projects under the ESPRIT programme, a scalable mixed-signal test system architecture is emerging. The first systems have been installed for engineering test, i.e. two models of test stations, one of which is a line of low cost personal test stations and the other is a line of high performance test stations. These two lines of solutions have proven very efficient and competitive.

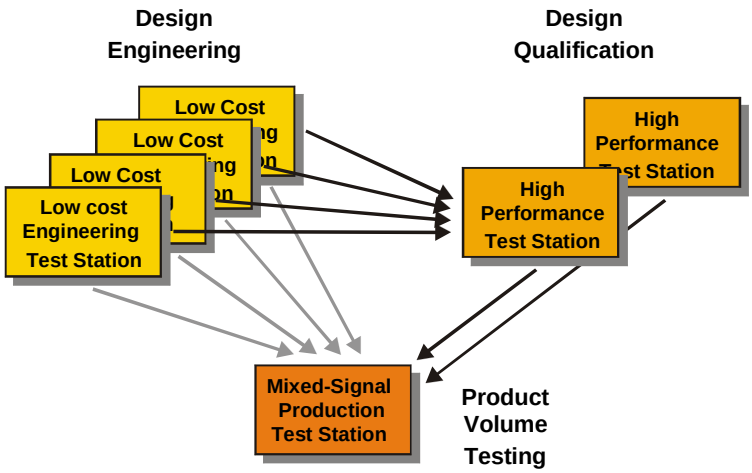


Fig. 2: The 3 lines of mixed-signal test system categories in the scalable solution. The software architecture offers the same look-and-feel at all three levels.

A third line of systems, a medium volume production test system is soon to be marketed as well.

The scalable set of system solutions have been developed with the following in mind:

- Low cost
- Openness in concepts (software and hardware)
- Ease-of-use
- Modularity, preferable standard off-the shelf instrument hardware modules

- Software instrumentation to meet the needs of the user applications
- Efficient test execution
- Minimum test times
- Minimum program development time

Fig. 3: A high performance mixed-signal engineering test station, part of the scalable solutions.

In addition, the system concept allows easy transfer of test results between a mixed-signal design environment and the engineering test station or production test station. The transfer allows bi-directional transfer of test results from the design environment to the mixed-signal test environment as well as it allows transfer of modified test results back to the design environment.

An important feature of the scalable solution is the relatively high compatibility of test programs between the engineering test environments and the production environment, supporting easy transfer of results and test programs, shorter time-to-market, and not least allowing the mixed-signal design engineer to take responsibility for the test itself. Bridging of design and test is a major prerequisite for future mixed-signal ASIC designs.

7 System Architecture

To manage optimally the access of designers to mixed-signal testing as well as offering a volume test capability for mixed-signal, once the ASICs go into production, a range of solutions are available in the scalable range of mixed-signal test stations.

The scalable test system architecture builds upon a three-tiered architecture having the following distinct types of test hardware platforms:

- The Personal Mixed-Signal Engineering Test Station, the *ALPHA* Test Station.
- The High Performance Mixed-Signal Engineering Test Station, the *BRAVO* Test Station.
- The Mixed-Signal Engineering Production Test Station, the *CHARLIE* Test Station.

The Alpha Test Station is a low cost engineering test solution based upon standard PCI instrument platforms running under WinNT, and having some supporting GPIB-controlled instruments like relays switches and Power supplies. The analog input and output functions are obtained using a MIO module offering 8 differential analog inputs or 16 single ended inputs, and 2 analog outputs. A 16-bit resolution is achieved at sampling rates up to 100 kSa/s or 12 bits to 1,25 MSa/s. Counter functions are available. If for example higher speed analog digitisers are needed, this can be added as well. Digital channels are available as static functional high speed digital I/O channels in steps of 32. The speed is up to 20 Mwords/s in handshaking I/O.

The high Performance Bravo Test station offers similar functionality (and more), and the software has the same look-and-feel as that of the mixed-signal Personal Test Station. Here a variety of analog capabilities are available. Selecting the generic drivers in the system yields portability of application test programs for the low-cost personal test station. Analog test features may offer digitising up to 5 GSa/s at 8 bits, and 18-19 bits in the audio range is featured as well. For analog stimuli, 19-bits of linearity is achievable in the audio range, and up to 500 MSa/s can be achieved at 8-10 bits. Digital test can be offered up to data rates of either 25 MHz or 50 MHz, dynamic digital testing, offering full control over timing edges, trailing as well as leading edges. Positioning of edges to within a few ns is featured. A vector memory depth of 256 k is available at e.g. 96 channels or more in steps of 32 channels, and loop based testing can be obtained without any cycle steel. Switching of signals through high speed switching systems improves the versatility of the system, allowing the user to route signals under software control.

Volume testing is featured using a Charlie mixed-signal production test station. This test station has almost identical characteristics as the high performance Bravo engineering test station. However, in addition a separate test head holds pin electronics and parallel precision measurements features (PMUs) and programmable loads. This allows parallel measurements of DC parameters like leakage measurements and other DC characteristics that typical have to be verified at all pins of a DUT, hence reducing the overall test time significantly. Ironically enough, DC measurements often comprise a substantial part of the total test time for a device under test. To reduce this part of the test time and to avoid that costly functional test resources are idle for long sequences, the system is equipped with 4 source meters for every 32 test channels.

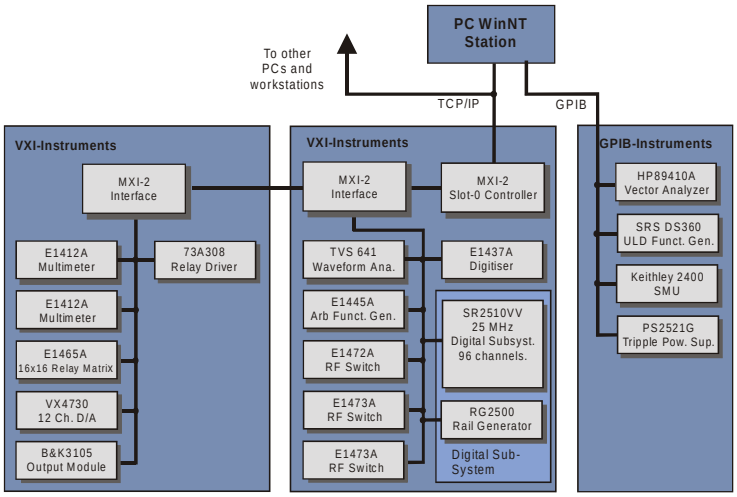


Fig. 4: A typical example of instruments in a high performance Bravo test station. Most instruments are contained in two VXI racks, but some GPIB-bus controlled instruments are employed as well.

The test head of the production test system features easy access to component handlers and wafer probers, and offers a short signal path from test system I/Os like the programmable drivers and receivers to the DUT.

8 Software support for Ease-of-Use

The scalable solutions build upon an optimum system architecture as well as a flexible software, not least very efficient solutions for signal manipulations of mixed-signal and versatile software instrumentation (elaborate software instruments for the given type of test applications). Emphasis has been put on providing the same look-and-feel of the software for the various platforms of testers. Hence, a design engineer, who normally performs mixed-signal testing at his personal test station will be familiar with how to operate the more advanced systems, should he or she have a need to use such systems.

The system software builds upon a proven, advanced, software architecture and its related test tools for test and validation systems. This is tailored to meet the needs of especially mixed-signal applications. Since test optimisation is a major issue, dedicated software instruments constitute an important part of the adaptation. Test programs are generated in the test sequencer environment, SequenTEST. In this environment, the user can easily overview all conditions associated with making a test. Most programming is done using a menu-style fill-in of parameters. If dedicated changes are called upon, this is facilitated through the availability of graphics based programming (LabVIEW). From the test sequencer, basically most other software tools can be

Fig. 5: The production version, Charlie, of the scalable range of test system solutions has separate test head that

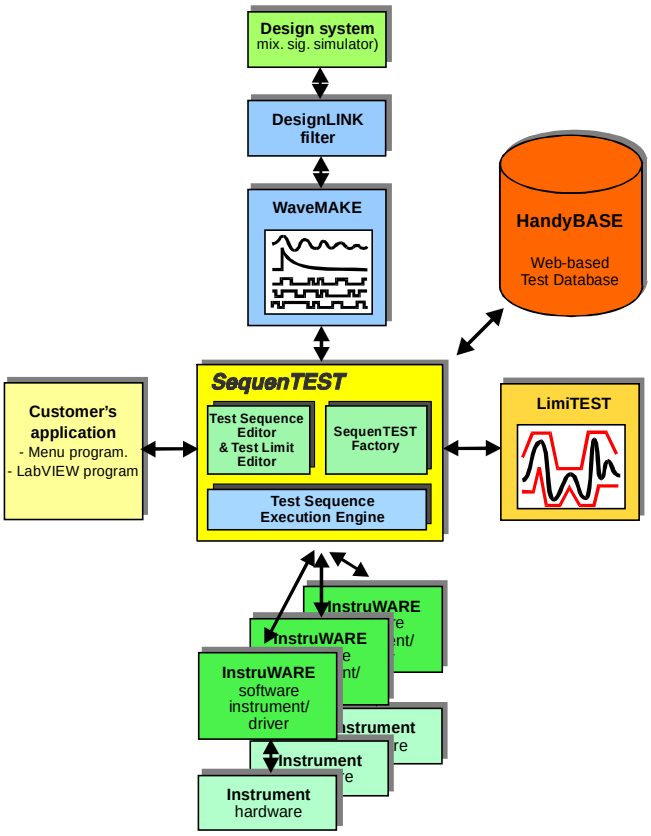


Fig. 7: Software tools of the IntegraTEST scalable test environment consists of test sequencer, limiter functions, waveform editor/viewer, instrument subsystems, test database, etc.

controlled. This applies to limiter functions, Instru-WARE software, the test database HandyBASE, etc. Under the test sequencer, different categories of mixed-signal testing are facilitated like parametric test (analog), vector based test (analog waveforms), boolean (digital test, etc.), and strings.

The LimiTEST software tool makes it possible for a user in an easy manner, and at a minimum of time, to set up even complex types of limiter templates for tunnel based limiters, window limiters, point limiters etc. Limiters for analog signals can be programmed, or imported from e.g. a design environment or learned from a known good device. The LimiTEST subsystem also features test and logging of key parameters. These are user definable and may include finding the peak coordinates of a analog signal (amplitude, frequency), the frequencies at which the curve is 3 dB down, as well as a variety of other key parameters, where basically only human imagination sets a limit. Use of limiter templates is essential in mixed-signal testing.

The test sequencer tool also has features for controlling production test environments like providing control over handlers, wafer probers, and other external equipment as well as facilitating statistical tools for averaging, read out of Cp and Cpk values and many others. A list of the 10 most frequent failure in production testing is continuously updated.

In engineering testing as well as in production testing, large amounts of test data often needs to be manipulated and analysed. To ease this job of the user, a test database, HandyBASE, is available. This is a Web-based data management, analysis, and reporting solution for data acquired during test and characterisation. The test database utilises a MsAccess or SQL Server database for its operation. Through an easy-to-use, internet browser-based interface, the user can get access to the data stored in the database. A variety of analysis tools exists for making this task easier. For the user, a clear advantage is that no special software needs to be installed at the individual user platforms, only at the database server. Hence, the updating of new features is easily handled for even a large group of users. The test database can be accessed over internet, intranets, through modem lines, etc. provided that the user is given access through the security system.

The mixed-signal waveform editor and viewer, WaveMAKE, is a pivot of mixed signal editing and interfacing to design tools. This tool offers a true mixed-signal environment, where all signals, input stimuli as well as output response, can be visualised in one viewing window. Signals may be analog, digital or arbitrary

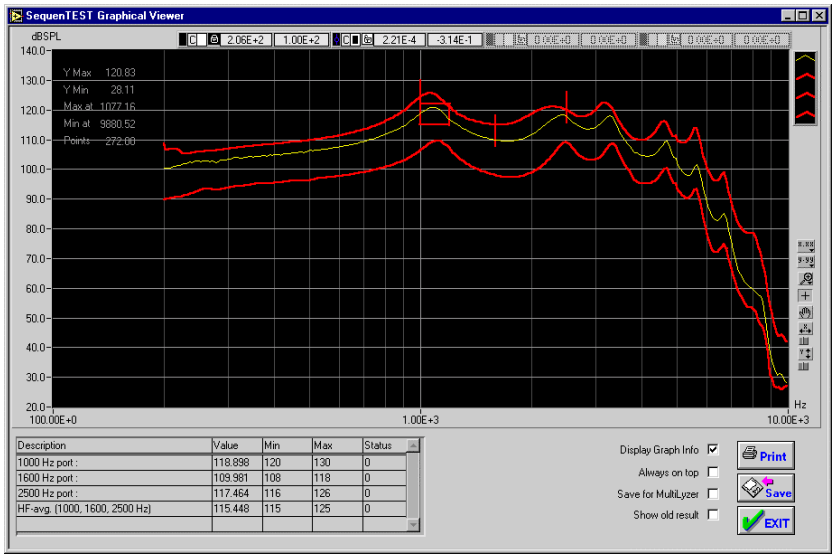


Fig. 6: An example of a tunnel limiter applied to an analog signal. Below the view graph is a table displaying user defines key parameters. All results or subsets thereof can be logged to the test database.

signals including a mix of combinations. Separate editors are available for the analogue signals, the arbitrary signals and the digital signals. They allow for easy and fast creation of signals, using an intuitive programming style. In addition to signal editors, the tool includes analysis functions such as fast fourier analysis (FFT) and signal characterisation features such as rise time measurements. A double cursor system allows for selective FFT of a given signal or may be used for parameter estimation like rise/fall times, signal levels, etc.

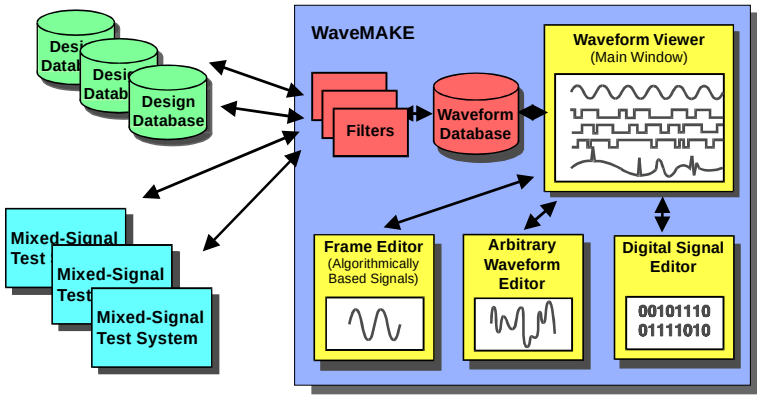
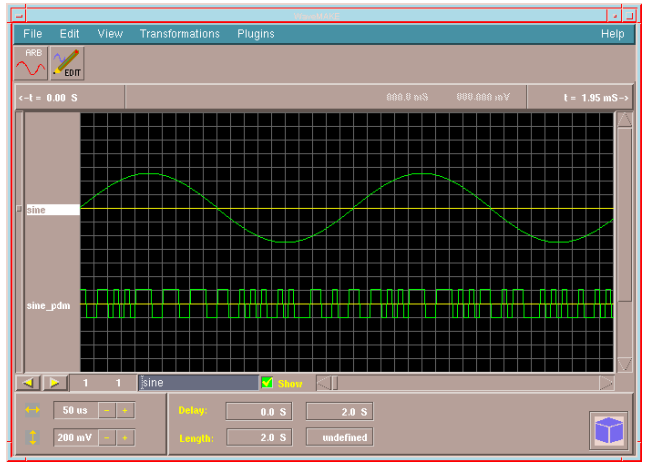


Fig. 8: The WaveMAKE waveform editor and viewer can be used to include all analogue and digital signals in a test. Signals may be transferred from a design database and after integration downloaded to the tester.

The WaveMAKE tool can export/import signals to and from e.g. a mixed-signal simulation environment. In this manner the tool serves as the natural bridge between the design environment and the physical test environment. Using WaveMAKE, simulation results can be downloaded from a simulator to the test hardware for generation of actual electrical signals. Similarly applies to the actual response to be captured from a device under test (DUT). The tool allows large amounts of data to be transferred to be handled, and a number of conversion features allows easy conversions between domains, e.g. analog-to-PDM, PDM-to analog, FFT of digitised waveforms, etc.

From the WaveMAKE tool, waveforms can be downloaded into the actual test hardware, i.e. analog waveform generators, digital test subsystem, etc. Transfer times are of high importance in this process. Below is shown an example of transfer times for digital signals from WaveMAKE to a VXI-based digital test hardware subsystem (Interface Technology SR2500).



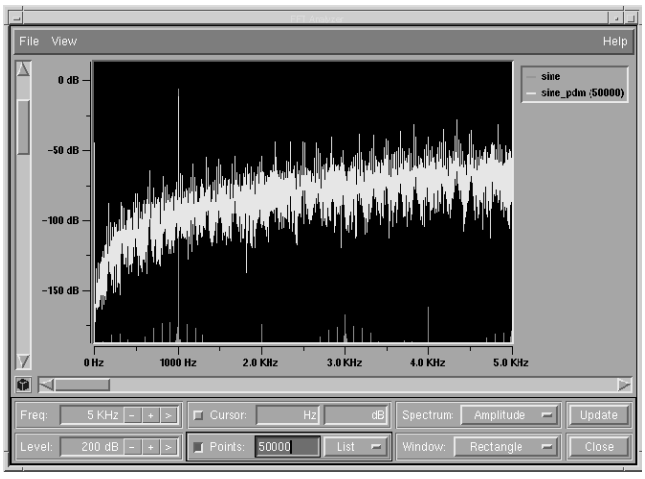


Fig. 9: WaveMAKE easily handles conversions between domains, here analog and digitised PDM signals. The FFT can be invoked on the analog as well as the digitised version of the signal.

Data transferred	Transfer type	Time [sec.]
256k x 1 bit	Export	2,3
256k x 1 bit	Import	5,2
25 waveforms x 256k x 1 bit	Export	57
25 waveforms x 256k x 1 bit	Import	130
65k x 16 bits	Export	7,1
65k x 16 bits	Import	5,8
256k x 16 bits	Local disk	< 2

9 Reuse of Results

A major element in the scalable approach is that is allows a maximum of reuse of results. Basically 4 important elements of reuse have been identified for the solutions.

Reuse of design elements (1) offers a means of providing faster and more efficient generation of tests

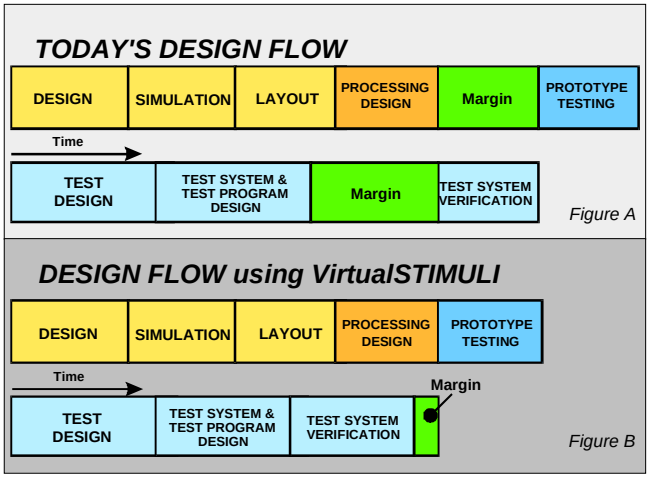


Fig. 10: Today's design flow of mixed-signal can be optimised, if concurrent test generation can take place before actual silicon exists.

results from the bridging of the design tools and the test environment. This is primarily the transfer of signals, analog and digital from the mixed-signal simulation environment.

Reuse of important parts of the engineering test in production testing (2) helps avoid re-doing many software elements again, once an ASIC chip goes into production. Several elements can be reused here. However, one should also note that some elements have to be reprogrammed due to the simple fact that production testing aims at verifying flaws in the ASIC manufacturing process whereas engineering test aims at disclosing design errors. Hence, some testing will by nature be different.

Reuse of vital, well-proven test macros (3) that have been used in previous design/test solutions of similar chip block functionality. This may for example be test macros for given A/D or D/A converters, or other types of digitised analog signals.

Finally, the reuse of major test program elements in an optimal way (4) is essential for several applications. If for example several devices types, almost identical, but having small variations, are to be tested in a production environment, the test sequencer should offer a efficient way of handling diversities.

The scalable solutions support above.

10 Concurrent Test Generation for Mixed-Signal

A general problem in many ASIC engineering test environments is that debugging of the test program cannot really start until first silicon is available. This major problem does not fit with an improved time-to-market strategy.

One strategy to improve on this has been pursued in the TACTIC project [Ref. 1]. Here, simulated electrical response signals from a chip design, that has been finalised but not yet processed, are used in conjunction with arbitrary function generators in a test system. In this way, it is possible to generate some complex electrical signals similar to the ones that the chip will eventually generate, once the first prototypes exist. In this manner, the user generating the actual test program has a means of generating the electrical signals for debugging the test program itself. Using the WaveMAKE environment of the engineering test solutions described earlier on in conjunction with the test hardware itself, it is possible to debug the actual test program before actual silicon exists, See Fig 10.

The approach, we refer to it as VirtualSTIMULI, is convenient for the class of very complex mixed-signal chips that is designed at a leading mobile phone manufacturer. For such chips, only relatively few ports have to be verified for rather complex signal. Using the approach at this company means cutting about 1-2 months off the design time, which is important in a market segment , where the market window of opportunity may only be 6-9 months. The optimisation is shown in Fig. 10.

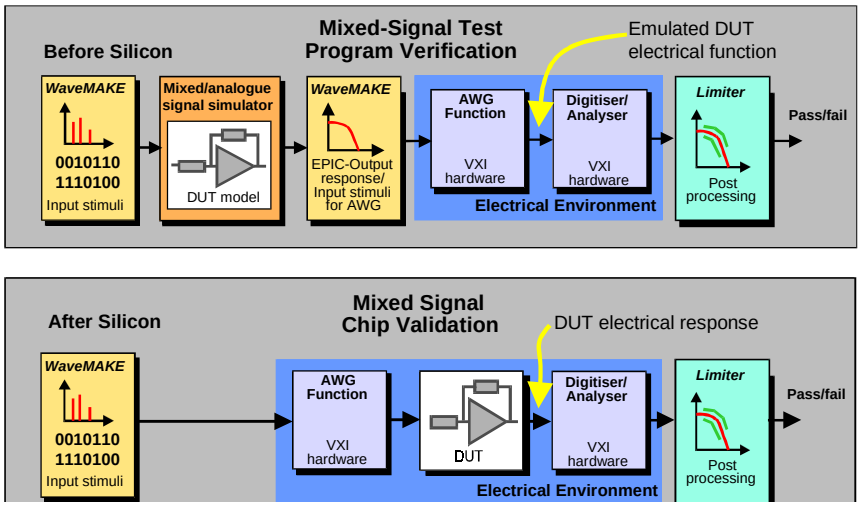


Fig. 11: Illustration of principles in VirtualSTIMULI. In the upper picture, simulated signals are used to generate electrical stimuli for verifying the test setup. In the lower picture, the actual chip is being tested using the hardware modules that were earlier used for test program

11 A Case Study for Concurrent Test Generation in Mixed-Signal

To illustrate some of the achievements obtained using the design links and the general tool environments of the scalable test system approaches described, some examples of signal generation are shown below.

The signal is valid for a 1 kHz sine. Simulations of the signal and its digitised version at the chip level took about 95 hours using a Sun Ultra 450 Processor (4 internal CPUs). This simulates a duration of about 15 ms. If a single CPU processor architecture like the older HP735/200 is employed, the simulation time is about 340 hours.

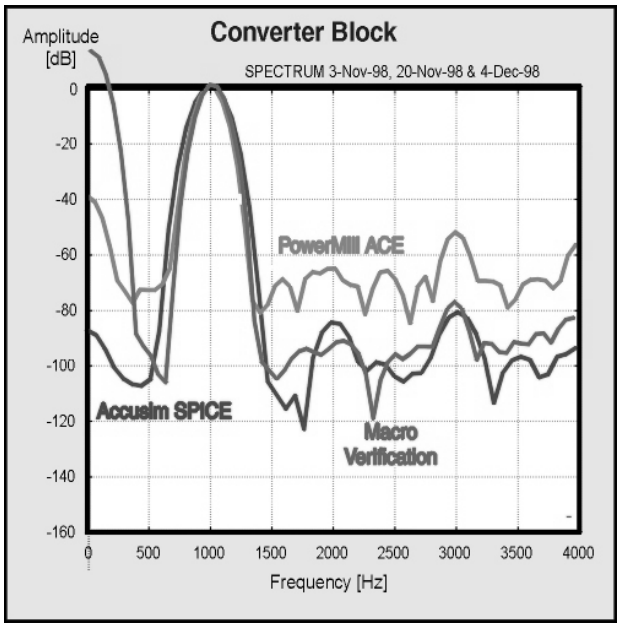


Fig. 12: Verification of simulated results for an advanced mixed-signal macro block (Spice and functional simulation) versus actual macro verification of the silicon.

Three different results were analysed. First a simulation was done for the given converter block using Accusim SPICE. Following that, a functional simulation of the same block was carried out using Cadence PowerMill ACE. Finally the actual silicon was analysed, Macro Verification. As can be seen from Fig. 12, the results are in good harmony with one another at least down to -60 dB, and for the Spice simulation and Macro Verification the results even showed good results to -80 dB. As can be expected, the DC conditions differ. A number of similar results were obtained supporting the importance of the VirtualSTIMULI approach. Ongoing work is in process bringing in also simulation results based upon behavioural level simulation like HDL-A and VHDL-AMS.

12 Conclusions

A scalable engineering test and production test approach for mixed-signal is shown. The set of solutions presented aims at bringing the cost of the testing solutions down and at the same promoting tools that will allow ASIC designers to take a lead in the ASIC test generation process.

A technique for performing concurrent test generation of complex mixed-signal circuits is discussed, and some results are shown.

The general mixed-signal tool environment presented seems to have an appeal to a number of the organisations that participate in the CERN experiments, since it will ease the task of mixed-signal test. At the same time, it provides the users with more powerful tools than normally available for the designers of mixed-signal.

13 Acknowledgement

The author would like to thank Tapio Koivukangs, Esko Kurttila, Veikko Loukusa, Yrjö Mäkelä, Veli-Matti Karpinen, Kalle Lipping, Pekka Rytky, Arto Suopanki and Thomas Burger for valuable and inspiring discussions concerning the test approaches reported for the mixed-signal testing.

We would also like to thank the Commission of the European Union for its contribution to the R&D activities laying the foundations for the system approaches mentioned as well as to several of the tool developments facilitating the scalable mixed-signal approach. This has been funded through projects under the ESPRIT Programme, more specifically ESPRIT 24.268 “TACTIC”, ESPRIT 26.877 “OPTIMISTIC”, and ESPRIT 27.943 “SUPREME”.

14 References

[1] ESPRIT 24.268, TACTIC, "Test Applications Concerted for Telecom Industry Challenges"

[2] ESPRIT 26.877, OPTIMISTIC, “Optimisation Methodologies in Mixed-Signal Testing of ICs”

[3] ESPRIT 27.943, SUPREME, “Solution for Users of Production-Test and Rational Engineering-Test of Mixed-Signal Electronics.

[4] Matthew Mahoney
“DSP-Based Testing”
IEEE Computer Society Press, 1987,
ISBN 0-8186-0785-8

[5] Birger Schneider, Soeren Soegaard,
"IntegraTEST: The New Wave in Mixed-Signal Test". IEEE International Test Conference, 1995