A PROTOTYPE FRONT END CHIP FOR THE CMS RESISTIVE PLATE CHAMBERS

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Abstract

A new front-end amplifier-discriminator-monostable integrated circuit for the CMS Resistive Plate Chambers is presented.
The aim of the circuit is to amplify current signals, ranging from 20 fC to 20 pC and generate output pulses having rise time as fast as possible for timing purposes.
The full custom ASIC was designed and manufactured in the 0.8 μm BiCMOS technology by Austria Mikro Systeme.

1. INTRODUCTION

The Resistive Plate Chambers are gaseous parallel-plate detectors that will be used in the CMS experiment for the *muon trigger system* [1]. In fact they combine good spatial resolution with an excellent time resolution and make the muon trigger capable of identifying muon track, measure its transverse momentum and relate it to the correct bunch crossing.

The RPC proposed for CMS consists of two 2-mm gaps with common pick-up readout strips in the middle and will be operated in the so-called avalanche mode, for sustaining event rates up to 1000 Hz/cm². The shape of the current signal, induced by a single cluster, is described by the function $I(t) = I_0 \exp(t/\tau)$, $0 \le t \le 15$ ns, for freon-based gas mixtures having electron drift speed in the order of 130 μm/ns and τ (gas time constant) ~ 1 ns at the nominal working point of the detector. This can also be considered a good approximation of the real signal, since almost the whole-induced current originates from the first two clusters.

2. DESIGN CONSTRAINTS

In the barrel RPC, the readout strips are 1.3 m long, with a propagation delay ~ 5.5 ns/m while their width ranges between 2 and 4 cm, according to RPC position in the apparatus. The characteristic resistance of the strip ranges from 40 to 15 Ohm respectively, while their capacitance ranges between ~160 pF and ~ 420 pF. The induced signal has a rise time (~ 1ns) shorter than propagation delay of the strip, therefore this one behaves like a transmission line and must be properly terminated at both ends. In fact, reflected signals increase occupancy and, if the termination resistance is larger than the characteristic resistance of the strip, a fraction of input charge is reflected and lost. The strip is terminated on one end by the input resistance of preamplifier, on the other end by a resistor.

Simulations and past experience show that, setting the threshold around 20 fC, the detector is fully efficient. This means that a $\sigma_{noise} < 4$ fC could be tolerated.

3. CIRCUIT DESCRIPTION

The circuit is made of eight identical channels, each one consisting of amplifier, zero-crossing discriminator, monostable and differential line driver. A single channel block diagram is shown in Fig.1. Since the termination resistor has a small and variable value, an AC coupling between strip and amplifier is required.

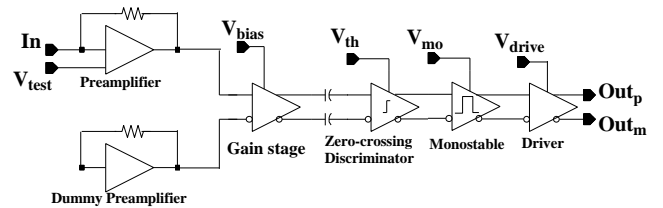The requested power supplies are +5V and GND; the overall power consumption is about 45 mW/channel.

Fig.1. Single channel block diagram

3.1 The Amplifier

The preamplifier (Fig. 2) is a *cascoded common emitter transresistance stage*, with input impedance of 15 Ohm at the signal frequencies (between 100 MHz and 200 MHz), in order to match the characteristic impedance of the strip in the worst case of 4-cm wide strips. In the other cases, the matching will be obtained adding an external series resistor at board level. The current in the input transistor Q_{in} is about 700 μA (for noise reason, as shown in §3.2) and, in order to reduce the supply voltage value [2], a resistor R_{casc} is added between the emitter and the base of the cascode transistor Q_{casc}. The value of R_{casc} is about 4.5

k$\mathbf{W}$ that is much higher than the input impedance of Q_{casc} and only a small fraction of the signal current is lost into R_{casc}. The open loop gain is about 100, while the dominant pole is about 116 MHz and the charge sensitivity is 0.5 mV/fC. A "dummy" input preamplifier was required to balance the DC output variations of the real input first stage.
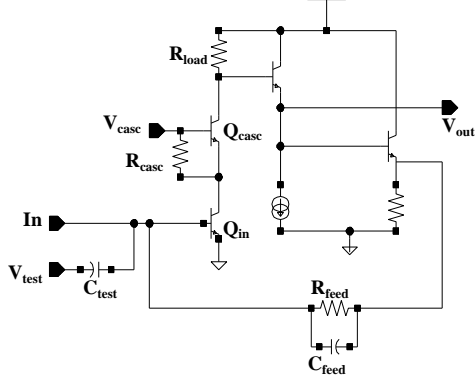

Fig. 2: Current Preamplifier

The expression of the input admittance is:

$$Y_i(s) = sC_{in} + \left(\frac{1}{R_{feed}} + sC_{feed} \right) \left(1 + \frac{g_m R_{load}}{1 + sR_{load}C_{load}} \right) \qquad (1)$$

where C_{in} is the input capacitance of Q_{in}; R_{feed} and C_{feed} are, respectively, the feedback resistance and capacitance; $g_m \sim 27$ mA/V is the transconductance; the parallel of R_{load} and C_{load} is the internal load across which the voltage gain is produced.

If we set $R_{load}C_{load} = R_{feed}C_{feed}$ and define $C_{tot} = C_{in} + C_{feed}$

then $Y_i(s) = sC_{tot} + \dfrac{g_m R_{load}}{R_{feed}}$ $\qquad (2)$

If we impose $R_{in} = \dfrac{R_{feed}}{g_m R_{load}} = 15\Omega$, then

$$Z_i(s) = \frac{R_{in}}{1 + sR_{in}C_{tot}} \qquad (3)$$

Being $C_{tot} < 3$pF, the pole of the above expression is > 1 GHz and

$Z_i \sim R_{in} \sim 15$ Ohm $\qquad (4)$

up to the signal frequencies (between 100 MHz and 200 MHz), as required by the matching condition.
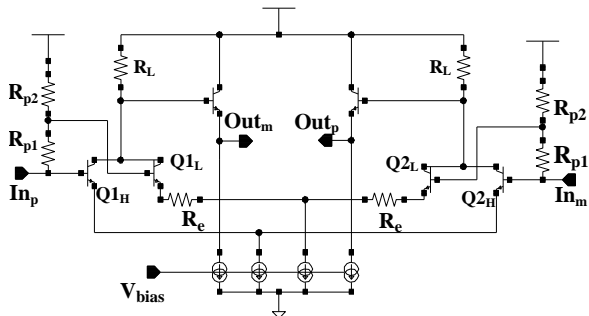

Fig. 3: Gain stage

The preamplifier is DC-coupled to a gain stage, whose schematic is shown in Fig. 3. It is designed to provide

non-saturated response on the dynamic range and to fully exploit the zero-crossing timing, as shown in §3.3. The circuit must ensure a linear behaviour only in the threshold range ($Q_{in} < 100$ fC), while for larger inputs non-linearity is not a problem. A simple way to meet these requirements is to design a two-step piecewise-linear function fitting, which is accomplished by summing the output currents of two gain segments. The preamplifier output is sent to two differential amplifiers having different gains but common output nodes. The external amplifier ($Q1_H$, $Q2_H$, R_L) has a DC voltage gain ~ 7 and is used to amplify small signals ($Q_{in} < 200$ fC) while the internal one ($Q1_L$, $Q2_L$, R_L) has a voltage gain ~ 0.25 and amplifies signals above 200 fC never saturating in the dynamic range. The overall charge sensitivity is 2 mV/fC for input charges < 100 fC and the power consumption of the amplifier, including the "dummy stage", is 15 mW.

The transfer characteristics of the amplifier are shown in Fig.4, while a typical transient response is shown in Fig.5.
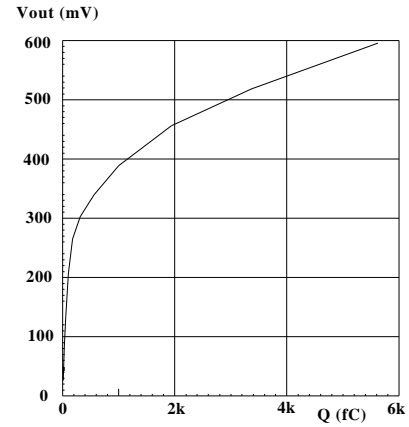

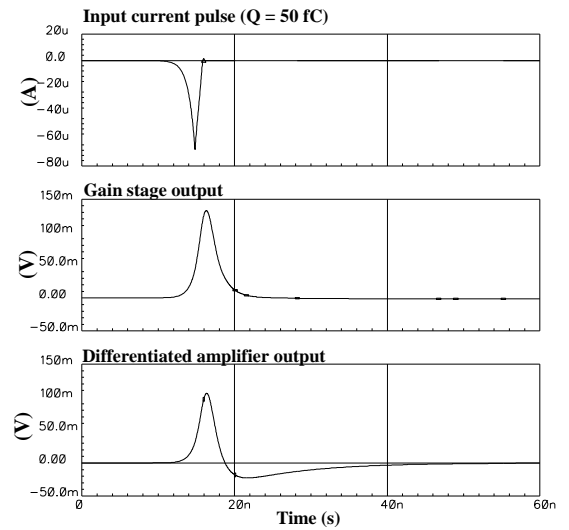Fig. 4: Transfer characteristics of the amplifier

Fig. 5: Typical amplifier output

3.2 Noise calculation

The equivalent circuit of RPC and amplifier for noise analysis is shown in Fig.6 [3].

The parallel noise is dominated by the thermal noise of the terminating resistor R_0 at the far end of the strip and can be represented by an equivalent noise current generator with power density i^2_n (A^2/Hz) in parallel to R_0:

$$i^2_n = 4KT/R_0 \sim 1.1*10^{-21} \ A^2/Hz \ (T = 300 \ K) \quad (5)$$

The series noise is represented by an equivalent noise voltage generator with power density e^2_n (V^2/Hz) in series with the input:

$$e^2_n = 4KT \ (0.5/g_m + R_{BB'}) \sim 4.9*10^{-19} \ V^2/Hz \quad (6)$$

being $R_{BB'} \sim 11$ Ohm the base spread resistance of Q_{in}.
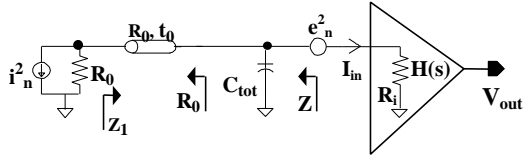

Fig. 6. Equivalent circuit of RPC and amplifier for noise analysis.

The preamplifier is current sensitive, so it is convenient to transform the noise voltage generator into an equivalent current noise generator with power spectrum

$$i^2_{ns} = \frac{e^2_n}{|R_i + Z|^2} \quad (7)$$

where $Z = \dfrac{R_0}{1 + sR_0C_{tot}} \approx R_0$ is the impedance shown in Fig.6, assuming the strip impedance matched at the far end. For simplicity, assuming $R_{in} \sim R_0 = 15$ Ohm, as shown in the expression (4), we obtain:

$$i^2_{ns} = \frac{e^2_n}{4R_0^2} = 5.5 *10^{-22} \ A^2/Hz \quad (8)$$

The rms noise at the output is found by integration of the noise current through R_{in} multiplied by the square of the magnitude of the amplifier transfer function H (jω):

$$V_{ns} = \sqrt{\int_0^\infty i^2_{ns}|H(jw)|^2 \ df} \sim 2.1 \ mV \ rms \quad (9)$$

where $H(s) = \dfrac{V_{out}(s)}{I_{in}(s)} \approx \dfrac{A}{1 + st_L} \quad (10)$

being τ_L the time constant of the dominant pole and A the gain. Assuming the line to be ideal, the impedance seen at the far end is:

$$Z_1(s) = R_0 \frac{Z_i(s) + R_0 \tanh(st_0)}{R_0 + Z_i(s)\tanh(st_0)}, \quad (11)$$

being $t_0 \sim 7$ ns is the propagation delay and Z_i the expression (3). Then, the parallel noise current flowing into the preamplifier is:

$$i^2_{np} = i^2_n \left| \frac{R_0}{R_0 + Z_1} \right|^2 \quad (12)$$

If we assume again $Z_i = R_{in} = R_0$, then $Z_1 = R_0$ and

$$i^2_{np} = \frac{i^2_n}{4} = 2.8*10^{-22} \ A^2/Hz \quad (13)$$

The rms parallel noise at the output is:

$$V_{np} = \sqrt{\int_0^\infty i^2_{np}|H(jw)|^2 \ df} \sim 1.5 \ mV \ rms. \quad (14)$$

Finally, the total output noise is:

$$V_n = \sqrt{V_{ns}^2 + V_{np}^2} \sim 2.6 \ mV \ rms. \quad (15)$$

Simulations of the circuit, including all the noise sources, shows a total output noise $\sim$ 3.4 mV, corresponding to an ENC $\sim$ 1.7 fC, fully satisfying the noise limit of 4 fC.

3.3 Zero-Crossing Discriminator

Accurate timing information from the RPC is crucial for unambiguous assignment of the event to the related bunch crossing. The simplest method to provide trigger pulse is the *leading edge timing*, which can be performed by a threshold discriminator. Though its simplicity, this method is affected by the amplitude time-walk. In the case of RPC signals, with a 1000:1 dynamic range (20fC to 20 pC), the time walk is $\sim$ 10 ns [4].

An amplitude-independent timing response can be approximated by the technique of zero-crossing: a C-R network differentiates the input signal and produces a bipolar pulse crossing the zero in correspondence of the peak of the input signal [5]. In the hypothesis that input signals have the same peaking time, the zero-crossing time is independent of signal amplitude and can be used as time reference. This solution can be easily integrated into ICs. In Fig. 7, the block diagram of the implemented discriminator is shown. The differential outputs of the amplifier are strongly differentiated through a CR network having 4 ns time constant. This grants the fast recovery time of the baseline (< 50 ns) as shown in Fig. 8.
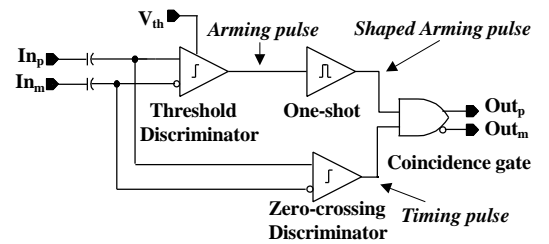

Fig. 7: Discriminator block diagram

The threshold (arming) discriminator provides charge selection capability and consists of a double stage differential amplifier, with a threshold range between 5 fC and 500 fC.
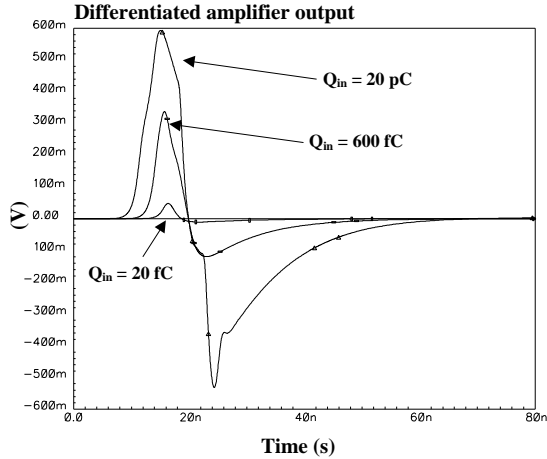
Fig.8 Differentiated amplifier output in the dynamic range.

A one-shot circuit follows the arming discriminator. It shapes the arming pulse typically at 20 ns, in order to ensure its coincidence with the ZCD output.
The zero-crossing discriminator is another double stage differential amplifier, having no threshold. Combining the output of the one-shot and that of the ZCD, we obtain the output of the discriminator, as shown in Fig. 9.
The power consumption of the discriminator is about 8 mW.

3.4 The monostable and the Output Driver

In an RPC working in avalanche mode, an after-pulse often accompanies the avalanche pulse with a delay ranging from 0 to some tens of ns. Therefore, a monostable circuit follows the discriminator and gives a pulse shaped typically at 100 ns, in order to mask the possible second trigger and to prevent the zero-crossing discriminator from triggering on the noise. The choice of the pulse length comes from the trade-off between the possible second trigger and the dead time. Being the expected maximum rate less then 400 kHz/channel, a length of 100 ns, giving a dead time of 4%, has been considered a good compromise. In any case, there is the possibility to tune it in the range 50 ns ÷ 300 ns. The dead time introduced by the monostable is ~ 10 ns and its power consumption is ~ 2 mW.
The Output Differential Driver is capable to feed a twisted pair cable with a signal level of 250 mV on 100 Ω, as required by LVDS receivers. The power consumption is ~ 18 mW but the driver output current can be tuned in order to compensate process variations.
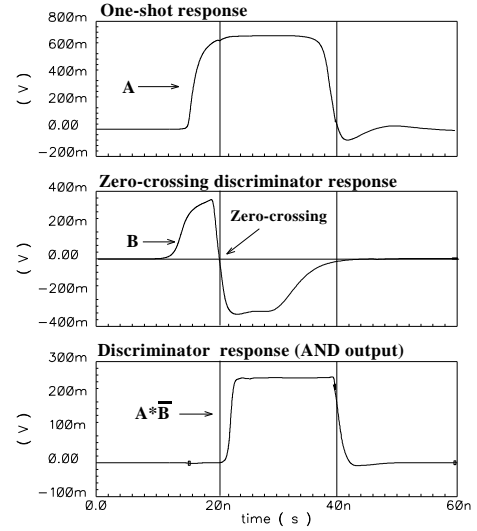
Fig.9 Discriminator principles of operations.

4. TEST RESULTS

14 untested prototypes were received and tested in April 99. They were mounted on a test board housing 2 chips.

4.1 Analog performances

In the first phase, we set the gain of the amplifiers to the nominal value of 2 mV/fC. In the chip, four channels share the same gain control input so we measured the gain uniformity inside each group of four channels. The maximum spread measured was less then ±7%, for input charges < 80 fC. Being the amplifier AC-coupled to the discriminator, this spread represents also a measure of the threshold uniformity and, for our application, it is fully satisfying. For instance, setting the threshold to the nominal value of 20 fC, the maximum expected error is only ±1.5 fC.
The noise was measured using the following technique [6]: an input charge Q_{in} at the frequency f_{in} is sent to the circuit. With the superposition of the noise, the signal amplitude has gaussian distribution; we set two different threshold V_{th1} and V_{th2} in order to have the output signal with frequency $f_{out1} = 0.117 f_{in}$ and $f_{out2} = 0.883 f_{in}$. Then, $V_{th1}-V_{th2} = 2.35\sigma_n = 8.5$ mV, corresponding to an ENC ~ 1.8 fC.

4.2 Timing performances

Timing performances were measured using an oscilloscope HP54542C. The threshold was set to 30 fC and charge pulses ranging between 35 fC and 20 pC were injected by means of a pulse generator LeCroy 9210. For all the prototypes, the maximum input to output propagation delay dispersion among the eight channels was measured as shown in Fig. 10. The maximum ΔT resulted to be 0.9 ns.

Fig. 11 shows the average delay time: for $Q_{in} < 2$ pC, the time walk is less then 1.5 ns. For higher charges (up to 20 pC) it rises up to 2.5 ns.

Fig.10. In-chip delay dispersion.
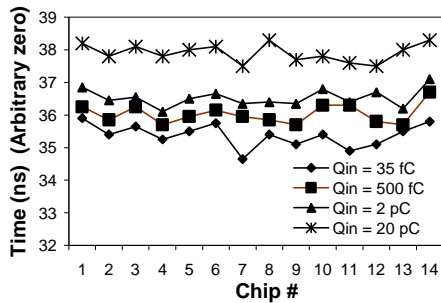
Fig.11. Average delay time.

5. CONCLUSIONS

A BiCMOS front-end chip for the CMS-RPC detectors has been designed and prototyped. Measurements on 14 prototypes agree with the simulation results and fulfil all the design constraints.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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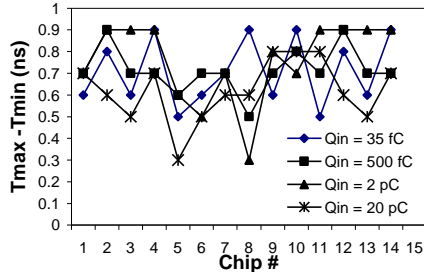[6] P. Jarron et al., "A fast current sensitive preamplifier (MSD2) for the silicon microstrip detector", Nucl. Instr. & Meth. 226 (1984) 156-162.