OVERVIEW OF THE ATLAS LARG ELECTRONICS

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Abstract

This document briefly reviews the main detector characteristics relevant to the read-out electronics of the ATLAS Liquid Argon calorimeters, lists the main requirements and discusses briefly the general architecture and the basic building blocks. The next steps in the construction of the ATLAS electronics are outlined.

1. INTRODUCTION

The Liquid Argon sampling calorimeter technique is used for all electromagnetic calorimetry covering the pseudorapidity interval $|\eta| < 3.2$ and also for hadronic calorimetry from $|\eta| = 1.4$ to the acceptance limit $|\eta| = 4.8$. The global layout is shown in Figure 1. The central cryostat contains the barrel electromagnetic calorimeter (EMB). Each end-cap cryostat houses an electromagnetic calorimeter (EMEC), two hadronic wheels (HEC) and one forward calorimeter (FCAL). Close to ~190 k high precision, high dynamic range and low noise electronic channels are needed to read out this detector

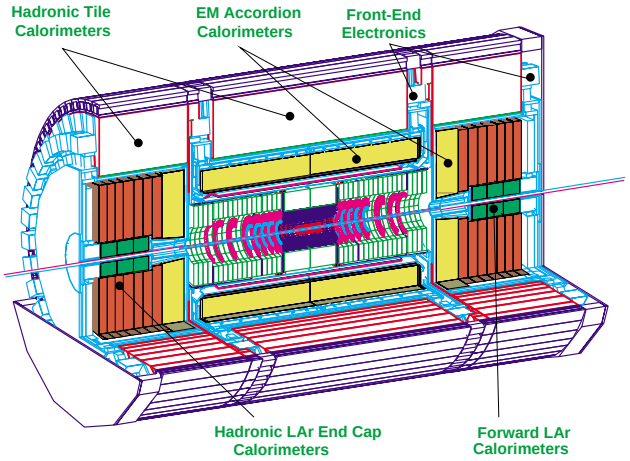

Figure 1: 3D view showing the Liquid Argon calorimeter system and the location of the front-end electronics

Common electronics is used everywhere, with the exception of the very front-end where the HEC uses cold preamplifiers. This minimizes design effort, standardizes hardware and will facilitate maintenance.

A great deal of work has been done to define this electronics system and to prototype it. Samples of nearly every front-end board have been built for a total of about 6000 read-out channels. They are now being installed in the test beam at CERN. This electronics is being used to test and qualify ATLAS calorimeter modules. This provides a very valuable experience with the system.

This note briefly reviews the main detector characteristics relevant to the read-out electronics, lists the main requirements and discusses briefly the general architecture and the basic building blocks. The next steps in the construction of the ATLAS electronics are outlined.

More detailed information can be found in [1, 2].

2. DETECTOR CHARACTERISTICS

The calorimeters are finely segmented both longitudinally and transversally for a total of ~190 k active read-out channels. These channels are grouped consistently to form ~ 5120 trigger towers (see figure 2).

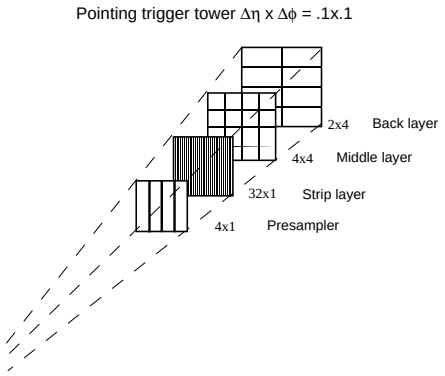

Figure 2: Typically 60 cells are summed to form pointing trigger towers with a size $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$.

As sketched on Figure 3 the detectors deliver on their electrodes a triangular-shaped current signal with a fast rise time (a few ns) decreasing to zero at the end of the drift time of ionization electrons in liquid argon (~ 450 ns). For the FCAL, since the argon gap is smaller, the pulse duration is shorter (~ 50 ns).

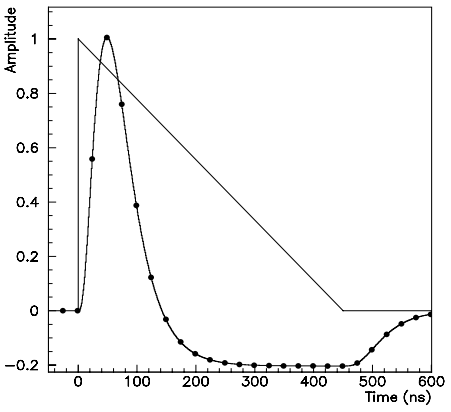

Figure 3: Signal shape as produced in the detector (triangle), and after shaping (curve with dots). The dots represent the position of successive bunch crossings.

The amplitude of the current varies from one sub-detector to another. A value of 2.8 μA/GeV is typical for the EM accordion calorimeters; this drops down to ~0.3 μA/GeV for the HEC. This signal is delivered on the detector impedance, which, to a very good approximation, is a pure capacitance from as low as 75 pF to as high as 2 nF. More information can be found in the LARG TDR Section 10.2. [2]

3. REQUIREMENTS

The main requirements for the read-out electronics can be summarized as:

- The dynamic range of the input is at least 16 bits. The degradation introduced by the read-out system should be minimal.
- The read-out system should be inter-calibrated to better than 0.25% over the whole energy range, in order to achieve a small constant term in the energy resolution.
- The amount of coherent noise per cell should be less than 5% of the level of incoherent noise.
- A pipeline with a depth of at least 2.5 μs should be provided; in addition a large enough derandomizing buffer and a fast enough read-out should allow for a maximum Level-1 trigger rate of up to 75 kHz.
- Cells should be summed in trigger towers $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and the result sent out to the Level-1 processor. The required precision for the analog trigger sums is 5%.
- A fair fraction of this electronics will be located in an area with limited access. High reliability is thus a concern. In addition, although radiation levels at that location are not very large (10^{12} n/cm^2/yr; 20 Gy/yr; 10^{10} ionizing particles/cm^2/yr), this electronics has to be radiation tolerant.
- The large number of channels (~ 190 000) involved requires development of a system with low power consumption and moderate cost.

4. READ-OUT ARCHITECTURE

Signals from the detectors are processed by various stages before being delivered to the DAQ system. Figure 4 shows the read-out architecture as well as the basic elements of the system: preamplifiers, shapers, pipeline memory, digitization, and digital filtering. The data are then sent off to the Level-2 buffers. Much of the digital electronics: control, digital filtering, and Level-2 buffering, is located off the detector, in a control room. This limits digital activity close to sensitive analog electronics to the absolute minimum. The off-detector electronics will use standard non radiation-hard techniques. It will be easily accessible, and can be delivered relatively late; the latest available technology can be used. It will also be more easily upgradable.

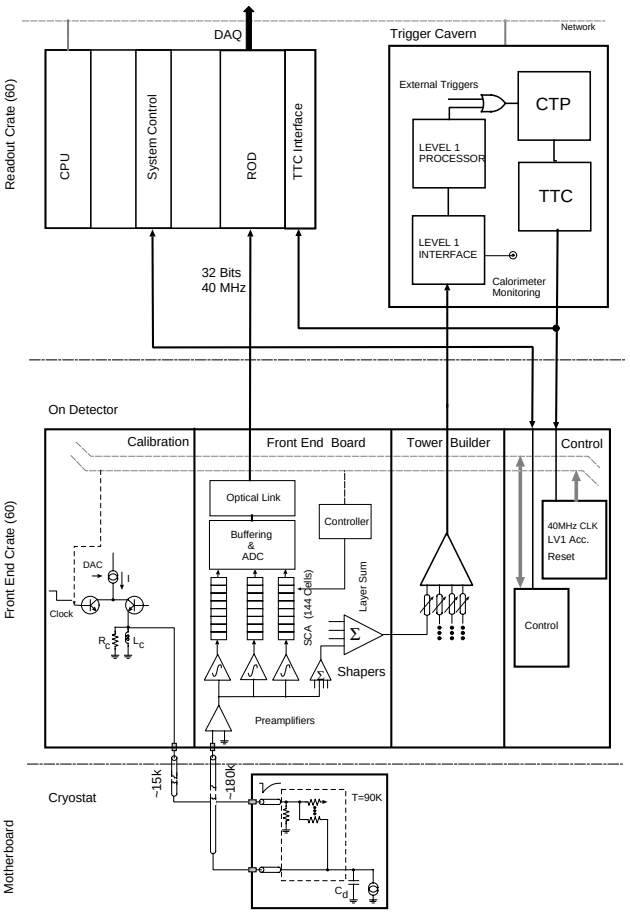

Figure 4: Block diagram of the read-out electronics. In the drawing warm preamplifiers are located on the front-end board, which is the case for the EM and FCAL calorimeters. For the hadronic end-cap calorimeter, a preshaper - that interfaces preamplifiers located in the liquid argon to the standard shaper chip - replaces them.

The clock and control signals (level1 accept, resets...) are generated in the trigger room, where special care has to be taken to minimize trigger latency, and fan-out to the various boards using the TTC system developed by the RD12 collaboration. The global system is split into 8 partitions, which can run independently if needed.

The sensitive analog electronics is housed 'on-detector', in a front-end crate attached to the cold to warm feedthroughs, in the crack between the barrel and end-cap calorimeters and at the rear of the end-caps (see figure 1). This crate is positioned on top of the warm feedthrough flange, effectively becoming an extension of the cryostat Faraday cage. This should efficiently shield the LARG read-out electronics against external electromagnetic radiation. In addition, this keeps the warm part of the signal and calibration cables to a minimum length and therefore minimizes the associated attenuation and noise. The design of the crate system is now well advanced as explained in [3]. It strives to minimize pick-up noise that might be coherent over many channels. It also provides

for an efficient water cooling of the ~3kW dissipated power. Crate production will start early 2000.

5. THE FRONT-END SYSTEM

In the cold, a system of G10 boards gangs electrodes together to form readout cells and holds precision resistors that inject calibration pulses. Small diameter coaxial cables connect to these boards and bring signals to the cold to warm feedthroughs. All these parts are already in production [4, 5].

The front-end crate (FEC) contains several types of boards.
The calibration board houses 128 precision pulsers which inject precisely known current pulses, covering the whole dynamic range, as close as possible to the read-out electrodes through high-precision resistors located in the cold, to simulate energy deposits in the calorimeters. The timing of the calibration pulses is set to reproduce the timing of physics signals, taking into account the variation of time of flight. More information can be found in the G. Perrot's contribution to these proceedings and in [6].

Front-end boards (FEBs) [7] also house 128 channels:

- They amplify and shape the input analog signals. Three gains are used to cover the full dynamic range [8].
- They sum calorimeter cells by trigger tower within each depth layer, and drive the summed signals to the tower builder board.
- They store the signals in a 144 cell deep analog memory (SCA) waiting for the decision by the first level of triggering,
- They digitize the selected pulses, and transmit on optical fibres the multiplexed digital results.

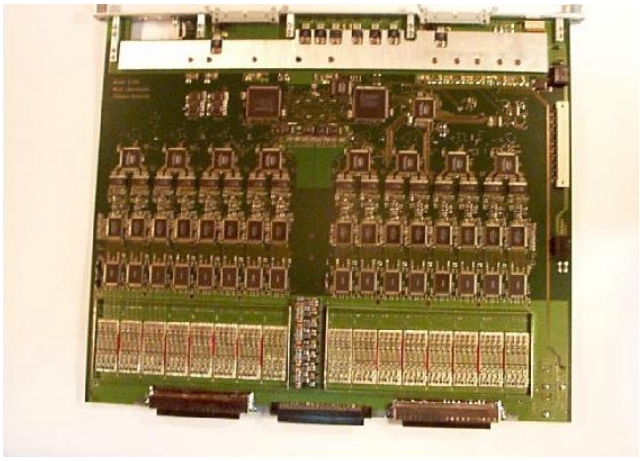

Figure 5: Photograph of a FEB board. The input signals come into the board from the two external connectors at the bottom. The shaped and summed signals for the trigger are output on the middle connector at the bottom. The various sections: preamps, shapers, SCA's, ADC's are clearly visible. Voltage regulators are laid out in the top row.

Production of amplifiers is now well-advanced [9] as can be seen from H. Brettel's and M. Citterio's contributions, and a preproduction run is going to be ordered very soon for shapers and SCAs.

For the EM barrel and endcap calorimeters, Tower Builder Boards (TBBs) [10] are used to perform the final level of analog summation to form trigger tower signals and to transmit the analog signals to the Level-1 cavern for digitization and processing by the Level-1 trigger processor. A prototype has been built and tested in the test beam. For the HEC and FCAL calorimeter, Tower Drivers (TDB) transmit the signals to the level 1 cavern.

Control boards receive and distribute the 40 MHz clock, the level-1 trigger accept signal, as well as other fast synchronous signals and information to configure and control the various boards in the crate.

Monitoring boards read out various monitors, like liquid purity and temperature sensors.

More information about the content of every crate in the system and on how every calorimeter cell gets routed to its FEB can be found in [11].

Quite a substantial amount of power (~ 250 kW) is needed to supply the large number of electronics channels in the front-end system. None of this power should be transferred to the surrounding detectors and liquid cooling is mandatory. To minimize the risk for leaks, the cooling fluid will be circulated below atmospheric pressure, typically 600 mb into heat exchanger plates mounted on every front-end board. Heat conductive pads will be used to eliminate air gaps between components and cooling plates and maximize heat transfer. Much more information can be found in the contribution by H. Takai and in [3].

The distribution of this large amount of power has to be done carefully. Each front-end crate will have its own low voltage power supplies. Compact high power DC-DC converters with good noise properties have been identified. First tests seem to indicate sufficient radiation tolerance. The current base line is then to locate these supplies on top of each crate, minimizing the length of the low voltage lines and associated loss of power. As this is a poorly accessible area, redundancy is to be built into the system. See contribution by M. Citterio for more on this. These supplies will be 'isolated'. Strict control of ground loops will be observed, and there will be only one location allowed where connection to ground is made. The cryostats with all their cryogenic lines and services will be electrically insulated [12].

6. "MODULE 0" ELECTRONICS

To test, in beam, calorimeter modules and to qualify their production, a read-out electronics was needed. This was used as an opportunity to prototype the front-end

ATLAS electronics. About 6000 channels of ATLAS like electronics have been produced and ~2000 are already installed in the beam. In this exercise, we learnt a lot about the real ATLAS electronics and some preliminary results look already quite encouraging:

- The boards were efficiently cooled; the board temperatures were between 25 °C and 28 °C (i.e. below ambient at the time of the test) and very stable with time.
- The pedestal stability is very good: 0.1 ADC counts over a 3-week period.
- The incoherent electronics noise closely matches expected values i.e. ~20/50/35 MeV for the EM front/middle/back cells.
- The coherent noise is slightly larger (5-7%) than the ATLAS goal of 5%. However this is already a very good result as in the test beam we are not yet using optical links.
- The measured integral non-linearity is below 0.25% on all three shaper gains.
- Figure 6 shows samples measured on a single 100 GeV electron pulse in a middle layer cell. The pulse shape is nice and follows expectation.

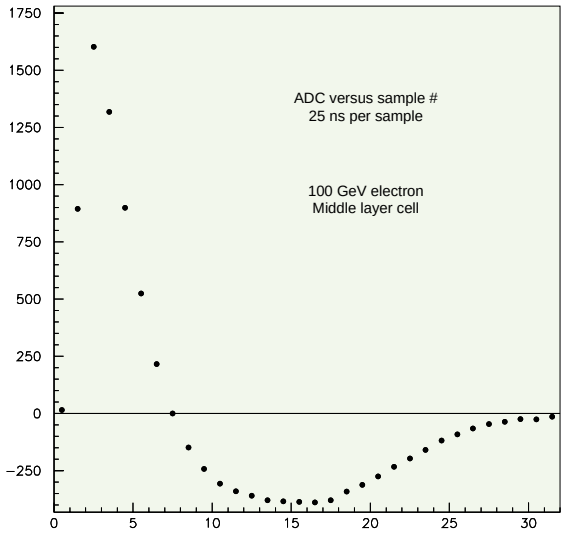

Figure 6: Samples, 25 ns apart, measured on a single 100 GeV electron pulse in a middle layer cell.

7. OFF-DETECTOR ELECTRONICS

For reasons connected with the construction schedule of the experiment, the front-end electronics has received considerably more attention than the electronics that will reside off the detector.

7.1 Trigger clock and control system

In the Level-1 cavern, ~50 meters away from the detector, signals from trigger towers are received and delivered to the calorimeter Level-1 trigger processor. The central trigger processor (CTP) will deliver not only physics triggers but also calibration signals and triggers. These signals, together with the 40 MHz clock and other synchronous commands, are transported to the front-end crates and to the read-out crates by the TTC system (timing trigger and control) developed in the RD12 project. To benefit from the excellent intrinsic time resolution of the detector (50 ps at high energy), clock jitter should be kept as low as possible (< 100 ps).

To ease the timing in of the system, fibers distributing the clock will be cut to length and/or their transit time measured and programmable delay lines in calibration boards will be preset to reproduce the timing of physics signals. This should allow not only to align in time the various calorimeters, barrel, end-cap... but also to time in the level 1 processor, the CTP and the distribution of the level 1 accept signals. These adjustments will be checked and refined by analyzing real shower pulses from collisions.

7.2 Read-out driver system

To each front-end crate is associated a read-out driver crate. A set of such front-end crate - read-out driver crate pairs, together with a TTC driver form a partition controlled by a master CPU. Eight such partitions are considered 4 for each end of the experiments. This would allow running independently the EMB, the EMEC, the HEC and FCAL calorimeters.

The read-out driver crate contains:

- a CPU connected to the network to control this crate and the associated front-end crate;
- a SPAC master module to configure or down-load parameters into the various boards of the front-end crate or to read back registers [13];
- a TTC and BUSY module to receive the TTC information, fan it out to the RODs and collect their BUSY signals
- Read Out Driver (ROD) modules, which receive raw data from the FEBs and produce the corresponding energy, time, and some form of data quality measure, sending the result to the DAQ, i.e. to the Read Out Buffer (ROB) modules.

Fast unidirectional, 1 Gbit/s optical links connect the FEBs to the RODs. A frame of typically five samples centered on the bunch crossing of interest is sent down the link to the ROD module for digital processing. This is accomplished using the well-established method of optimal filtering. In practice one obtains a weight for each sample which results in the minimum error on the energy subject to the constraint that the pulse can be moved in time without affecting the result to first order. Any loss in energy resolution due to small phase jitter between the pulse and the clock is minimized. The weights are chosen to minimize the total noise (electronics pile-up) for the current value of the luminosity, and the quality of the waveform can be checked to detect events subject to large

out-of-time signal overlaps. The available computing power in these modules will also be used to monitor every channel. Examples include checking for drift in the phase of the clock with respect to the particle signal, histogramming energy spectra, and the preprocessing and histogramming of data during calibration runs. More detailed information can be found in the contribution by W. Cleland.

8. NEXT STEPS

A major milestone in the development of the LARG electronics has been met with the production and successful running in of ~ 6000 channels of ATLAS like electronics. However, several short cuts had to be taken given the rather tight schedule:

- Digital optical links to connect the FEBs to the RODs: We are currently using shielded twisted copper pairs. These will be replaced by optical links. We already have hints that this will reduce the amount of coherent noise. A lot of work has been done to assess commercial solutions i.e. based on the HP G-Link chip set. The main pending issue there is radiation tolerance and more specifically SEE effects. A lot of information can be found in R. Stroynowski's contribution.
- Distribution of TTC signals : In ATLAS, we are planning to use the standard TTC system as developed by the RD12 collaboration. We plan to test this distribution scheme in the test beam set-up as soon as enough standard TTCRx chips become available.
- Radiation tolerant electronics : Though the radiation tolerance of our main critical components (preamps, shapers, SCA,...) is now well established, there are many other areas where a lot of work is needed:
  a. Power regulators, (we are planning to use the work of P. Jarron et al. from RD49)
  b. Logic: we are working on moving logic cicuits described in high level languages (i.e. VHDL) and prototyped in FPGAs to custom ASICs using the DMILL technology.
  c. ...

All this effort aims at producing two full crates of hopefully final front-end electronics by mid 2001. This would allow exercising these crates for some time before launching the board production for ATLAS by mid 2002. Note however, that some parts of the front-end electronics will be needed even sooner – i.e. the front-end crates or the front-end chips: shapers, SCA - or are already in production like preamplifiers.

9. REFERENCES

Most of the references below are accessible from the Web, using the EDMS system, starting from the ATLAS main page.

1 Overview of the LARG electronics:
ATL-AL-EN-0003

2 ATLAS Liquid Argon Calorimeter TDR:
CERN/LHCC/96-41

3 Liquid Argon Front-End Crate:
ATL-AL-EN-0004

4 The LAR Mother Board System. Documentation:
http://www.usatlas.bnl.gov/lar/mb/

5 PRR of LArg Cold Cables – Report:
ATC-RA-ER-0003

6 The LARG Calorimeter Calibration Board:
ATL-AL-EN-0005
ATL-AL-EN-0006

7 Design of the ATLAS LAr Front End Board:
ATL-AL-EN-0009

8 The LAr Tri-Gain Shaper:
ATL-LAR-98-092

9 Report on the HEC Cold Electronics PRR:
ATL-TC-ER-0013
Liquid Argon Calorimeter Preamplifiers PRR:
ATL-TC-ER-00xx

10 The Level 1 Trigger and the Tower Builder Board:
ATL-AL-EN-0007
The ATLAS Receiver/Monitor System:
ATL-AL-EN-0010

11 Cabling of the EM calorimeters:
ATL-AL-ES-0004
ATL-AL-PITT-ES-9.0

12 Guidelines for Grounding. V. Radeka:
http://www.usatlas.bnl.gov/lar/ground.html

13 SPAC : Serial Protocol for the ATLAS Calorimeter:
ATL-LAR-98-093