# COLD ELECTRONICS FOR THE LIQUID ARGON HADRONIC END-CAP CALORIMETER OF ATLAS

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## 1. ABSTRACT

For the ATLAS hadronic end-cap calorimeter a monolithic Gallium Arsenide front-end chip has been developed. The full production (6600 chips) is completed. Basic characteristics and results of mass measurements are presented. The manufacturing of 360 preamplifier and summing boards, equipped with these chips, is in progress. Boards undergo the ATLAS quality assurance procedure in an automatic equipment. Special front-end boards - a subset of the circuitry of standard FEBs - have been built with pole-zero compensation hybrids instead of warm pre-amplifiers. At the recent beam runs in June and August 99 they where installed in a standard front-end crate on top of a LAr-feed through. Beside physics studies and calibration of the stacks mainly the coherent noise has been investigated.

## 2. OVERVIEW

HEC MODULE

⇒ HEC module has 4 longitudinal segments

⇒ GaAs chips are mounted on preamplifier and summing boards (PSB) at the top of the module.

ELECTRONICS CHAIN

⇒ Cold Electronics: LAr gap, HEC cables, GaAs chips, Quadrant cables

⇒ Warm Electronics: Preshaper, Monolithic shaper, DAQ

## 3. ELECTRONICS CHAIN

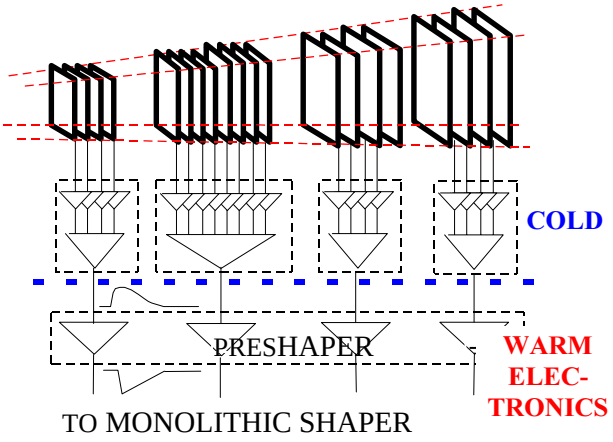


Figure 1 Summing scheme

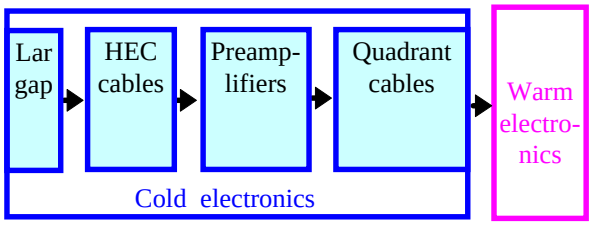


Figure 2 Electronics chain block diagram

## 4. COLD ELECTRONICS

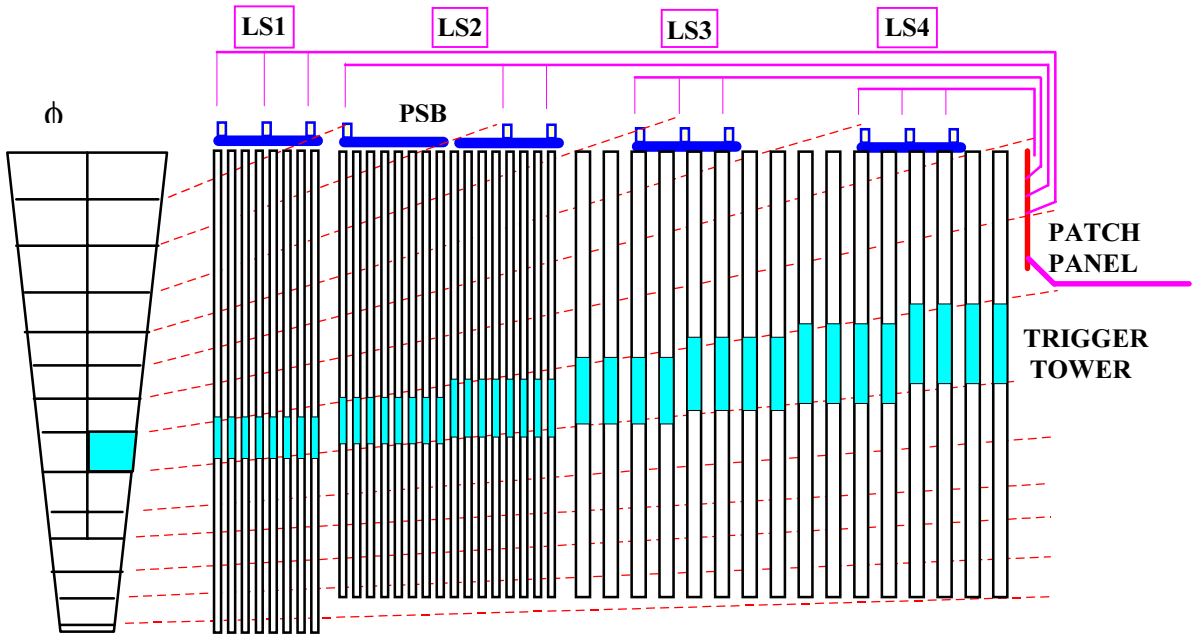


Figure 3 HEC module. Left: Readout board with pad structure Right: Cross section with a trigger tower

### *4.1 Preamplifier and Summing Stages*

⇒ ASIC GaAs designed by MPI
⇒ Process: TriQuint QED-A (1µm)
⇒ Internal: 8 preamplifiers and 2 drivers
⇒ External: decoupling capacitors, driver feedback components, summing connections
⇒ Quantity: 67 chips/Module, 4288 chips/HEC
⇒ 6600 chips on 18 wafers produced and delivered
⇒ Detailed studies of several chips warm and cold

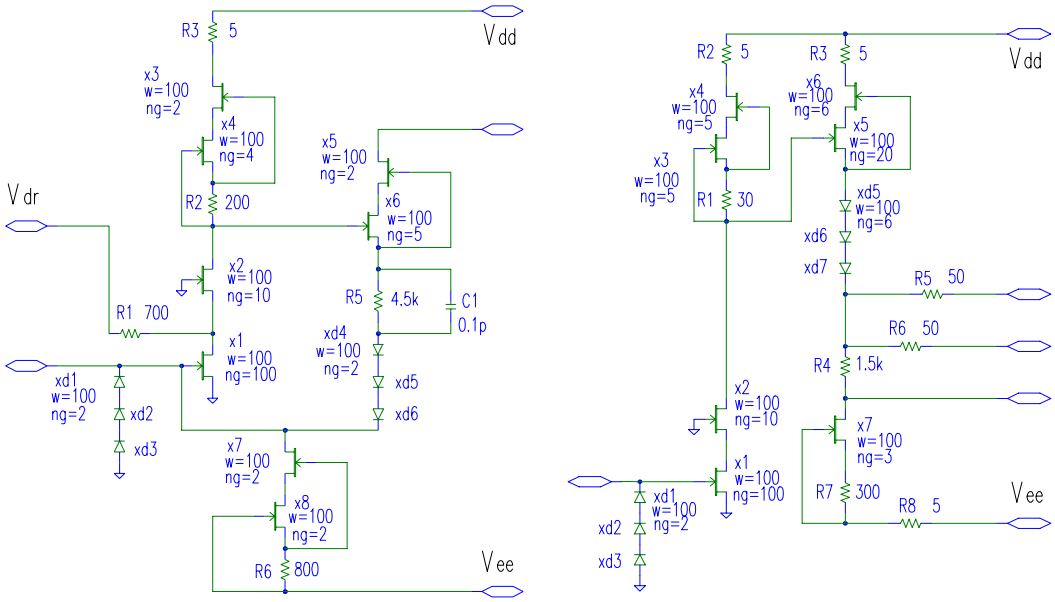


Figure 4 Circuit diagram of preamplifier (left) and driver stage (right)

## *4.2 Dynamic Characteristics of Chip*

⇒ Input impedance close to 50Ω

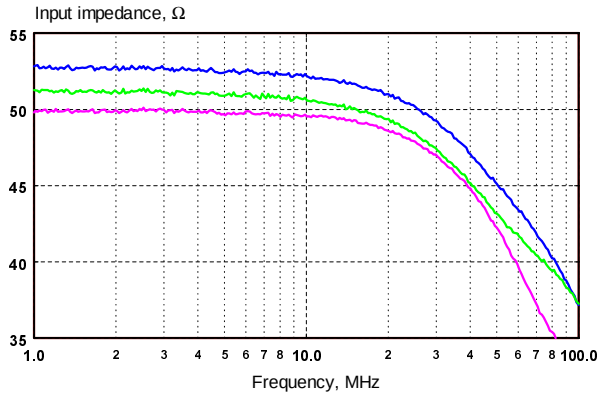


Figure 5 Input impedance of different chips

⇒ Nonlinearity in full LHC range less than 1.4% for preamplifiers and 1.6% for complete channel
⇒ Signal rise time close to expected value T=Ri*Ci
⇒ Transfer function is adjusted by driver feedback

## *4.3 Signal to Noise Ratio of Chip*

⇒ Equivalent noise current is 20% less than specified value. Peaking time in ATLAS is 50ns.

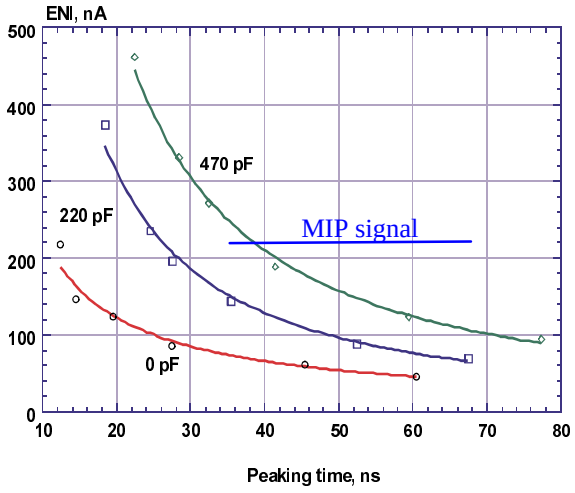


Figure 6 Equivalent input noise current

⇒ Some excess noise appears at LAr temperature if Vee exceeds the normal working range.
⇒ For nominal Vee the noise sources are:
- white serial Rs=35Ω
- white parallel Rp=800Ω
- parallel flicker corner $F_f$=1.5 MHz

## *4.4 Chip Selection*

⇒ Each chip is measured at room temperature before being soldered on the board.
⇒ Criteria are:
- gain of each preamplifier
- gain variation between channels
- noise
- risetime

⇒ 2 types of measurements: summing 8 preamplifiers to one driver and summing 4 preamplifiers to one driver
⇒ By now all 6600 chips are measured with summing 8. The summing 4 measurement is in progress. 5600 chips are measured , the remaining will be finished at end of October.
⇒ 7% of chips dead, 80% keep HEC specifications

## *4.5 Preamplifier and Summing Boards*

⇒ 12 to 16 chips/PSB, 5 PSBs/module
⇒ 320 PSB / HEC, 134 produced
⇒ 59 tested in liquid N, 6 PSB/load (2 days)
⇒ 2 loads/week = 12 PSBs

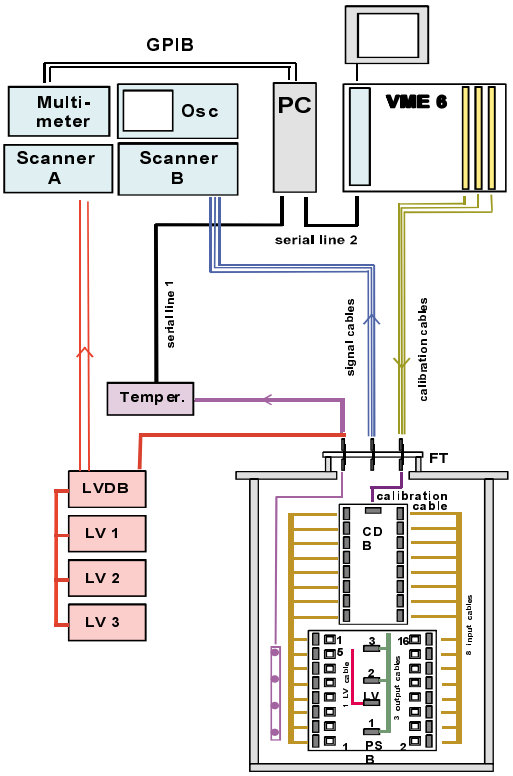


Figure 7 PSB test setup

### *4.6 PSB Test procedure*

The production includes a visual inspection after the cleaning process. Warm and cold functional tests of each board have to proof, that no chip has been damaged by handling or soldering, before the PSBs are measured by the automated setup in the cryostat.
The PSBs are inserted in groups of six, the cryostat is evacuated, cooled and filled with liquid nitrogen. A full measurement of all channels is carried out according to ATLAS quality specifications and all data are recorded for later reference. Then the nitrogen is removed and the cryostat warmed up.
The whole procedure lasts about 2 days.

### *4.2.2 Results*

Even if the statistic up to now is low, we can see already a trend. We found 10 problems at 134 boards, mainly bad soldering. 3 chips out of 1680 (on 59 PSBs) did not meet their specifications in cold.

## 5. TESTS at CERN

### *5.1 Modules and Cold Electronics*

PSBs are installed on the modules and undergo the foreseen procedures in the cryostat. If no problems show up, the boards Dremain in position and the complete modules with electronics are stored until the assembly of the wheel.

### *5.2 Entire Electronics Chain*

Beside its main purpose as a test and calibration tool, the setup at CERN offers valuable possibilities for test of elctronic circuitry in an environment comparable to the situation at ATLAS.
In contrast to the other liquid argon calorimeters the preamplifiers and summing stages of HEC are inside the cryostat and emerged in the liquid argon.
The motivations for the cold electronics were:

- less thermal noise
- short input cables reduce pickup
- local summation requires less feedthroughs
- less interference from digital part

The front-end boards (FEB) outside are standard, with the only exception that preshapers are mounted at the signal input instead of warm preamplifiers.
A pole-zero cancellation in these hybrid circuits compensates the effect of different gap capacitances on the signal rise time.
A gain stage with an appropriate time constant delivers the correct signal shape, amplitude and polarity for the following monolithic shaper.

### *5.2.1 Final Setup at ATLAS*

The FEBs are mount in the front-end crates, which are an integral part of the Faraday cage (cryostat). The output signals are transmitted to the data acquisition (DAQ) via optical links (Fig. 8).

### *5.2.2 Test Setup at CERN*

As the final FEBs are not yet available and the link to the DAQ is still missing, we applied FEBs which contain only a subset of the final circuitry, namly preshapers, monolithic shapers and drivers for coaxial cables. The analog to digital converters (DAQ) are contained in a separate crate together with a VME interface for the Test DAQ (Fig.9). An additional branch has been established which delivers the same data format as the final FEB. If required, thus transmission to the central DAQ will be possible, in parallel to current local test activities.

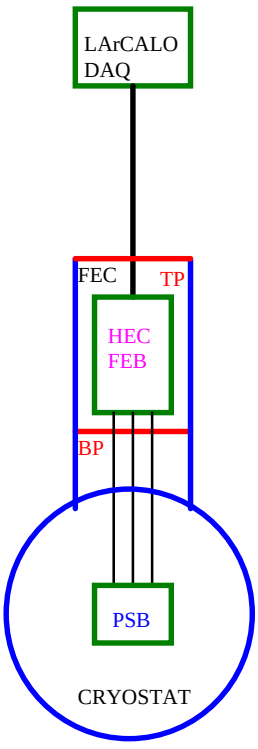


Figure 8
Final setup at ATLAS

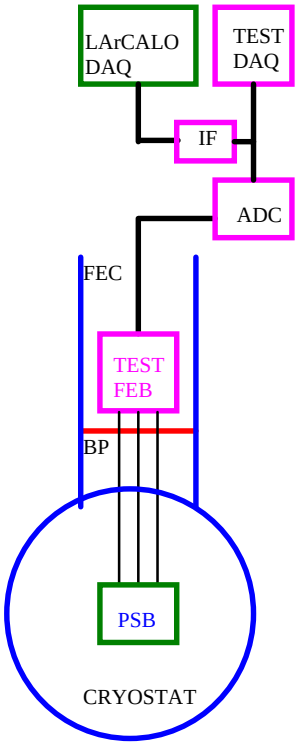


Figure 9
Test setup at CERN

### *5.3 Results*

The mechanics of the front-end crate FEC which we have there, is far from the final one. It has no top cover and at our first run during this year there was not even a base plain. The cables, coming from the feedthrough have been connected directly to the inputs of the FEB. As a consequence we had a high level of coherent noise. After installation of a base plain the coherent noise was reduced dramatically. The total noise of all channels is shown at fig. ...There are a few channels (1, 100, 200 for example) which have excessive noise. We tried to find the nature and origin of this noise. The fig. ...and ...show a the auto-correlation function of a good and a noisy channel. We find that the excessive noise is not white, but there must by an oscillation. When the power of the preamplifiers was switched off, the white noise of all channels diminished but the oscillations remained. The origin is obviously not a preamplifier. It seems that the inputs of the pre-shapers are sensitive to capacitance and the edges of connectors or strip-lines are not perfect (wrong impedance). This has to be improved. At the correlation plot (fig. ...) we see that the bad channel influences the next neighboring channels.

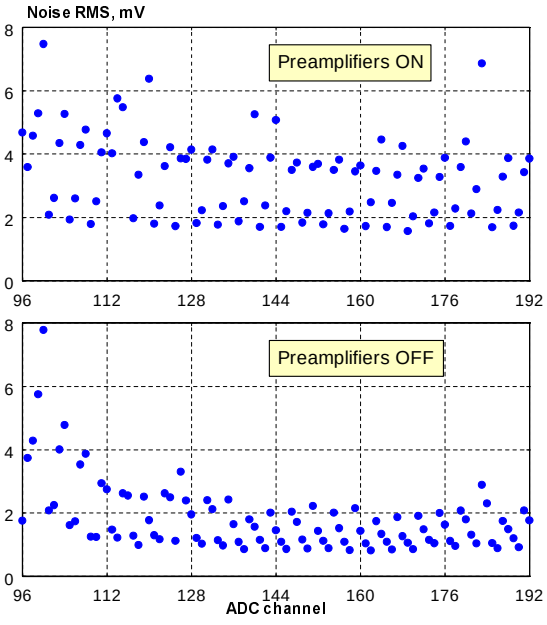


Figure 10 Total noise RMS at input of ADCs

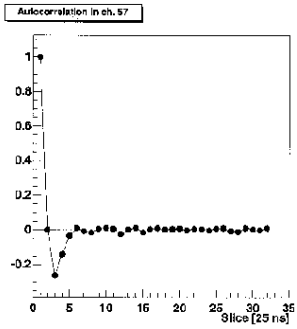


Figure 11 Auto-correlation good channel

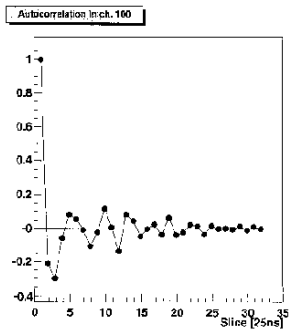


Figure 12 Auto-correlation bad channel

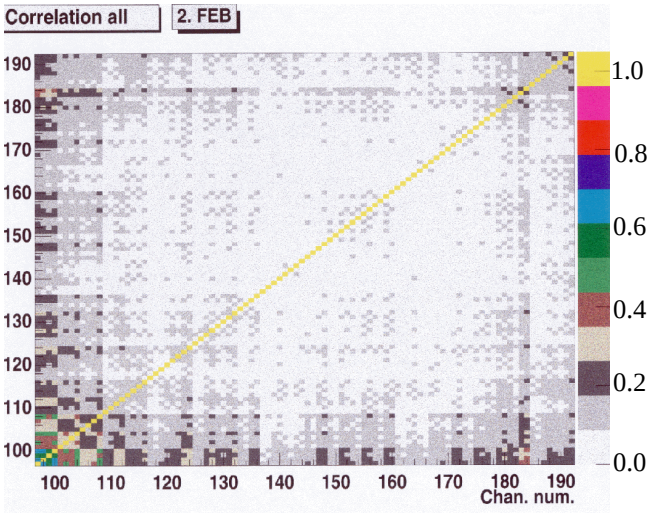


Figure 13 Cross-correlation

## 6. References

1. Cold Electronics for the Liquid Argon Hadronic End-Cap Calorimeter of ATLAS, presented by L.Kurchaninov,
VIII International Conference in High Energy Physics