# A PROTOTYPE FAST MULTIPLICITY DISCRIMINATOR FOR ALICE L0 TRIGGER

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FOR THE ALICE COLLABORATION

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*Abstract*

The design details and test results of a prototype Multiplicity Discriminator (MD) for the ALICE L0 Trigger electronics are presented.

The MD design is aimed at the earliest trigger decision founded on a fast multiplicity signal cut, in both options for the ALICE centrality detector: Micro Channel Plates or Cherenkov counters.

The MD accepts detector signals with an amplitude range of plus-minus 2.5 V, base duration of 1.8 ns and rise time of 300-400 ps. The digitally controlled threshold settings give an accuracy better than 0.4% at the maximum amplitude of the accepted pulses. The MD internal latency of 15 ns allows for a decision every LHC bunch crossing period, even for the 40 MHz of p-p collisions.

## 1. INTRODUCTION

A functional scheme for the MD as an element of ALICE L0 Trigger [1,2] Front-End (F.E.) electronics is shown in Figure 1, for the proposed MCP based option. In the scheme shown in the figure [3,4,5], fast passive summator F.E. electronic units Σ [6], integrated in the detector, are used for linear summation of isochronous signals coming from pads belonging to an MCP disk sector. These signals, whose amplitude is proportional to the sampled multiplicity, are fed to the MD. The discriminator produces a multiplicity trigger PTM (Pre-Trigger on Multiplicity) according to programmable threshold codes delivered by a Source Interface Unit (SIU), through the ALICE Detector Data Link (DDL).

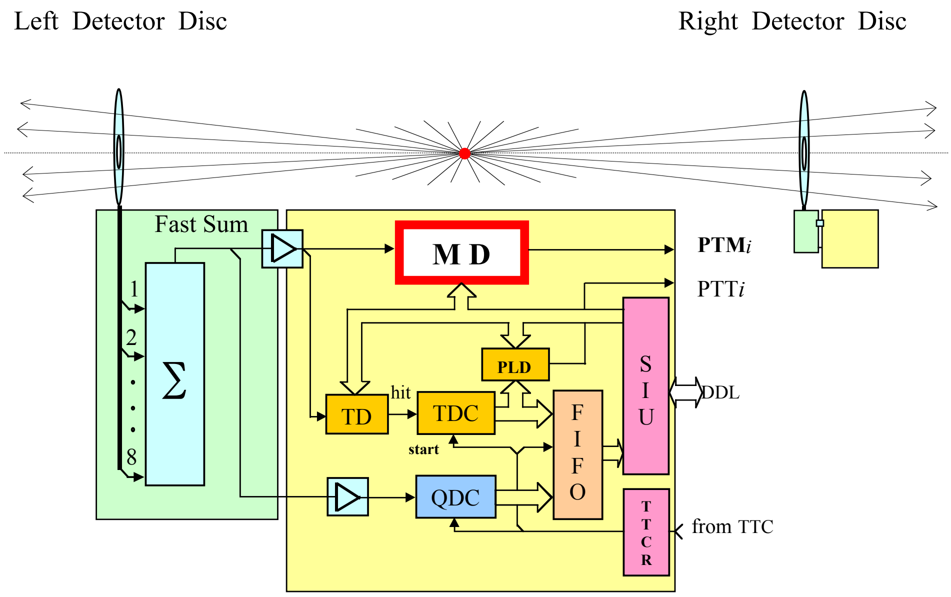


**Figure 1: General layout of the Multiplicity Discriminator (MD) within ALICE L0 Trigger Front-End Electronics (TTCR = the LHC Timing, Trigger and Control Receiver; TD = Time Discriminator; TDC = Time to Digital Converter; QDC = Charge to Digital Converter; PLD = Programmable Logic Device).**

Each i-th FEE card has to produce $PTM_i$ in conjunction with another, time trigger signal $PTT_i$ (Pre-Trigger on Time of Flight) needed to provide a precise time mark for the measured particles collision time T0. Pipe-line memories are needed to store the T0 and charge information, for each MCP sector, at the 40 MHz rate of the LHC clock.

All MD's $PTM_i$ as well as all $PTT_i$ are collected together, within fast programmable logical units (not shown), to compare the signals from different sectors and produce a L0 centrality trigger.

## 2. THE MD CONCEPTUAL DESIGN AND SCHEMATICS

The functional scheme for the prototype MD is presented in Figure 2. The approach used in the MD design was to implement a leading edge discriminator by a proper combination of a voltage comparator and a digital-to-analog converter. Inputs InA and InB for analog signals with positive and negative polarities have been foreseen.

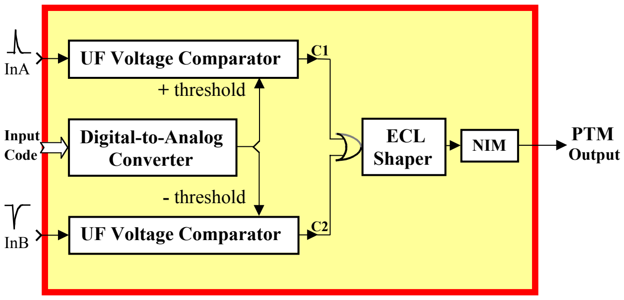


**Figure 2: Functional scheme of the prototype MD.**

An Ultra-Fast (UF) ECL-compatible voltage comparator AD96685BQ from Analog Devices [7] has been selected as the basic MD component. This comparator has a typical propagation delay of 2.5 ns and a high precision differential input stage with a common-mode signal range from -2.5 V to +5 V,.

To provide the required accuracy for multiplicity discrimination, within the dynamic range of the fast preamplifier 0 ÷ ±2.5V, an 8 bit DAC, with control settings of 10 mV threshold resolution, is sufficient [1]. This DAC, realized on the AD558KD-DACPORT base [8], delivers an output voltage from 0 to ±2.56V with an accuracy of ± 1/4 LSB (1LSB = 0.39% of full scale), that corresponds to 0.1% of the device dynamic range. The ECL shaper is implemented using a high-speed Motorola MECL 10KH D-trigger [9] and a series of logical gates [10] to achieve the correct form and the width of the output signal needed. The NIM level converter provides a standard output signal of 16 mA for 50 Ohm load. The total latency of the PTM trigger output, referred to the leading edge of fast input signals, is about 15 ns; the PTM pulse width can be adjusted from a minimum of 10 ns up to 20 ns, using a potentiometer.

Two operational amplifiers from NS [11] provide the comparator inputs with a differential unbalance of 5÷10 mV, to avoid exciting the circuit with noise under zero threshold. The prototype MD board is mounted in a double-width NIM module. Two high frequency 50 Ohm coaxial BNC-type connectors, isolated from the module frame with an analog ground, and a miniature LEMO, with a standard grounded case, are placed on the front panel for analog inputs and logical output signals respectively. Two hexadecimal constant register switches, also mounted on the front panel, allow for the setting of binary threshold codes.

## 3. IN-LAB TESTS OF THE MD PROTOTYPE

Tests were performed on the MD in Bari and Dubna. The aim of these tests was to study the MD sensitivity to fast input signals and to obtain a calibration curve for the MD thresholds. S curves were also performed to evaluate the width of the MD transition gap near threshold.

### *A STUDY OF THE MD SENSITIVITY TO INPUT SIGNALS*

It is essential, for a correct use of the MD, to study the correlation between preset and effective thresholds. In fact a minimum input signal amplitude Ueff should be applied in order for the comparator to be triggered at the preset DAC reference UDAC. It is a known that, when handling very fast and low-amplitude signals, the shorter and the smaller the input pulses, the bigger is the difference between the applied and the effective threshold values [16]. This circumstance could be explained due to a certain minimum of effective charge Qeff, which must be accumulated at the MD input capacity Cin, to reach UDAC and then to trigger the comparator by some additional charge Qtr :

$$Q_{eff} = C_{in}\, UDAC + Q_{tr} \quad (1) .$$

Pulses of smaller integrated area require more and more extra-charge compensation and for the MCP, which produces signals of almost fixed width, this compensation can be achieved only by increasing the pulse amplitude.

In order to obtain a calibration curve for the comparator thresholds and to study the sensitivity of the MD to input signals, a series of measurements has been performed using a LeCroy 9211 [12] programmable pulse generator. The pulse generator time parameters were chosen and fixed such as to simulate MCP output signals. So we used the minimum available value of 0.9 ns for leading and trailing edges (Te), and a pulse width of 2.5 ns base (Tb), at a selected repetition rate of 40 MHz.

The fine and high stabilized tuning of the generated pulse amplitudes, with 5 mV programmable steps, made it feasible to investigate effective thresholds precisely over the full prototype MD linear range. Here we present some results of these measurements, corresponding to DAC voltage values in the reduced range 0 to 500 mV, with 50 mV steps.

In Figure 3 we present, as a function of the DAC threshold values, the effective voltage thresholds (squares) obtained and the absolute difference between effective and DAC voltage thresholds (triangles).

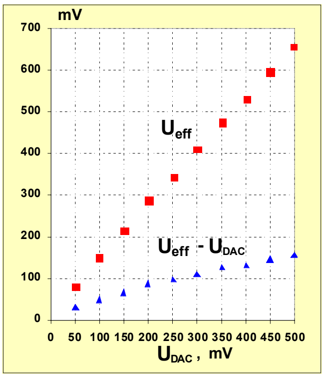


**Figure 3: Effective vs. DAC thresholds for 500 mV sweep of signals with 1.6 ns FWHM and 0.9 ns edges.**

The percentage of this difference, with respect to the DAC values is given in the figure 4, where an increase for signals of smaller amplitude is clearly observed, going from 31% needed at 500 mV DAC threshold up to 60% at 50 mV.

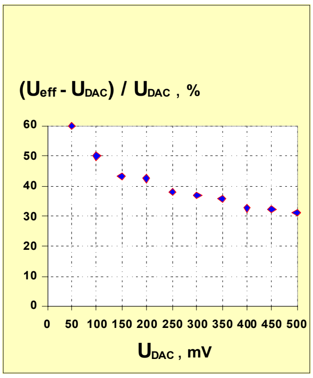


**Figure 4: Relative effective over DAC thresholds prevailing for 500 mV sweep of signals with 1.6 ns FWHM and 0.9 ns edges.**

An estimation of the sensitivity of the electronic scheme proposed for the MD prototype, would involve a measurement or calculation of the effective charge $Q_{eff}$ according to (1). This is hard to perform directly but can be roughly achieved using the measured data on $U_{eff}$ and the known time parameters settings of the LeCroy pulse generator.

In fact, by fitting the LeCroy 9211 output pulses with an isosceles trapezium-like shape (Figure 5), it is possible to calculate the full electric charge Qpef carried by every pulse with amplitude Ueff, time base Tb and equal Te edges, as an integral of the pulse current ip(t):

$$Q_{eff} \sim Q_{pef} = \int_0^{T_b} i_p(t)dt = (T_b - T_e)U_{eff}(U_{DAC})/R_S$$

where Rs=150 Ohm is the total equivalent schematics resistance limiting the current charging Cin .

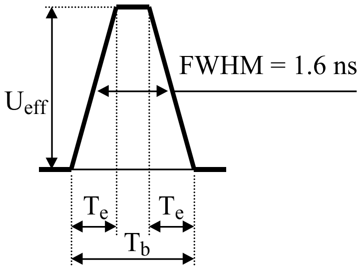


**Figure 5: Approximate shape of the generated pulse, indicating the quantities Te = 0.9 ns and Tb = 2.5 ns.**

The calculated effective charge values versus DAC voltage thresholds are shown in Figure 6. The implicit linear Q(U) dependence is evident from the fit presented in the figure, corresponding to the analytical expression: Q = 0.0136U + 0.2557.

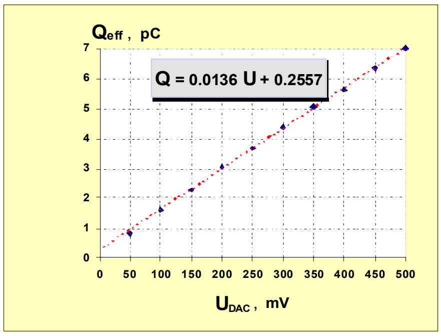


**Figure 6: Effective charge vs. DAC thresholds for 500 mV sweep of signals with fixed 1.6 ns FWHM and 0.9 ns equal edges.**

A comparison of this formula with the equation (1) allows some considerations:

- the input capacity $C_{in}$ plays an especially important role because the lower the $C_{in}$ value, the smaller $Q_{eff}$ is for a given UDAC and the faster this value can be achieved;

- for our prototype MD $C_{in}$ = 0.0136 pC/mV=13.6 pF, and, keeping in mind $C_{in}= C_c+C_m$, where $C_c$ = 2 pF is the comparator input capacity, a parasitic input capacity of the MD mounting Cm of 11.6 pF must be considered;

- a $Q_{tr}$ value of about 0.26 pC can be inferred from (1). This value should be considered as the minimum of over DAC threshold pulse charge to trigger the scheme, i.e. the MD sensitivity.

## *B S CURVES*

In order to test the MD performance, S-curves were produced, at 3 different threshold values, to evaluate the width of the MD transition gap, near threshold.

Extremely precise, fixed width pulses (3.5 ns FWHM) were sent simultaneously to the MD and to a reference LED-type discriminator, set at its minimum threshold over noise (20 mV). The pulse height of the generated signal was varied in steps of 2.5 mV.

The results are shown in figure 7. The MD shows a good threshold accuracy, reaching ≈ 100% efficiency in short threshold ranges: ≈ 3 mV at 360 mV and less then 10 mV at 1080 mV threshold. These plots give, for all 3 settings, an almost constant ratio of (threshold gap/threshold setting) not exceeding 1%, and uncertainties which are, in any case, smaller then the minimum setting step (10 mV).

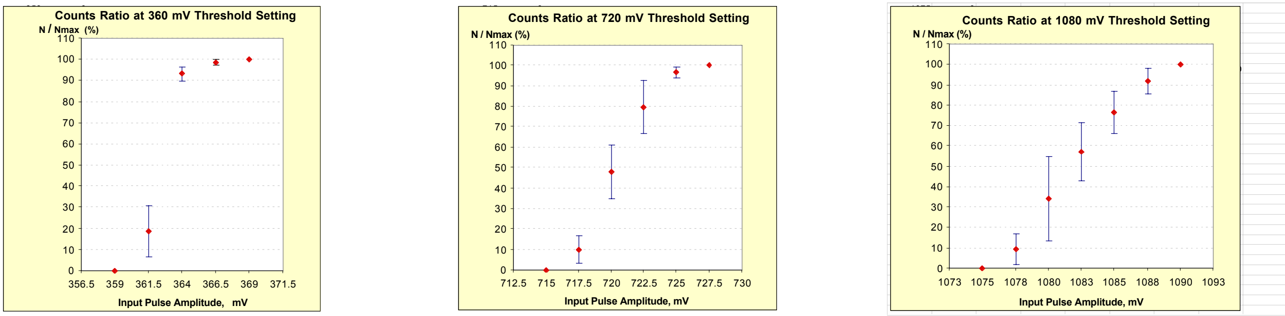


**Figure 7: S curves for 360, 720 and 1080 mV threshold setting.**

## 4. IN-BEAM TESTS OF THE MD PROTOTYPE

A first test of the prototype MD was performed in the CERN experimental area PS/T10, with muon beams of 7.5 GeV/c. This test was planned to study he time resolution and the efficiency of different micro channel and micro sphere plate-based vacuum sectors for the ALICE T0 / Centrality detector [13]. Several modules of fast electronics, including high-speed amplifiers and discriminators were also tested.

The MD module was plugged in a front-end electronics rack used for time-of-flight measurements, during 10 runs, in place of specialized fast timing discriminators, such as Constant Fraction, Double Threshold- [14] and Pico-Timing [15] - type schemes, at a distance of about 5 m from the tested detectors. The experimental setup for a single channel of the electronics is shown in Figure 8. Various combinations of new specialized ultra-fast SMD devices [6] with a different gain, in the range 7÷30, were tested to search for the best signal/noise ratio. A LeCroy 2228A TDC of 50 ps LSB was used for Time-to-Digital conversion.

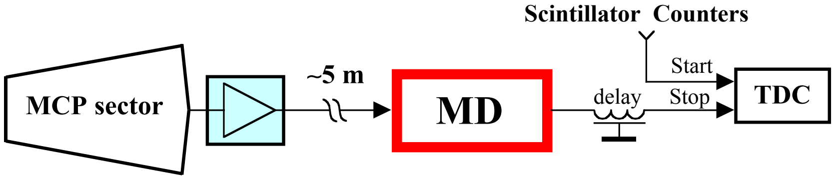


**Figure 8: Experimental arrangement of the prototype MD tests with PS CERN / T10 setup facilities.**

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The experimental aim of this test was two-fold:

a) to simulate a study of multiplicity / centrality versus the prototype MD threshold.

b) to test the timing properties of the prototype MD;

In figure 9 we show an experimental plot giving the ratio $D/D_{max}$ VS different values of relative MD threshold settings $U_{DAC}/U_{DAC(max)}$ , where $D = N_{TDC\text{-}stop}/N_{TDC\text{-}start}$.

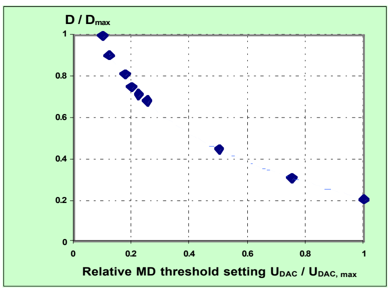


**Figure 9: Relative TDC start/stop counts ratio VS the MD relative threshold setting.**

The fitted curve of figure 9 reproduces well the shape of a single particle distribution (figure 10), showing the correct operation of the MD with short and fast pulses.

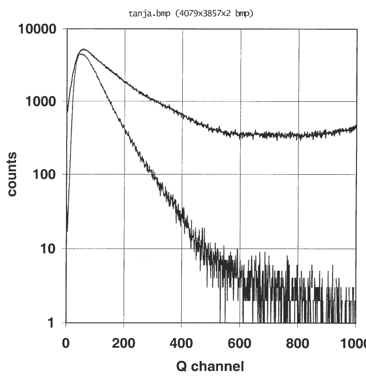


**Figure 10: Single and multiparticle distributions (p-Pb and Pb-Pb)**

Another experimental result is presented in figure 11, where a TDC histogram of 5115 accepted events is shown. The fit gives a resolution of about 120 ps, a rather good result for a discriminator not optimized for timing applications.

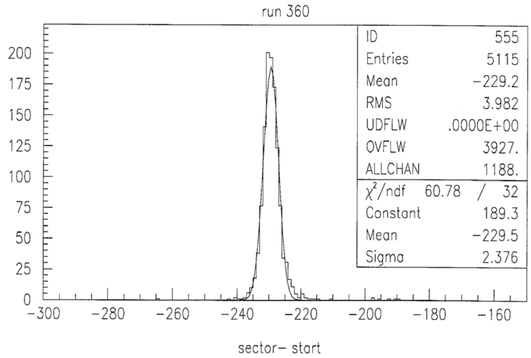


**Figure 11: Example of events over TDC channels distributions from the prototype MD tests at CERN PS (1 TDC channel = 50 ps).**

## 5. CONCLUSIONS

A prototype amplitude discriminator, for the ALICE L0 multiplicity Trigger, has been designed, elaborated and tested. The discriminator was designed to stand short nanosecond signals coming from the ALICE T0/Centrality detector, based on Micro Channel Plates.

Commercially available, inexpensive and fast components have been used to implement the MD prototype. It features an input signal range from 0 to ±2.5V, a programmable threshold control with 8 bits resolution, and an output signal latency of 15 ns.

The minimum input signal charge, to trigger the comparator over the DAC threshold, has been found in about 0.26 pC.

Experimental tests of the prototype multiplicity discriminator, using an MCP-based detector, have been carried out at the CERN PS beam facilities. While applying the discriminator for timing in MIPs time-of-flight measurements, a resolution of ~120 ps has been obtained. The MD was also tested by studying the response to real MCP signals as a function of the discriminator threshold.

Further development of the multiplicity discriminator in terms of schematics and PCB design could still be made in order to improve parameters and overall performance, e.g. to reduce input capacity currently evaluated at 13.6 pF and to integrate the unit with other elements of the ALICE L0 Trigger electronics.

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