The Final Multi-Chip Module of the ATLAS Level-1 Calorimeter Trigger Pre-Processor

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Abstract

The final Pre-Precessor Multi-Chip Module (PPrMCM) of the ATLAS Level-1 Calorimeter Trigger is presented. It consists of a four-layer substrate with plasma-etched vias carrying nine dies from different manufacturers. The task of the system is to receive and digitize analog input signals from individual trigger towers, to perform complex digital signal processing in terms of time and amplitude and to produce two independent output data streams. A real-time stream feeds the subsequent trigger processors for recognizing trigger objects, and the other provides deadtime-free readout of the Pre-Processor information for the events accepted by the entire ATLAS trigger system. The PPrMCM development has recently been finalized after including substantial experience gained with a demonstrator MCM.

I. Introduction

The event selection at the ATLAS experiment requires a fast three level Trigger system for the selection of physics processes of interest. The first trigger level (Level-1 Trigger) is designed to reach an event rate reduction from the 40 MHz LHC bunch-crossing rate down to the first level accept rate of 75 kHz - 100 kHz [1]. The Level-1 Trigger is composed of a number of building blocks - the Calorimeter Trigger, the Muon Trigger and the Central Trigger Processor. The input to the Level-1 Trigger for the calorimeter part is based on reduced granularity. Analog calorimeter signals are summed to 'trigger towers' on a basis of a two dimensional grid with steps of 0.1 in the η and ϕ direction. This is done separately for the Electromagnetic and the Hadronic Calorimeter. It amounts to about 7200 signals which are then transmitted electrically via twisted pair cables to the Level-1 Trigger.

Figure 1 shows a block diagramm of the Calorimeter Trigger. The Pre-Processor at the front-end of the Calorimeter Trigger links the ATLAS calorimeters with the subsequent object finding processors - the Cluster Processor and the Jet/Energy-Sum Processor.

The maximum latency to find a Level-1 trigger decision is 2.0 μs including cable delays. This and the large number of trigger tower signals requires a compact system with fast hard-wired algorithms implemented in application-specific

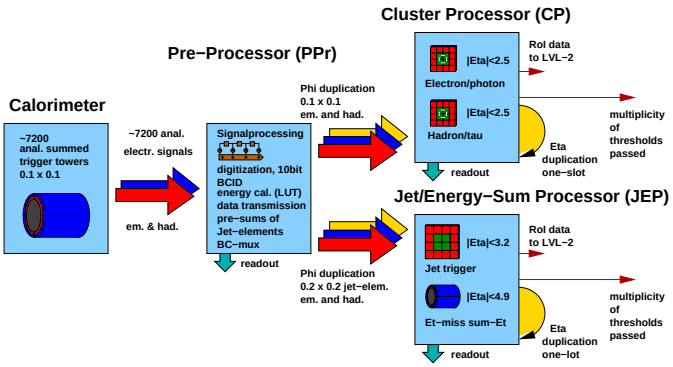

Figure 1: Architecture of the Calorimeter Trigger

integrated circuits (ASICs) and Mulit-Chip Modules (MCMs)

An overview of the tasks of the Pre-Processor system is given in Section II. This is followed by a functional description of the Multi-Chip Module in Section III, which includes a description of the production technique and the layout. The test of the MCM is described in Section IV. The plans for mass production and quality assurance are described in Section V.

II. Tasks Of The Pre-Processor

The reliability of the Pre-Processor is of importance for the running of the ATLAS experiment because all the Level-1 Calorimeter Trigger input data have to go through it. The tasks, that the Pre-Processor system has to perform based on its 7200 analog input signals, can be summarized as follows [2]:

- **Preprocessing:** Provide the trigger processors downstream with digital data containing the transverse energy deposited, identified with the corresponding bunch-crossing. For the Cluster Processor (CP) the granularity is 0.1×0.1 for $|\eta| < 2.5$ and for the Jet/Energy-Sum Processor (JEP) the granularity is 0.2×0.2 for $|\eta| < 4.9$. In both cases the input data are separate for the elctromagnetic and the hadronic calorimeters. The preprocessing is done at 40 MHz with a maximum latency of 15 clock cycles (375 ns).
- **Readout of event data:** Raw trigger data from the Pre-Processor are needed to be able to tell what has caused a trigger and to allow monitoring of the performance of the trigger system.

The basis of the Pre-Processor is a compact 64-channel Pre-Processor Module (PPM) shown in figure 2. All in all the Pre-Processor consists of 128 such modules. This modularity with a high degree of component integration is required to process all trigger tower signals economically in eight electronics crates. Each Pre-Processor Module carries four Analog Input boards for signal conditioning and 16 MCMs. The position of the MCMs on the PPM was optimized in terms of good heat exchange and a minimum of crosstalk between the high-speed MCM output signals and the analog inputs. On the backplane side of the PPM the readout bus connectors

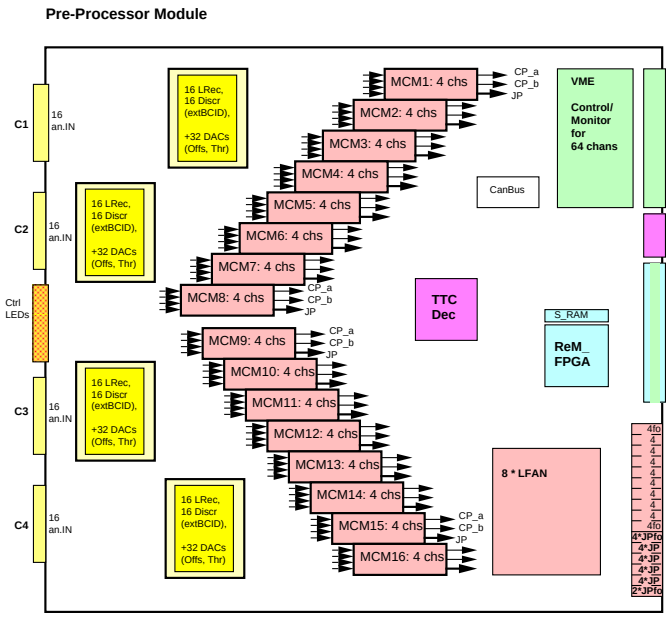

Figure 2: The Pre-Processor Module.

(PipelineBus), the VMEbus connectors and the connectors for the serial LVDS links will be located.

III. Functional Description Of The MCM

In the ATLAS Level-1 Calorimeter Trigger, the MCM combines preprocessing and readout for four trigger tower signals on a single substrate. The electrical boundaries of the MCM package were placed at locations in the processing chain where a minimum number of signals enter and leave the package. The MCM features analog input and digital output, and therefore houses both mixed-signal and purely digital chips. Some of them are commercially available and others are application specific. A Pre-Processor ASIC (PPrASIC) forms the heart of the system and carries out digital signal processing of four trigger towers. In total the MCM contains nine dies: four FADCs, one Pre-Processor ASIC, three LVDS serializers for the digital data transmission to the subsequent processors and a timer chip required for the phase adjustment of the FADC strobes with respect to the analog input signals. The tasks of the Multi-Chip Module are:

- to digitize four analog trigger tower signals at 40 MHz with 10-bit resolution. Digitization at 12-bits is used to extend the effective number of bits;
- to preprocess digital trigger tower data in terms of energy calibration and bunch-crossing timing identification;
- to serialize processed trigger tower data using high-speed LVDS chip-sets;
- to provide deadtime-free readout of four trigger towers;

In order to achieve these, the MCM consists of:

- four 12-bit FADCs manufactured by Analog Devices (AD9042);

- one four-channel PPrASIC, providing readout and preprocessing;
- one timer chip (Phos4) for the phase adjustment of the FADC strobes with respect to the analog input signals;
- three Bus LVDS Serializers, 10-bits at 40 MHz (400 Mbit/s user data rate, 480 MBd including start- and stop bit);

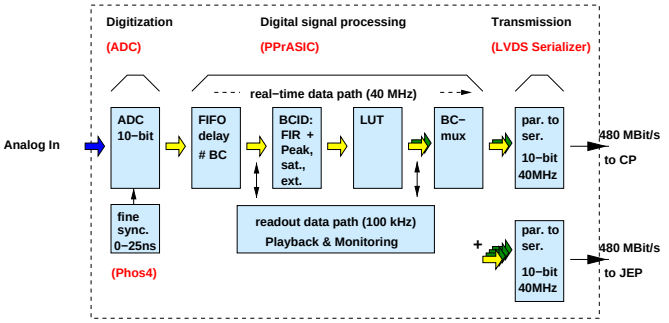

Figure 3: Block diagram of the final MCM

Figure 3 shows the preprocessing of one trigger tower signal. Four such channels are combined on one MCM. The real-time signal processing flows from the left to the right. First, the FADCs digitizes the analog trigger tower signals at 40 MHz with 12-bit resolution (only 10-bits are used, the two lowest significant bits are not connected) in a range of 1 V peak-to-peak around the internal generated 2.4 V reference voltage. Each FADC die generates its own reference voltage. The offset adjustment and scaling from the 2.5 V input signal range to this 1 V range is done by the Analog Input board shown in figure 2. Next, the four 10-bit data buses emanating from the four FADCs are each digitally preprocessed inside the PPrASIC. The PPrASIC output is interfaced to three LVDS Serializer chips. In the case of the data transmission to the Cluster Processor (CP), a bunch-crossing multiplexing scheme (BC-mux) is applied, so that one LVDS Serializer transmits the data from two FADCs. Due to the coarser jet-elements the LVDS Serializer used for data transmission to the Jet/Energy-Sum Processor (JEP) transmits the data from four channels. Figure 3 also shows the second independent output data stream produced by the MCM. This second stream allows pipelined readout of raw trigger input data as well as E_T values after the lookup table (LUT) in order to tell what has caused a trigger and to provide diagnostic information. It allows the monitoring of the performance of the trigger system and the injection of test data for trigger system tests. The function of the readout pipelines in the Pre-Processor is equivalent, but independent of those of the detector readout. The Level-1 Trigger captures its own event data as soon as it has triggered. Two sets of pipeline memories capture the event data in the Pre-Processor. One records the raw FADC data at the Pre-Processor input and one records after the lookup table. Without introducing deadtime to the readout, the readout data path can record data from the pipeline memories up to a Level-1 accept rate of 100 kHz for five time-slices including the BCID result.

A. Design Experience

Considerable design experience has been gained from a demonstrator MCM which has been built, simulated and successfully operated (see [3] for details). This demonstrator MCM was designed with the same feature size (100 μm) as the final MCM and it was fabricated in the same laminated MCM-L process described in the following subsection.

B. MCM production technique

The MCM technology can be classified by its substrate type. It is refered to as an MCM-L (laminated) technology. This technique was chosen to combine small feature sizes with low prices. The design process of the laminated multi-layer structure is based on an industrially-available production technique for high-density printed circuit boards. The process, which is offered by Würth Elektronik [5] is called TWINflex®. It is characterized by its use of plasma etched micro-vias, where plasma is used for 'dry' etching of insulating material (Polyimide). Plasma etching enables precise via contacts between layers with a diameter of 100 μm down to 50 μm.

The body of the MCM is a combination of three flexible Polyimide foils laminated on a rigid copper substrate to form four routing layers. The layer cross-section consists of a *core* foil of 50 μm thickness, which carries 18 μm copper plates on either side. Plasma etching is used for 'buried' via connections to adjacent layers and routing structures are formed in copper using conventional etching techniques. The core foil is surrounded by *outer* foils of 25 μm Polyimide, which are copper plated only on one side. The actual contact through the core foil is accomplished with electroplated copper and after that, the routing structures are formed. The electroplating process increases the track thickness from 18 μm to 25 μm. The application of adhesive accomplishes laminating.

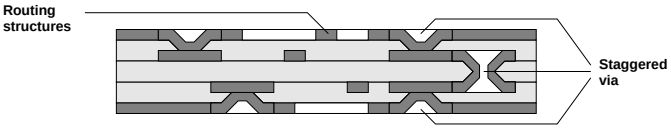

Figure 4: Cross-section of the flexible MCM part after laminating. Staggered vias are used for the connection through all layers.

Figure 4 shows the final laminated and flexible part of the MCM. A combination of three vias (staggered vias) is needed to accomplish a contact from the top to the bottom layer. Finally the flexible part is glued onto a copper substrate of 800 μm thickness.

Due to the high power dissipation of the FADCs (0.6 W for each), for all four FADCs staggered vias were grouped as close as possible to form thermal vias which provide good thermal conductance to the substrate.

Figure 5 shows the final MCM cross-section. Components such as capacitors and resistors are connected to the multi-layer structure using surface-mount technology (SMD). On each end a 60 pin SMD connector from SAMTEC (BTH030) connects the MCM to the Pre-Processor Module. The chips are

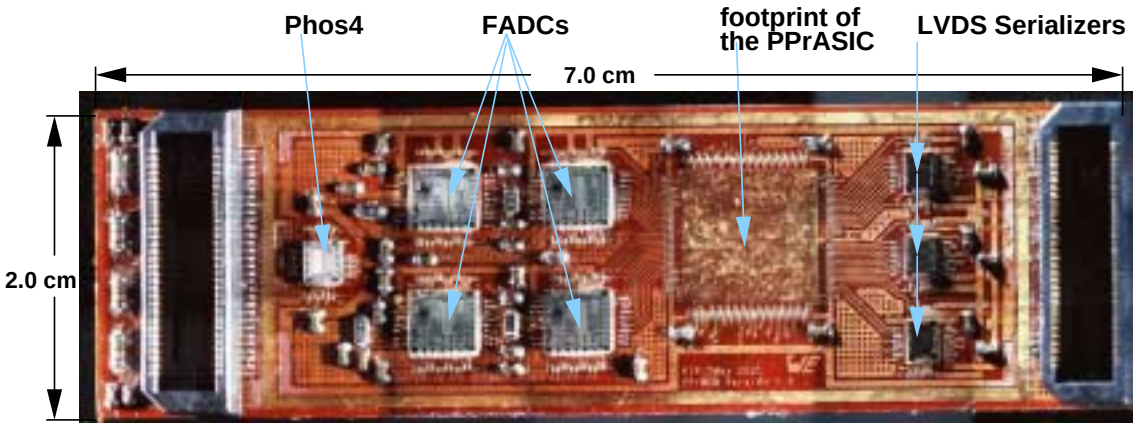

Figure 6: Partly assembled MCM substrate.

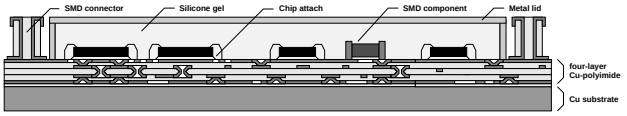

Figure 5: Side view of the hermetically sealed MCM. High-density SMD connectors were used to allow quick replacement upon component failure.

encapsulated with a lid in between the two SMD connectors. The lid will be glued with electrically conducting epoxy to the layer compound. It will act as an EMI-shielding device and it will be filled with a silicone gel to remove atmosphere and to protect the dies from moisture. On the backside of the substrate an 8 mm Al heatsink is glued to it.

C. MCM layout

This section describes the physical layout of the MCM. The following points were considered in the design of the final MCM:

- Analog and digital parts were separated: this applies to power and ground, the signal routing and the placement of the dies.
- Broad power traces ($> 500\mu$m) were used to limit the voltage drop, the width of the other traces are usually only 100μm.
- For each die at least two decoupling capacitors were used.
- The clock distribution was done for each die individually using short traces, this ensures a uniform propagation delay for all clock signals.
- A bond pad size of 150 μm $\times$ 300 μm was used. This size is large enough for wire-bonding, even if one needs to probe at bonding pads during the MCM test or to place a second bond.
- Copper shapes beneath each die are required to connect the die substrate with its voltage potential.
- A solder mask is used to prevent short circuits during soldering of SMD components.
- On the top layer, a cross-hatched ground shape surrounds bonding and SMD pads. This reduces the electromagnetic influence of signals to each other and it stabilizes the ground potential. A cross-hatched shape is needed because drying moisture coming out of the cross-section can destroy the MCM.

A partly assembled MCM is shown in Figure 6 prior to final hermetic encapsulation. The PPrASIC is missing on the picture. The layout has a form factor of 2.0 cm $\times$ 7.0 cm. The total power consumption is 5.2 W. 932 vias were used, the total line length is about 2.5 m.

IV. Functional Test of the MCM

As more than 3200 MCMs have to be tested, an automated test able to say 'well working' or 'defective' within minutes is required. Figure 7 shows the necessary hardware for such a test.

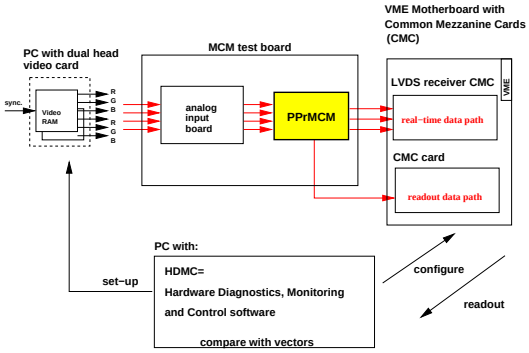

Figure 7: MCM test-setup.

First of all, a dual head video card is used as a signal generator. The advantages of using a video card as a signal generator are that a video card is very cheap, very fast and arbitrary analog output signals can be programmed. A dual head video card has six analog outputs. Out of these six outputs four are chosen to provide the analog stimulus signals

for the test. The signals are conditioned by the Analog Input board, the same board which is used on the Pre-Processor Module. The conditioned signals are received by the MCM to be tested. Both, the MCM and the Analog Input board are plugged on a test board. The output of the real-time data path is received by a LVDS receiver CMC card. The data of the readout path are received by a Xilinx FPGA, located on a second CMC card. This CMC card also hosts a large SRAM which buffers the data of the readout path as well as the data of the real-time path which is transmitted from the LVDS receiver CMC card to this CMC card. The memory can be read out by VME and thus data can be transmitted to a PC.

The test will be set-up and analysed by the Hardware Diagnostics, Monitoring and Control software (HDMC) which was developed by the ATLAS group of Heidelberg. The output of the MCM can now be compared with expected results gained from a mixed signal simulation of the full MCM including the chip logic. Because of the analog part of the MCM the check will have boundaries within which the result can be seen as correct.

V. Mass Production and Quality Assurance

The development and design of the MCM was done by the University of Heidelberg, whereas the final production of 3200 MCMs needs to be done in cooperation with external companies. The four-layer MCM substrate including the 800 μm copper carrier is done by Würth Elektronik [5]. The mounting of dies and SMD components, wire-bonding and encapsulation will be done by Hasec [4].

The following list provides the sequence for mass production and quality assurance:

1 Production: Substrate layer compound

2 Test : Electrical test

3 Test : Test bonding

4 Assembly : Silk-screen printing of solder paste

5 Assembly : Placement of SMD components

6 Assembly : SMD reflow soldering

7 Assembly : Chip mounting

8 Assembly : Ultrasonic wire-bonding

9 Test : MCM test with the test system shown in section IV

10 Assembly : Repair of defective MCMs

11 Assembly : Encapsulation, lid and silicone gel

12 Test : Performance test on the Pre-Processor Module

VI. Conclusions

The design of the final MCM benefited from the design experience gained by a demonstrator MCM. Compared to this demonstrator MCM the final MCM presented here is less demanding in terms of power, temperature and link speed and hence it can achieve an improved reliability. An extensive test will be done in the near future when the so called 'slice test' starts. It is planned to assemble the whole preprocessing chain with the subsequent object-finding processors for several hundred analog trigger tower signals. This test will show if the final MCM meets all the requirements.

VII. References

[1] ATLAS Level-1 Trigger Group
ATLAS First-Level Trigger Technical Design Report
ATLAS TDR-12, CERN/LHCC/98-14, CERN, Geneva 24 June 1998
http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html

[2] Pre-Processor Module
Specification of the Pre-Processor Module (PPM) for the ATLAS Level-1 Calorimeter Trigger
The ATLAS Heidelberg Group
http://wwwasic.kip.uni-heidelberg.de/atlas/docs/modules.html

[3] Pfeiffer, U.
A Compact Pre-Processor System for the ATLAS Level-1 Calorimeter Trigger
PhD Thesis, Institut für Hochenergiephysik der Universität Heidelberg, Germany 19 October 1999
http://wwwasic.kip.uni-heidelberg.de/atlas/docs.html

[4] HASEC-Elektronik.
http://www.hasec.de

[5] Würth Elektronik
http://www.wuerth-elektronik.de