# New building blocks for the ALICE SDD readout and detector control system in a commercial 0.25µm CMOS technology

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*Abstract*

This paper describes building blocks designed for the readout and detector control systems of the Silicon Drift Detectors (SDDs) of ALICE. In particular, the paper focuses on a low−dropout regulator, a charge redistribution ADC and a current steering DAC. All the parts have been developed in a commercial 0.25µm CMOS technology, using radiation tolerant layout practices.

## I. Introduction

Silicon Drift Detectors will be used in the third and fourth layer of the Inner Tracking System of the ALICE experiment [1]. The specifications and the implementation of the electronics for the SDDs are described in detail in [2], [3], [4] and will not be covered here. For the purpose of this work it is sufficient to remember that the SDD system requires the development of four full−custom ASICs, which are used both for data processing and control tasks. Two of these chips are purely digital and two are mixed−mode designs. The building blocks presented in this paper will be integrated in the mixed−mode circuits.

The more complex mixed−signal component is the front−end chip (named PASCAL), which performs the amplification, filtering and analogue−to−digital conversion of the detector signals. In its final implementation, the ASIC host 64 amplifiers, each coupled with a row of a switched capacitor array (SCA), having 256 cells. When a trigger signal is received, 32 on board ADCs convert the analogue data stored in the pipeline to a 10 bit digital code. A single ADC digitises the content of two adjacent rows of the SCA. The converter, described in detail in [5], is based on the successive approximation technique [6], which offers a very good trade−off between speed and power consumption. Due to the severe space constraints on the front−end board, the reference voltage for the ADCs must be provided on chip. The generation of this reference is an issue, because the voltage source will be heavily loaded by the ADCs, which operate in parallel. For these reasons, a dedicate low dropout regulator had to be developed. The design of this block as well as the first results of the experimental measurements are discussed in section II.

The chip for the Detector Control System (DCS) performs the monitoring of vital parameters of the system and the control of some critical voltages and currents. For instance, this chip is used to measure the temperature of the electronics board. Additionally, it has to generate the amplitude−controlled signal which is needed to trigger the calibration circuitry of the detector. Therefore, an ADC and a DAC are the basic elements of the DCS ASIC. These circuits need to provide a medium resolution (8 bits), while minimising area and power consumption. They are described in section III and in section IV of this paper, respectively.

## II. The low dropout regulator

The low dropout regulator provides a stable DC voltage of 1.9V that is needed by the ADCs of the front−end chip. Depicted in fig. 1, the circuit uses a linear scheme, [7] whose key elements are the error amplifier $A_1$, the pass transistor $P_0$ and the resistive feedback network formed by $R_1$ and $R_2$. All these components are integrated on chip. The output voltage is derived from the reference voltage VBG, provided by a bandgap circuit.

The capacitor $C_0$ serves to filter the current spikes and provides the frequency compensation of the loop. Given the high value required for $C_0$ (1µF), an external discrete component must be used. In fact, it is very important to assure that the regulator works in all conditions with an adequate phase margin. The value chosen for $C_0$ guarantees that the feedback loop has always a phase margin of 76 degrees.

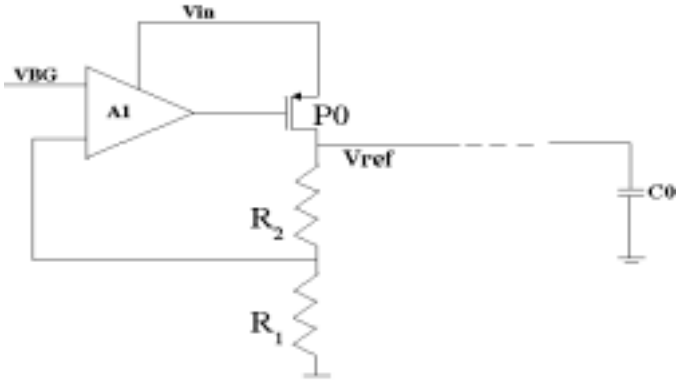


*Figure 1 : LDO simplified scheme.*

The LDO can deliver to the load a maximum current of 100mA. The static power consumption of the circuit is 2.5mW and it occupies an area of 230 x 150 $\mu m^2$ (excluding the bandgap reference, which will be shared by several circuits on the front−end chip.)

In order to check the functionality of the device before its integration in the final version of the front−end ASIC, a dedicated test chip has been produced and measured. The test results show a good agreement with the computer simulations. The circuit provides the required reference voltage with an overall accuracy of 1%. As an example of the performance of the circuit, Figure 2 reports the plot obtained for the load regulation. The current driven by the load is changed from zero to the maximum value of 100mA. The maximum change in the output voltage is 13 mV, resulting in a load regulation figure (defined as $\Delta V_0/\Delta I_0$) of 0.13 Ω.

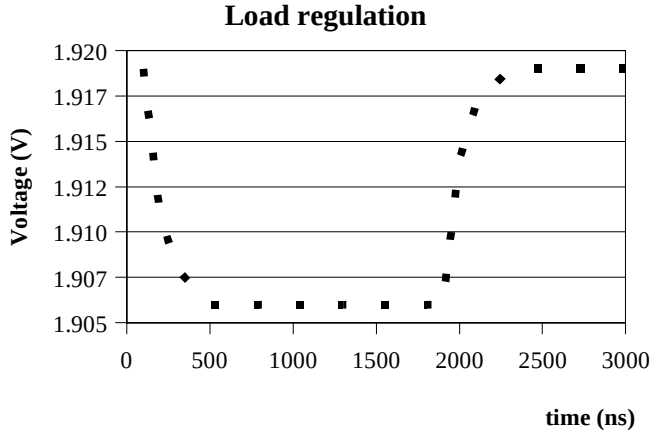


*Figure 2 : LDO load regulation performance*

The line regulation has been checked for Vdd ranging from 2.2 to 2.7 V, corresponding to the maximum power supply variation acceptable for the front−end chip. In this interval, the output voltage changes by 1mV giving a line regulation ($\Delta V_0/\Delta V_i$) of 0.002. The measured noise at the output of the LDO is 250μV rms, but the accuracy of this measurement is limited by the experimental set−up.

## III. The Analogue to Digital Converter

The ADC is an evolution of the converter embedded in the front−end chip. In order to profit as much as possible from existing blocks, the same successive approximation topology used in PASCAL has been chosen. The main modification occurs in the DAC, in which the resolution has been traded for area. Figure 3 shows the block diagram of a typical implementation of a 8 bit charge redistribution ADC. The two basic elements of the circuit are a voltage comparator and a DAC made of binary weighted capacitors.

The conversion is performed in two steps:

- In the acquisition phase, all the capacitors are connected in parallel and are used to sample the input signal.
- In the redistribution phase, the capacitors are used individually to generate binary fractions of the reference voltage, which are compared with the sample previously stored.

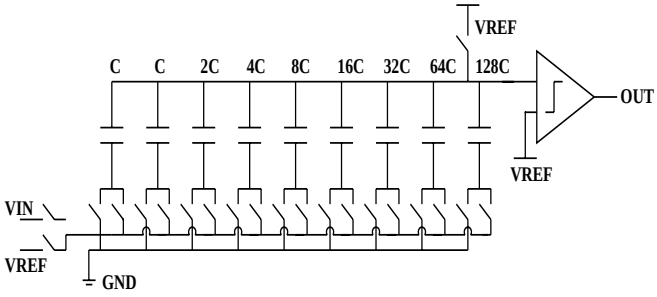


*Figure 3 : Schematic of a generic 8 bit ADC*

The conversion algorithm is described in detail in [6]. For the purpose of our discussion, it is sufficient to observe that if the DAC is implemented exactly with the scheme of Figure 3, its area doubles for every extra bit of resolution required. For instance, an 8 bit DAC occupies twice the area needed by a 7 bit one.

In order to reduce the surface of the DAC, the scheme of Figure 4 has been used. In this approach, the DAC has been splitted in two blocks, each with a 5 bit capability.

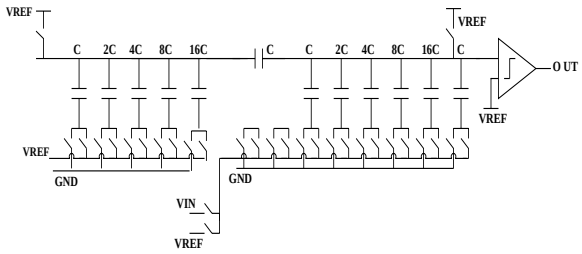


*Figure 4 : Schematic of the implemented ADC with segmented DAC*

The first DAC samples also the input signal and is capacitively coupled to the second DAC, which is used only during the redistribution phase.

In this way, two advantages are achieved:

- The total area is equivalent to the area of a 6 bit DAC, which is four times smaller than the area of a direct 8 bit DAC.
- Since the sampling is performed only by the main DAC, the input capacitance of the ADC is reduced by a factor eight with respect a straightforward 8 bit design.

The matching between the capacitors is critical to obtain a good linearity in the ADC. To improve the matching, in the layout only a fundamental cell is used and the bigger capacitors are built by connecting a suitable number of elementary cells in parallel. Actually, the structure of Figure

4 is more sensitive than the architecture of Figure 3 to the effect of random mismatches. This point can be understood by noting that in the ADC of Figure 4 the capacitor which determines the MSB is formed by 16 unit elements, whereas in Figure 3 it is composed by 128 individual cells. In the latter case, the MSB capacitor will be more precise, because it uses more elements in parallel and the random error affecting each one tend to average out. For this reason, the ADC is built using two 5 bit DACs instead of two 4 bit DACs, which in principle would be sufficient to get a total 8 bit resolution.

It must also be observed that the circuit of Figure 3 could be used to implement a 10 bit ADC. However, for the matching reasons mentioned above this resolution can not be assured if the individual capacitor is implemented with the minimum size allowed by the technology. In our application a 10 bit resolution is not required, whereas the area of the circuit is important. Therefore, the minimum size capacitance has been used, targeting 8 bit performance. Nevertheless, two extra bits have been made available for test purposes.

The layout of the circuit has an area of 300 x 800 $\mu m^2$, which is about 60% of what would be required by the direct implementation of Figure 3.

A test chip containing three identical converters has been designed and fabricated. The ADC is tested by sending to the circuit a sinusoidal input signal and reading the digital output codes with a logic state analyser. The data are the processed with a dedicated software to calculate the DNL, the INL, and the FFT. In the measurements, the ADC is operated with a full scale range of 1V, which results in a LSB of 4mV.

During the test, the circuit is running with a clock of 40MHz. Since two clock cycles are left to sample the input signal and to compensate the offset in the comparator [5], 10 clock periods are required for a complete 8 bit conversion. The sampling frequency is hence 4Msample/sec. The circuit is powered with a single rail power supply of 2.5V and dissipates 3mW.

Figure 5 show the result of a typical FFT that is obtained in the measurements.

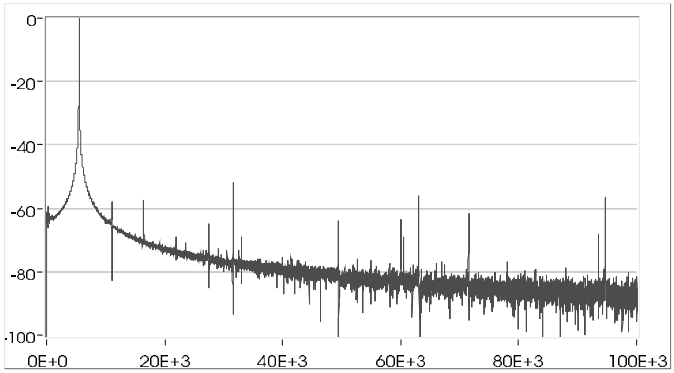


*Figure 5 : FFT measured for the ADC.*

As it can be seen from the figure, the second harmonic is well below 48dB and the ADC has a very low distortion.

The converter has a maximum DNL of 0.8 LSB, which is sufficient to guarantee a 8 bit resolution without missing codes. To give a more intuitive view of the performance of the circuit, Figure 6 shows the result of the conversion of a full scale ramp.

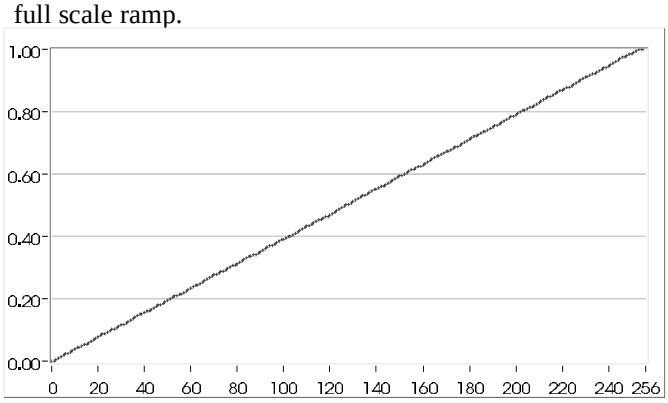


*Figure 6 : Digitization of a full scale ramp.*

## IV. The digital to analogue converter

The 8 bit DAC is the other analogue building blocks for the DCS chip. It must be observed that switched capacitor DAC used in the ADC is very compact, but it suffers from a number of drawbacks. These drawbacks make it inadequate to work as a stand−alone component. For instance, the parasitic capacitance on the top plate attenuates the voltage steps generated by the DAC. This and other phenomena are of minor concern in an ADC, since they affect in the same way both the signal and the partitions of the reference voltage that are used in the conversion. However, they can determine severe limitations when the DAC is used just to convert a digital code to an analogue level. For these reasons it has been necessary to develop a new circuit, using a different approach.

The circuit is based on a current steering configuration and is made of an array of current sources and a digital control logic. In order to improve as much as possible the matching between the sources and hence the linearity, a fully thermometric segmentation has been chosen. Therefore, the DAC is formed by 256 identical cells, which are organised in a 16x16 matrix.

The schematic of the elementary bit cell is shown in Figure 7. The cell is essentially a cascode current mirror, which copies a reference current. The sizes of the transistor are dictated by the need of having an adequate area and overdrive voltage, in order to get an appropriate matching. If the cell is selected by the control logic, the switch driven by sel_b is closed and the current is directed towards the output node. At the output node, all the currents generated by the individual mirrors are summed and converted to a voltage. The current−to−voltage conversion can be carried−out either by a simple resistor or by a transimpedance amplifier. Both

options are available in the DAC.

Each elementary cell is biased with a tail current of 5µA, resulting in a static power consumption 3mW for the whole analogue part of the DAC.

The circuit has been optimised to reach a conversion speed of at least 50Msamples/sec.

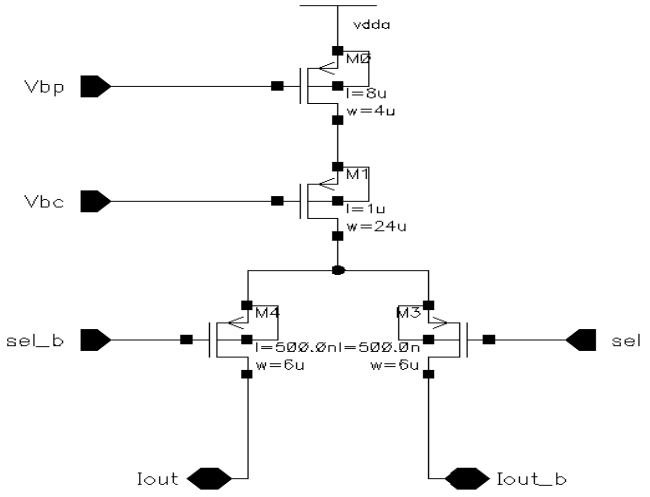


*Figure 7 : Schematic of the unit cell of the DAC.*

Shown if Figure 7, the layout of the complete DAC has an area of 1 x 0.6 $mm^2$. The test chip is in production and no experimental result is available at the time of writing.

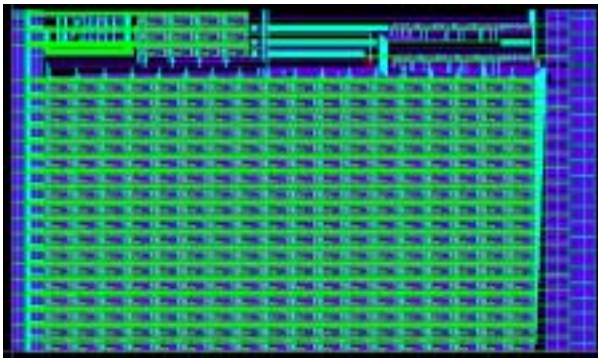

*Figure 8 : Layout of the full DAC*

## V. Conclusions

The front−end and detector control electronics of the SDD of ALICE requires complex analogue building blocks. The most critical circuits have been prototyped, in order to check their functionality before their integration in the final ASICs. These circuits are a low dropout regulators, an ADC and a DAC with moderate resolution (8 bits) but reduced area.

The low dropout regulator is needed to generate on board the reference voltage for the ADC of the front−end chip. The circuit integrates all the critical parts except the filtering capacitor and has shown characteristics which are adequate for the application. The output voltage change by 1mV for a change of 0.5V in the power supply. The regulator is able to provide a maximum current of 100mA with an output voltage drop of 13mV. The noise is less than 200µV rms.

The analogue to digital converter uses a segmented architecture in the DAC, in order to minimise the area as much as possible. The area of the ADC is 0.24$mm^2$. The circuit has a resolution of 8 bits over a full scale range of 1V and operate at a speed of 4Msamples/sec, dissipating 3mV from a 2.5V supply.

The last building block that has been developed is a current steering digital to analogue converter. This circuit is still in production and it will be tested in the forthcoming months.

All the three designs discussed in this paper have been implemented in a 0.25µm CMOS technology, using enclosed layout transistors and guardrings to prevent the damage from ionising radiation.

## VI. References


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