Single Event Upset Tests of Commercial FPGA for Space Applications[1]

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Abstract

Space based systems are looking more and more to the benefits from high performance, reconfigurable computing systems and Commercial Of The Shelf components (COTS). One critical reliability concern is the behaviour of the complex integrated circuits in a radiation environment. Field programmable gate arrays (FPGAs) are well suited for the small volumes in space applications. This type of products are driven by the commercial sector, so devices intended for the space environment must be adapted from commercial product. Heavy ion characterisation has been performed on several FPGA types and technologies to evaluate the on-orbit radiation performance. As the geometry keeps shrinking, the relative importance of various radiation effects may change. Investigation of radiation effects on each technology generation is found to be necessary. This paper presents methodologies and results of radiation tests performed on commercial FPGAs for space applications. Mitigation of Single Event Upsets will be discussed.

I. INTRODUCTION

Programmable logic has advantages over ASIC designs for the space community in the faster and cheaper prototyping, and reduced lead-time before flight. FPGAs based on antifuse technology are frequently used in space applications. Reprogrammable logic would offer additional benefit of allowing on-orbit design changes. From Single Event Upsets point of view the antifuse technology has offered better control and reliability. However, mitigation methods for reprogrammable logic technologies are under constant development. This paper discusses the Heavy Ion SEU testing of several Actel antifuse-based FPGAs and Xilinx *Virtex* FPGA.

II. RADIATION TEST SYSTEM

A. Test Board

The test system developed by Saab Ericsson Space consist of two boards, one Controller board managing the test sequence and the serial interface to the PC and one DUT-board housing two Devices Under Test (DUT). A schematic drawing is given in Fig.3.

The Controller board tests one DUT at a time using a "virtual golden chip" test method. The principal of the measuring technique is to compare each output from the DUT with the correct data stored in SRAM's. The general procedure for the tests are to load data into the devices under test, pause for a pre-set time, read data out, and analyse the errors for various error type signatures. New data are loaded into the DUT at the same time as old are read out. When an error is detected (when outputs do not match), the state of all outputs and position in cycle of the failing shift register will be temporarily stored in FIFOs. Data in the FIFOs is continually send to a PC through a RS232 serial interface. After each test run the data are analysed and stored in a database by the controlling PC. For each DUT, errors can be traced down to the logic module, logic value and position.

B. Test Facility

Heavy ion tests were performed at the CYClotron of LOuvain la NEuve (CYCLONE), Belgium. This accelerator can cover an energy range of 0.6 to 27.5 MeV/AMU for heavy ions produced in a double stage ECR source. The use of an ECR source allow the acceleration of an ion "cocktail" composed of ions with very close mass over charge ratio. The preferred ion is selected by fine-tuning of the magnetic field or a slight change of the RF frequency. Within the same cocktail it takes only a few minutes to change ion species.

The facility provides beam diagnostic and control with continuous monitoring of beam fluence and flux via plastic scintillators. The irradiations are performed in a large vacuum chamber with the test board mounted on a movable frame. Normally each device is tested with a variety of atomic species up to a fluence of 1e+6- 1e+7 ions/cm2, depending on the cross section for the device under test.

[1] This work performed by Saab Ericsson Space, is supported by the European space Agency

III. ANTIFUSE FPGA TECHNOLOGY

FPGA's from Actel Corporation are widely used in Aerospace applications. The company has been providing products to the stringent space requirements for several years. During the last years several new products have been introduced with the aim of having improved radiation resistance and logic circuit density.

The company uses several different manufacturers for the wafer production. Only wafers manufactured by Matshushita (MEC) are used in the products for space. The same products sold under the same electrical specification are likely manufactured in several fabs. Some of these products have been tested for total dose and found only good for a few krad(Si) total dose. Over the years there have been many SEU tests using heavy ions performed on Actel products, both to determine the SEU probability for the user logic's as well as determining effects of heavy ions on the antifuses. [1] Results obtained by Saab Ericsson Space are presented below.

IV. RESULTS ON ANTIFUSE FPGA

All results presented below have been tested with the same test method and test board described above.

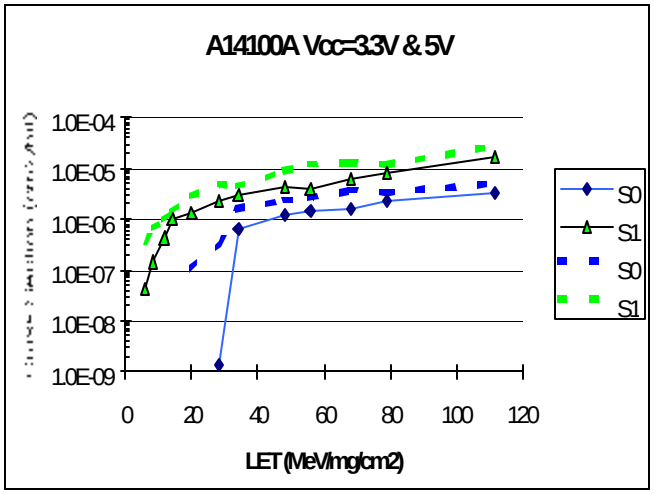

Figure 1 Heavy ion data on Actel A14100A S-module for 5V and 3.3V biasing conditions. Flip from logic "0" to logic "1" is noted S0. The opposite is noted S1. The dashed curves are showing the 3.3V data for the two SEU modes.

A. Actel A14100A

This FPGA is manufactured by Matshushita (MEC) in antifuse ONO gate 0.8µm two-level metal CMOS technology with 1153 logic modules. The SEU behaviour of this device is very typical for Actel devices. Biasing at 3.3V give a higher SEU probability. Actel has a large asymmetry in the flip-flop sensitivity between flip from logic "zero" to logic "one" compared to the reverse. This device type has been on the market for several years and according to Actel there are at the moment no plans to take it out of the market. This device type has been designed in on many spacecraft's, but only a few have been launched so far.

B. Actel RT54SX16

This FPGA is manufactured by Matshushita (MEC) in antifuse metal-to-metal gate 0.6µm 3-metal CMOS technology. This device type exists in a 32 kgate version as well. However, the device types became obsolete before it came out on the market because MEC decided to close down the 0.6µm line.

The SEU behaviour of this device is very similar to A14100A. The large asymmetry in the flip-flop sensitivity between flip from logic "zero" to logic "one" compared to the reverse could be observed here as well. The total dose tolerance for this type is around 50 krad(Si) compared to that of A14100A which only around 10-15 krad(Si). There are large differences in total dose tolerance between different production lots of these types.

Critical functions in space applications must be triple module redundant to mitigate for SEU. This consumes large portion of the devices and the cost per bit becomes quite expensive.

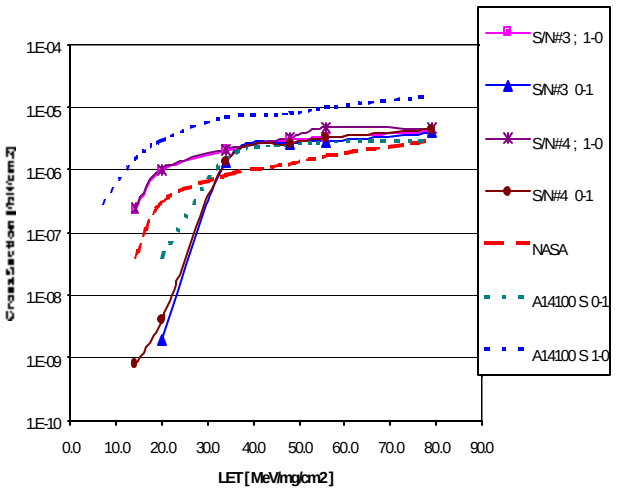

Figure 2. Heavy ion data on Actel RT54SX16 R-module. The data for A14100A are shown as dashed curves.

V. SRAM FPGA TECHNOLOGY

The Xilinx Virtex FPGA is an SRAM based device that supports a wide range of configurable gates from 50k to 1M. It is fabricated on thin-epitaxial silicon wafers using the commercial mask set and the Xilinx 0.25µ CMOS process with 5 metal layers. SEU risks dominate in the use of this technology for most applications. In particular, the reprogrammable nature of the device presents a new sensitivity due to the configuration bitstream. The function of the device is determined when the bitstream is downloaded to the device. Changing the bitstream changes the design's function. While this provides the benefits of adaptability, it is also an upset risk. A device configuration upset may result in a functional upset. User logic can also upset in the same fashion seen in fixed logic devices. These two upset domains are referred to as configuration upsets and user-logic upsets. Two features of the *Virtex* architecture can help overcome upset problems. The first is that the configuration bitstream can be read back from the part while in operation, allowing continuous monitoring for an upset in the configuration and the part supports partial reconfiguration, which allows for real-time SEU correction. Secondly, Triple Module Redundancy (TMR) can be implemented in order to filter out SEU effects.

VI. TEST METHODS FOR SRAM FPGA

A. SRAM Bitstream Readback

On the test board described above, a configuration controller chip on the DUT-board is controlling a PROM and configuration ports of the DUT. A program command can be sent to the DUT, which clears its configuration memory and starts an automatic re-configuration of the DUT from the PROM During the test of the DUT the configuration controller is continuously scrubbing the DUT configuration memory with new configuration data from the PROM's. A schematic drawing of the test board is shown in Fig 3

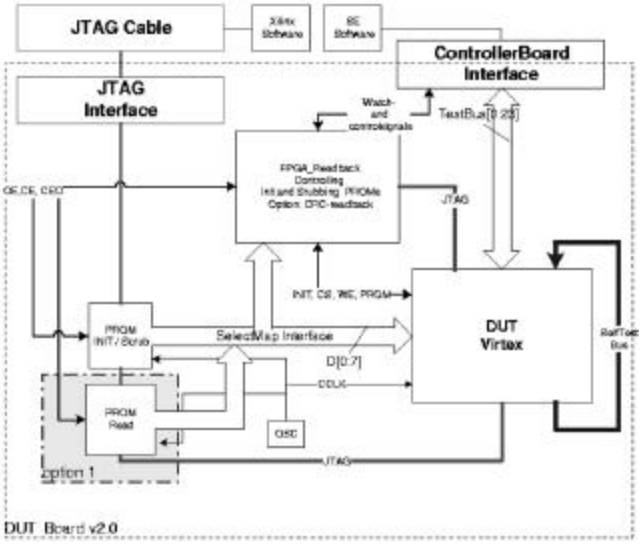

Figure 3 Schematic drawing of DUT board with configuration interface for the Virtex device

All data from the PROM's to the DUT is transferred through the parallel SelectMAP interface, which supports the partial configuration feature making it possible to continuously scrub the device with new configuration data during operation.

B. Error Separation

Errors could originate from SEU in registers of the device, SEU in the configuration data causing functional errors in parts of the device and from errors in control registers of the device causing global functional errors. The analysed data errors are separated into three different domains, SEU in registers, SEU in configuration data, and SEU in device control registers.

SEU in the register is corrected with the new data loaded into the DUT. The error will not last in next test cycle.

SEU in the configuration data would be permanent until the device is scrubbed with new configuration data. The SEU gives an error in only part of the device and could, for example, corrupt the function of one of the shift registers in the DUT. This means that the shift register will be out of function until the configuration data is corrected with new data.

The control register "POR" controls the initialisation sequence of the device when it powers up. An SEU in this register could change state of the whole device by initiating a complete clearing of the configuration memory. This type of error is detected when all shift registers go out of function at the same time.

C. DUT Designs

Two design methods were tested for comparison, TMR and non-TMR designs. Both designs have the same basic functionality. The TMR version uses the Triple Module Redundancy design techniques that Xilinx recommends for use with the Virtex FPGA [3]. The non-TMR design is a standard design used for Actel antifuse as well.

The non-TMR design, schematically shown in figure 4, implements into the device 14, 144 stage, pipeline shift register and a small self test circuit.

The TMR design, schematically shown in figure 5, implements a functionally equivalent circuit as the non-TMR design but with full internal triple redundancy. The outputs of the TMR design use triple tri-state drivers to filter data errors from the output.

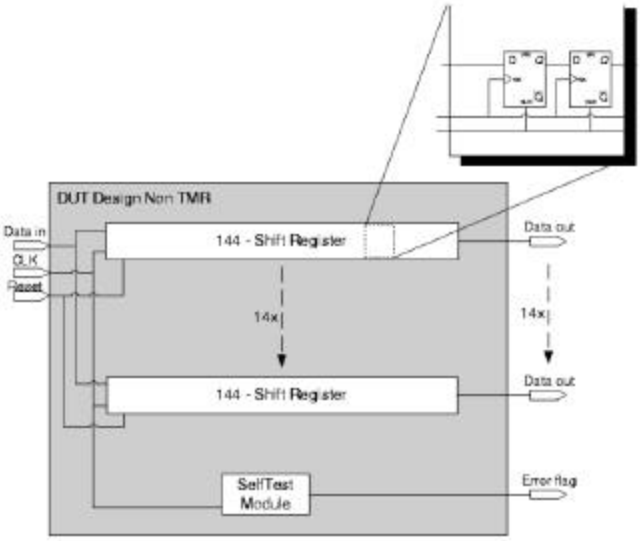

Figure 4 Schematic drawing of non-TMR DUT design

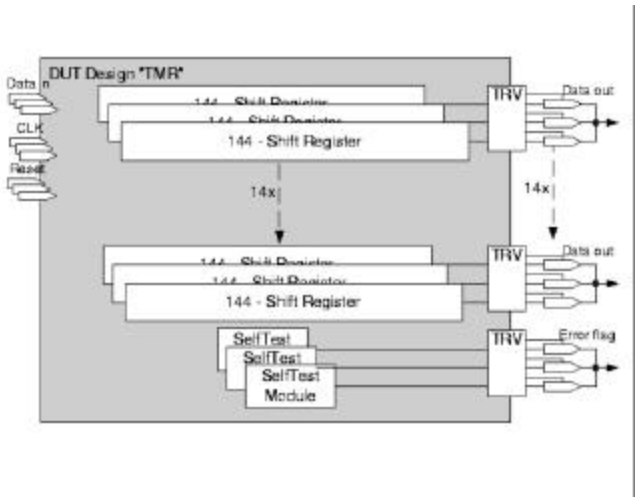

Figure 5 Schematic drawing of TMR DUT design

D. Other Test Considerations

An SEU in configuration data causing a functional error is corrected when new configuration data is written to the DUT. To be able to detect all of these errors the DUT must be continuously tested. Since the DUT is paused in our tests, we will not see all of these errors. Therefor we have to estimate the fraction of errors that we detect (Detection factor).

Two different pause times (time where DUT is not clocked between read/write of data) are used during the tests, 223ms and 4ms. Testing the non-TMR design mostly used the long pause time since the flow of error data was too high.

The test system allows selecting the scrub time between 10,38ms / 22,93ms and 166ms. The longer scrubbing rates were only used in the first test runs for calibration purposes.

VII. SRAM TEST RESULTS

Each test was performed with a variety of atomic species up to a fluence of 1e+6 ions/cm2, or until either one of the shift registers was permanently disabled by the "Persistent" error or all 14 shift registers were eliminated by the "SEFI" error. With this error in a shift register no data came out and the registers couldn't be tested. The fluence is calculated from the total fluence of the test and the mean value until each Persistent or SEFI type error. In this way the fluence of when the device is actually tested is achieved.

A. Configuration induced Error types

Errors that are caused by SEU in the configuration are quantified by observing the following signatures in the test data: The results are shown in figure 6

1) Routing

An SEU in the configuration logic (routing bits and lookup tables) may cause errors in the configured function of the operational device. This gives errors from the shift registers that are permanent until next time the device is scrubbed with new configuration data.

2) Persistent

A persistent error is a permanent error that is not corrected with new configuration data. The device needs to be reset to correct this error. This is the result of SEU in "week keeper" circuits used in the Virtex architecture when logical constants are implied in the configured design such as unused clock enable signals for registers.

3) SelfTest

SelfTest errors are of same type as the routing type, but instead of interrupting a shift register it interrupts the function of the SelfTest module.

4) SEFI type

Function of the whole device is interrupted in one hit and all shift register data is lost. The device requires a reset and complete reconfiguration for correction.

These errors are tested in a dynamic way, but due to limitations of the test system the device is rested between clocking of data. Since the device is continuously scrubbed with new configuration data, there will be a significant amount of errors of the routing and SelfTest data not seen

at read out (corrected before read out). The detection factor correlates the results for this.

5) Non-TMR design

At a LET of 2.97 MeV/mg/cm^2 each configuration type error was observed. Cross-sections are presented in Fig. 6. The presented data for all configuration type errors are correlated with an estimated "detection factor". With a scrub time of 10 ms and a pause time of 4 ms the detection factor is estimated to be 0.6 and with the longer pause time of 223 ms, it is estimated to be 0.05.

The cross section is specific for this design. To predict cross section for a 100% utilised device you must multiply these cross sections with the utilisation factor for this design (about 32% for the routing errors and maybe 5% for the SelfTest module).

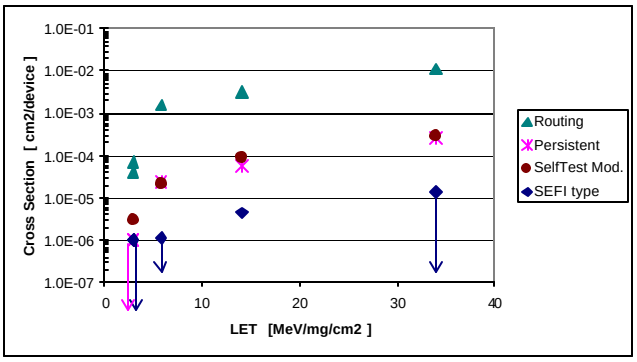

Figure 6 Configuration errors for non-TMR Design. The cross sections are per device and are specific for this design. For the non-TMR design one SEFI type error was recorded, at a LET of 14.1 MeV/mg/cm^2. This is likely due to the very low fluence required for the test to finish. Arrows indicate test without any errors.

6) TMR design

The SEFI type error was the only observable error type. The Persistent error is not observed. The SEFI was observed at a LET of 5.85 MeV/mg/cm2. This demonstrated that the TMR design method effectively eliminated all non-SEFI configuration induced errors.

The "SEFI type" error is believed to be an SEU in the POR control register, clearing the whole device from configuration data. All I/Os are 3-stated in this state and this was detected at the read out data, which slowly went from read high state to read low state after some test cycles.

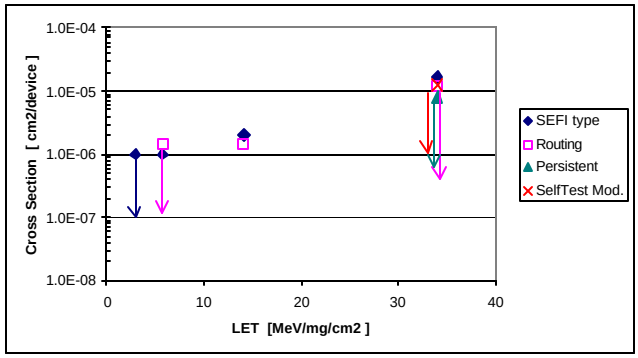

Figure 7 Configuration errors for TMR Design. Except for SEFI errors only one "routing" error was recorded at a LET of 14.1 MeV/mg/cm^2. Arrows indicate test without any upsets.

In one test run a "Routing" error was observed. The flux was ~1333 ions/cm2/s and the device were scrubbed with new configuration data every 10,38ms. This gives a flux/scrub-cycle ratio of 13ions/cm2/scrub.

Xilinx has reported that the number of accumulated configuration bit upsets to cause a functional failure in a TMR design ranges between 2 and 30 bits. It is therefore possible that enough errors in the configuration logic were allowed to accumulate before the next scrub cycle to cause the error. Therefore, the observed errors are most likely an artefact of the flux/scrub-cycle ratio.

B. Register Error Types

These errors are tested in a static fashion. Data is clocked into the shift registers, held for a pre-set time, and then clocked out for comparison. The procedure is repeated constantly during the test run. The data are analysed for single bit errors and categorised into the following error types:

FF(0-1) Read '1' from flip-flop registers when '0' is expected.

FF(1-0) Read '0' from flip-flop registers when '1' is expected.

FF A summation of all FF errors (above) read from the shift registers.

DataSwap This was an error type that had two errors in registers next to each other in the register chain. First a '0' was read when '1' was expected and in the next register a '1' is read when a '0' was expected. This error was isolated for two registers in the whole chain of 144 registers and didn't occur again in the next test cycle.

One possible explanation for this error type is that a routing bit error was being corrected just as test data was being read out for comparison.

1) Non-TMR design

FF errors were observed at a LET greater than 2.97 MeV/mg/cm2 with a saturation cross-section of ~1e-6cm2.

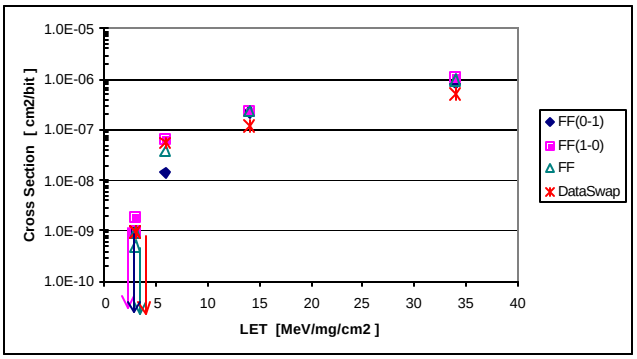

Figure 8 Register errors for non-TMR Design. Arrows indicate test without any upsets.

2) TMR design

Only one FF error was observed at a LET 14.1 MeV/mg/cm2 with an estimated cross-section of ~5e-10cm2. No other FF errors were recorded in absence of a SEFI type error. It is considered that this error is the result of the flux/scrub-cycle ratio as previously mentioned.

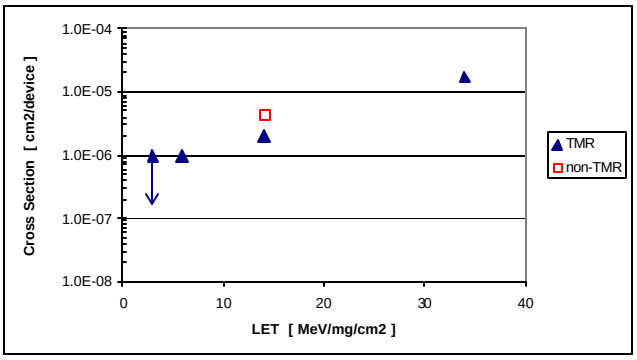

Figure 10 SEFI errors for non-TMR and TMR design. The non-TMR tests were performed to less fluence than the TMR, therefor less SEFI errors have been observed for non-TMR design. In principal the SEFI error cross section should be the same for the two designs. With the assumption the control registers have the same heavy ion sensitivity as the user registers. The number of fatal failure control bits of the device seems to be around ten. The LET threshold of the SEFI errors would with this assumption be around 5 MeV/mg/cm^2.

VIII PROTON INDUCED SEU

The main mechanism in energy loss leading to single event phenomena is due to inelastic collisions between incident protons and atoms in the substrate. The recoiling nucleus will thus be the particle that causes the SEU. The final mechanism for proton induced SEU is therefore very similar to that envisaged for heavy ions.

In Fig 11 below are proton data from Actel A14100A and Xilinx Virtex shown. The cross sections for proton SEU are a factor 10^{-8} lower than those observed for heavy ions. The low threshold observed for Xilinx manifest itself in the sensitivity for low energetic protons. For A14100A, is likely only the flip of logic "0" to logic "1" that is observed in the proton SEU. Circuits having a threshold higher than LET= 15 MeV/mg/cm2 are not sensitive to proton upset.

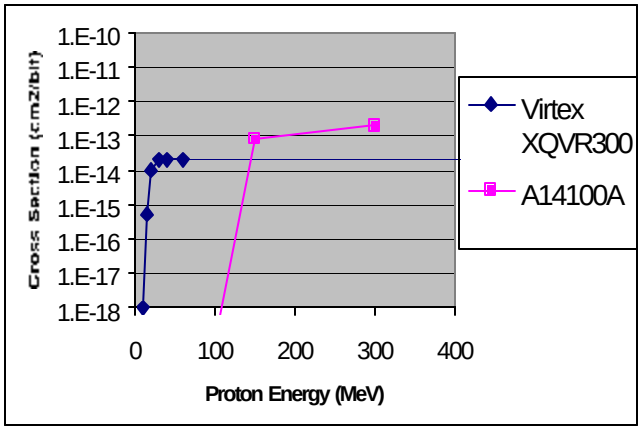

Fig 11 Proton upsets as a function of proton Energy for Actel A14100A and Xilinx Virtex QRV300. For Actel A14100A, no proton upsets have been observed at energies below 150 MeV. The results for Xilinx is taken from Ref [3]

IX SINGLE EVENT TRANSIENTS

In addition to "conventional" SEUs, charge particles can also induce transients in combinatorial logic, in global clock lines and in global control lines. These single event transients (SET) have only minor effects on technologies around 0.8-0.5 µm since the speed of these circuits are insufficient to propagate the 100 to 200 ps wide SET pulse any appreciable distance. However, as smaller feature size technologies are being used in spaceborne systems, these transients become indistinguishable from normal circuit signals.

If a charge particle strike occurs within the combinatorial logic block of a sequential circuit, and the logic is fast enough to propagate the induced transient, then the SET will eventually appear at the input of data latch where it may be interpreted as a valid signal. Similar invalid transient data might appear at the outputs of lookup tables and on routing lines due to SETs generated in the programming elements.

While conventional SEU error rates are independent of the chip clock frequency, SET increase in direct proportion of the operating frequency. Smaller feature size results in smaller gate delays that permit circuits to be operated at higher clock frequencies. For typical FPGA designs, SET induced error rates may actually exceed the SEU rate of unhardened latches as clock speeds approach 100 MHz for CMOS designs.

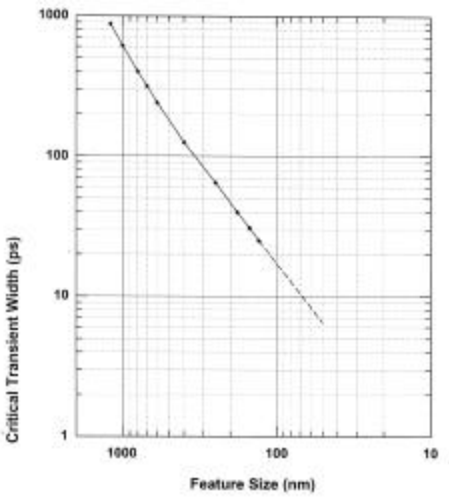

Fig.12 Critical Transient Width vs Feature Size for unattenuated propagation. The picture is taken from Ref [4]

In figure 12 is illustrated the critical transient pulse width as function of technology feature size needed to propagate without attenuation through any number of gates [x]. At pulse widths smaller than the critical width, the inherent inertial delay of the gate will cause the transient to be attenuated and the pulse will after passing a few gates die out. At pulse widths equal or larger than the critical width, the transient will propagate through the gate just as though it was a normal circuit signal.

A. RT54SX-S Details

The architecture of Actel RT54SX-S devices is an enhanced version of Actel SX-A device architecture. The RT54SX-S devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility. The RT54SX-S family incorporates up to four layers of metal interconnects.

To achieve good SEU requirements each register cell (R-Cell) in the RT54SX-S are build up with Triple Module Redundancy (TMR) The R-cells in the SX-S device consists of three master and three slave latches gated by opposite edges of the clock. The feedback path of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching.

With this solution the latches is continuously corrected and theoretically the only possibility for a SEU in a R-register is to have two latches hit by two ions within the recovery time of the transient created by the ions.

B. SEU Results of RT54SX32-S

No SEU in the R-register cells have been observed under static conditions up to LET= 64.5 MeV/cm2/mg.

Irradiation with heavy ions under 5 MHz dynamic condition resulted in errors, which had the same signature as if they were proper SEU. When lowering the FPGA operating frequency by a factor of 4 to 1.25 MHz no errors could be observed. From the static condition test it was concluded that the R-cells do not upset. Thus, the errors observed in 5 MHz dynamic mode are very likely due to transient effects SET which are clocked through to the output.

The duration and magnitude of the transients are, however, technology and circuitry design dependent. In the present experimental set-up it is not possible to isolate the error data to certain areas or functions of the device.

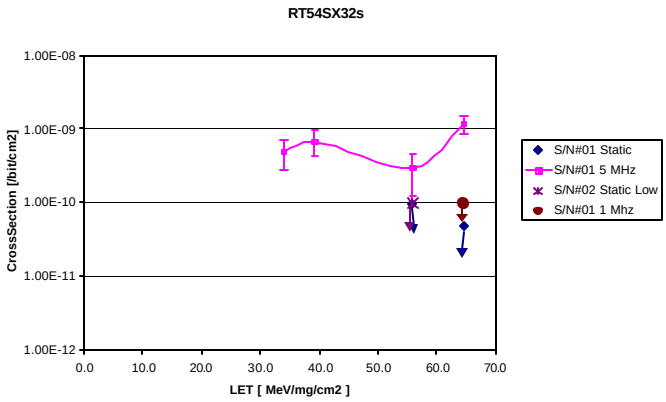

Fig 13 Single Event Transient cross section as a function of LET value for RT54SX32S. Errors have only been detected in 5 MHz dynamic test mode. The data points with arrows indicate fluence for test run without errors. The error bars are the standard deviation indicating counting statistics for each test run. No conventional SEU can be detected for this device type.

X. CONCLUSION

Test results presented in this paper are all on COTS type of FPGAs. The use of COTS in radiation environment require, however, that testing to the needed reliability requirements are performed. A vast majority of complex IC's will not pass the minimum requirement of being latch-up free in a charge particle environment. Once the single event upset problems have been characterised there are techniques to mitigate the SEU problems. Such knowledge helps selecting between hardened technologies and speed and area trade-offs in a softer technology. With decreasing feature size, the single event transients will become more important. For frequencies above 100 MHz, the probabilities are in the same order as for conventional upsets. So far no experimental data have been published which show the transient probabilities at proton energies for complex CMOS technologies.

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