

Development and a SEU Test of a TDC LSI for the ATLAS Muon Detector

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Abstract

A new TDC LSI (AMT-2) for the ATLAS Muon detector has been developed. The AMT-2 chip is a successor of the previous prototype chip (AMT-1). The design of the chip was polished up for aiming mass production of 20,000 chips in year 2002. Especially, power consumption of the chip was reduced to less than half of the previous chip by introducing newly developed LVDS receivers.

The AMT-2 was processed in a 0.3 μm CMOS Gate-Array technology. It achieved 300 ps timing resolution and includes several data buffers, trigger matching circuit, JTAG interface and so on.

First SEU test by using a proton beam was recently performed. Although the test results are very preliminary at present stage, we get very low SEU rate safely used in ATLAS environment.

I. INTRODUCTION

ATLAS precision muon tracker (MDT) requires high-resolution, low-power and radiation-tolerant TDC LSIs (called AMT: ATLAS Muon TDC). Total number of TDC channels required is about 370 kch.

The AMT chip is developed in a 0.3 μm CMOS Gate-Array technology (TC220G, Toshiba Co.). Block diagram of the chip is shown in Fig. 1. It contains 24 input channels, 256 words level 1 buffer, 8 words trigger FIFO and 64 words readout FIFO. Both leading and trailing edge timings can be recorded. The recorded data are matched to trigger signal timing, and the matched data are transferred through 40 Mbps serial line. By using an asymmetric ring oscillator [1] and a Phase Locked Loop (PLL) circuit, it achieved 300 ps RMS timing resolution.

A prototype chip, AMT-1, was successfully tested and reported in the last LEB workshop [1]. Already 500 AMT-1 chips were produced and mounted in front-end PC boards with ASD (Amp/Shaper/Discriminator) chips [2]. These boards are being tested with MDT chambers in several laboratories.

AMT-2 chip is a successor of the AMT-1 chip and regarded as a prototype for mass production. Major improvement of the AMT-2 is reduced power consumption. The AMT-1 consumes about 800 mW of which 470 mW is consumed in LVDS receivers. We have developed a new low-power LVDS receiver and proceeded to low power design of logics. Thus the power consumption of the AMT-2 is reduced to 360 mW.

In addition, the chip testability was enhanced. This is very important for mass production. Mass production chips will be mainly tested at LSI testes of the manufacturer. Only very small fraction of the chip will be tested in our laboratory. Since the LSI testers runs only at 10 MHz, special care must be taken to verify 40 MHz operation. We think reduced voltage test will certify the operation. To verify the stability of the PLL, internal counter is prepared to count 80 MHz PLL clock. After a fixed time, the counted value will be checked.

Photograph of the AMT-2 chip is shown in Fig. 2. The chip is packaged in a 144 pins plastic (ceramic) QFP with 0.5 mm pin pitch. About 110k gates are used in a 6 mm by 6 mm die.

The chip must be qualified to have adequate radiation tolerance in ATLAS environment. Gamma-ray irradiation to measure Total Ionization Damage (TID) was already done to the same process [3]. Recently we executed a first experiment of the Single Event Upset (SEU) test by using a proton beam. Preliminary results are described in section IV.

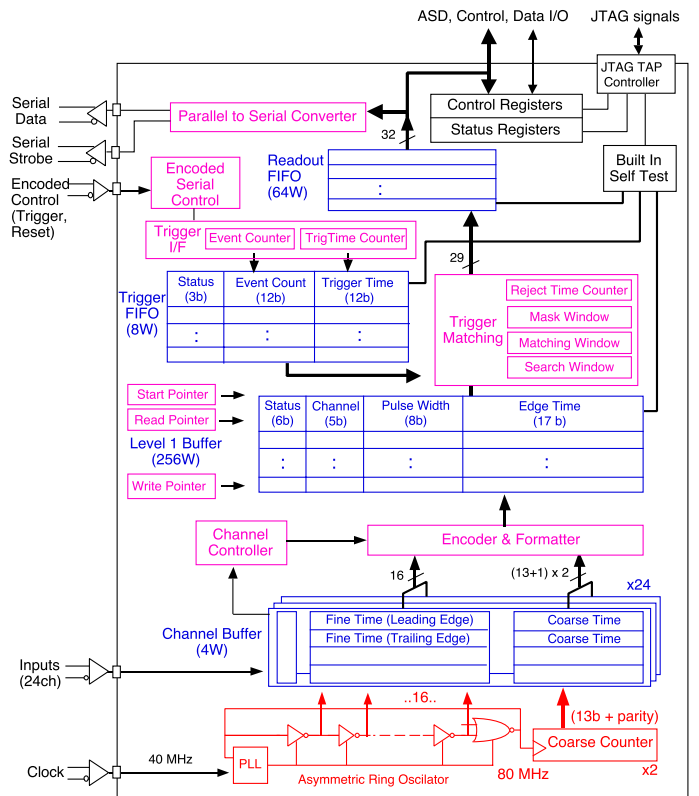


Fig. 1 Block diagram of the AMT-2 chip.

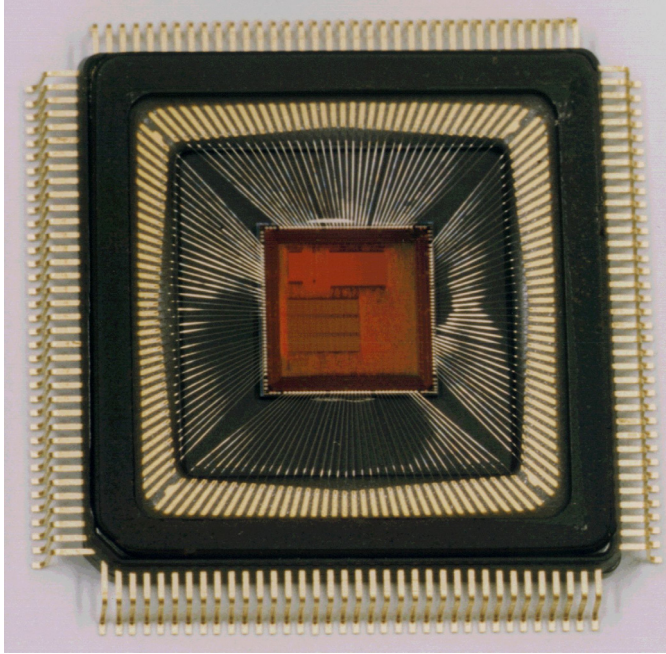


Fig. 2 Open view of the AMT-2 chip. The die size is about 6 mm by 6 mm. The photograph is ceramic packaged chip. Plastic packaged ones are used in circuit tests and beam tests.

II. AMT-2 CIRCUIT DESCRIPTION

Main specification of the AMT-2 chip is summarized in Table. 1. Since the detailed description of the AMT chip is available in other documents [4, 5], only new features are presented here after brief explanation of the chip operation.

Table. 1 AMT-2 Specification (@40MHz System Clock)

Least Time Count	0.78125 ns/bit
Time Resolution	300 ps RMS
Dynamic range	13 (coarse) + 4 (fine) = 17 bit
Max. Trigger Latency	16 bit (51 μ sec)
Int./Diff. Non Linearity	< 80 ps RMS
No. of Channels	24 Channels
Level 1 Buffer	256 words
Read-out FIFO	64 words
Trigger FIFO	8 words
Double Hit Resolution	<10 ns
Hit Efficiency	100% @400 kHz (single edge) >99.8% @400kHz (two edge)
Hit Input Level	LVDS
Data output	LVDS Serial (10 - 80 Mbps) or 32 bit parallel.
CSR access	JTAG or 12 bit control bus.
General I/O	ASD control I (5 pins) and general out (12 pin) and in (3 pin).
Power	3.3+0.3V, ~360 mW
Process	0.3 μ m CMOS Sea-of-Gate
Package	144 pin plastic QFP

A. AMT-2 Operation

The asymmetric ring oscillator produces a double frequency clock (80 MHz) from a LHC beam clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals in the oscillator, a time bin size of 0.78 ns is obtained.

A hit signal is used to store fine time and coarse time measurement in individual channel buffers. The time of both leading and trailing edge of the hit signal (or leading edge time and pulse width) can be stored. Each channel has a 4-word buffer where measurements are stored until they can be written into the common level 1 (L1) buffer.

The L1 buffer is 256 hits deep and is written into like a circular buffer. Reading from the buffer is random access such that the trigger matching can search for data belonging to the received triggers.

Trigger matching is performed as a time match between a trigger time tag and the time measurements themselves. The trigger time tag is taken from the trigger FIFO and the time measurements are taken from the L1 buffer. Hits matching the trigger are passed to the read-out FIFO.

The data are transferred to a Chamber Service Module (CSM) [6] through a serial data interface. The serial interface supports both DS-protocol and simple data-clock output. The data transfer speed is selectable between 10 MHz to 80 MHz (40 MHz will be used in the MDT).

There are 15 control registers and 6 status registers. These registers are accessible from JTAG interface. A total parity of the control registers is stored in the status register. If a SEU occurs in the control register, a parity error is caused and notified through an Error signal or an Error packet.

The chip has JTAG boundary scan circuit, which is used to scan I/O pins, the control and status registers, internal circuit registers for debugging purpose, and BIST (Built-In Self-Test) for the level 1 buffer and FIFOs. The channel buffer and the level 1 buffer have a parity bit for each word to detect SEU. In the AMT-2, ASD control function through the JTAG is also added (see section II-C).

B. New LVDS Receiver

We used existing Toshiba design of the LVDS receiver in the AMT-1. The power consumption of the LVDS receiver (15.5 mW) does not cause much problem if the number of the receiver is small. However we need 26 (30 in AMT-1) receivers, and the total power consumption becomes large (470mW). Thus a new low-power LVDS receiver was required.

Although the available transistor size is very limited in I/O pad area in a Gate-Array, a low-power LVDS receiver was successfully developed while keeping adequate performance.

Fig. 3 shows performance of the previous and new LVDS receivers. The propagation time is even improved while reducing the constant current. This was mainly achieved by reducing the size of input transistors.

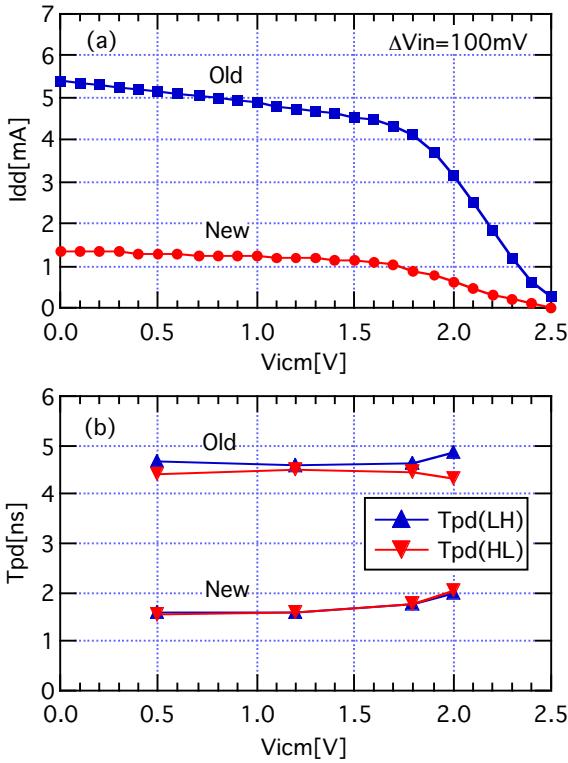


Fig. 3 Comparison of previous and new LVDS receiver characteristics (simulation). (a) Constant current (I_{dd}) vs. input common mode voltage (V_{icm}), (b) propagation delay (T_{pd}) vs. V_{icm} . LH and HL denotes Low to High and High to Low transition of the output.

C. ASD Control

The ASD chip has many registers to keep shaping time, threshold DAC value etc. A Xilinx chip is used to control these ASD registers from JTAG signal in the present front-end board.

This Xilinx chip consumes additional power and area, and it also must be qualified for radiation. Since the power and the area are very tight, it was decided to move the ASD control function into the AMT-2. Fig. 4 shows the principle connection between the AMT and the ASD. Five signal lines are used between the ASD and the AMT-2.

Main protocol is almost same as JTAG boundary scan cell. Data are shifted from ASDOUT to ASDIN through 3 ASD chip. The shifted data are stored in shift cells and copied to shadow cells when ASDLOAD signal is asserted.

In addition to the ASD control, 12 output and 3 input pins are prepared as a general purpose I/O pins. These pins can be used when additional control lines are needed in the front-end board.

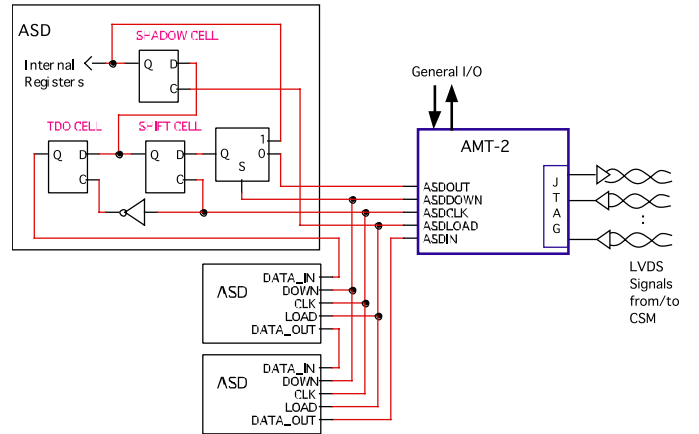


Fig. 4 ASD internal circuit and control signals from the AMT-2.

III. MEASUREMENT RESULTS

A. PLL

Jitter of the ring oscillator was measured by time distribution between input clock edge and PLL clock edge (Fig. 5). The jitter at operating point (3.3V, 80MHz) is 150 ps RMS. This value is sufficiently low compared with digitization error of 225 ps. Total timing resolution for a single edge measurement will be about 300 ps. This satisfies the required resolution of 0.5 ns in the MDT.

Fig. 6 shows the jitter variation to the oscillating frequency (F_{osc}) and the power supply voltage (V_{dd}). This indicates enough margins around the operating point.

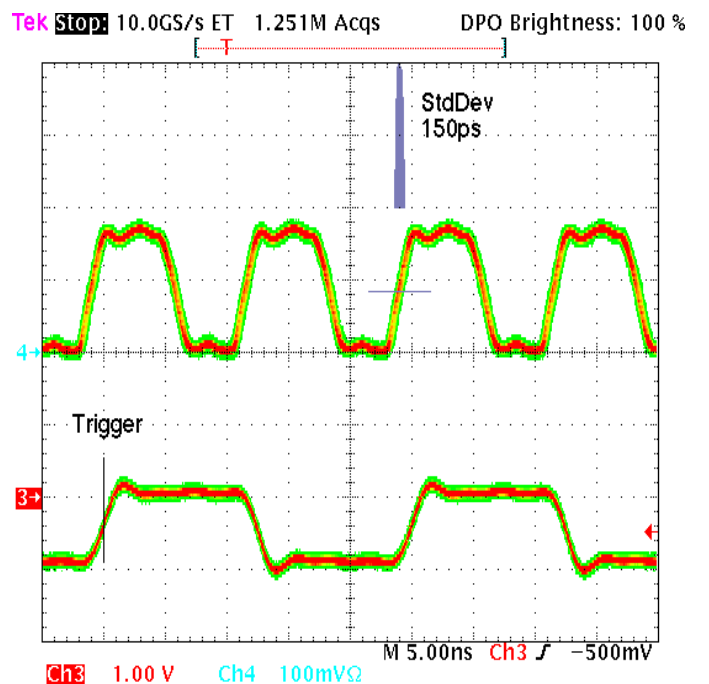


Fig. 5 PLL output clock (upper curve, 80MHz) and timing distribution (histogram) triggered with external clock (lower curve, 40MHz).

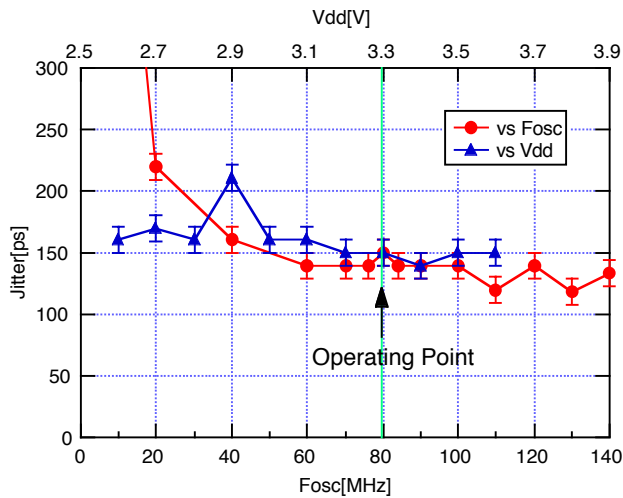


Fig. 6 PLL jitter variation for oscillating frequency (@Vdd=3.3V) and supply voltage (@Fosc = 80 MHz).

B. Power Consumption

Total power consumption of the chip is measured at several operating conditions and shown in Fig. 7. In a very severe condition (100kHz hit rate and 100 kHz Trigger rate) power consumption is about 15 mW/ch. Compared with previous chip (AMT-1) we could reduce 18 mW/ch. This is achieved mainly by using the new LVDS receiver and reducing the number of LVDS receiver from 30 to 26.

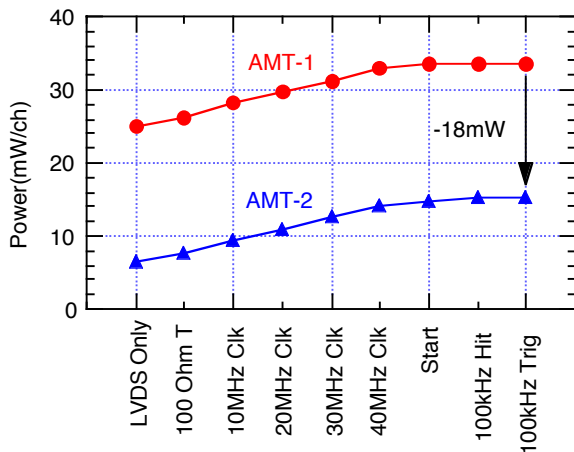


Fig. 7 Power consumption of the AMT-1 and the AMT-2 chips for different operating conditions. Conditions are changed from left to right; powered to LVDS circuit only, 100 ohm termination resistors were connected to LVDS drivers, external clock (10-40 MHz) is applied, measurement started, 100 kHz hit signals are applied, then finally a 100kHz trigger signal is applied.

IV. SEU TEST

Radiation tolerance of the present process for Total Ionization Damage (TID) was already measured and shows adequate tolerance to gamma ray [3]. Furthermore CMOS process is not sensitive to neutrons in estimated level of the MDT environment.

Remaining issue is Single Event Effects (SEE) caused by energetic hadrons (> 20 MeV) [7]. To measure the SEE, we need to perform beam test to the chip.

There are several single event effects in which Single Event Latch up (SEL) and Single Event Upset (SEU) are important for CMOS process. We have done first test of SEU by using a proton beam.

We used an AVF cyclotron at the Cyclotron and Radioisotope Center (CYRIC) of the Tohoku University, Japan. The Cyclotron was recently upgraded and has maximum proton energy of 90 MeV.

We have done a first beam test by using a 50 MeV proton beam, and irradiated 2 AMT-2 chips. Beam intensity was around 1 nA and the beam size was monitored visually to have 2 cm ϕ . During the irradiation, beam intensity was monitored with two plastic scintillators, but no special device was used to measure its distribution.

AMT-2 has 180 bits in the CSR registers, and a total of 11,360 bits in the L1, the trigger and the readout buffers. The CSR register was composed of Flip-Flops, and the buffer memories are composed of 6 transistors static memory cell. Both circuits has almost complimentary circuit for positive and negative logic signals, so we assume the SEU rate may be same regardless of the contents of memory.

Unfortunately we cannot directly read and write the contents of the buffers. Instead we used Built-in Self-Test (BIST) circuit to detect the SEU. The BIST circuit performs two kinds of 13N marching pattern test. The results are compressed in a 36-bit Linear Feedback Shift Register. If one or more error occurs in this test sequence, final result has different value.

We step forward the BIST sequence until writing all '1's (or '0's) to all memory location. Then irradiate the chip to the beam. After the irradiation, we continue the BIST sequence and read out the final value. These measurements were repeated several times. Since the SEU rate is very low, it is very rare to occur more than 2 SEU during one measurement. We have observed 3 SEU in 18 measurements.

As for the CSR, the contents are directly written and read through JTAG lines. Before the irradiation '0's and '1's were written to the CSRs, then after the irradiation the contents were checked for SEU. We have not observed any bit flip in the CSR test.

Fig. 8 shows leakage currents of the chip for gamma ray and proton. Horizontal scale is adjusted to fit both curves. Since the proton irradiation was paused during the measurement, annealing was occurred during the each measurement. Therefore the proton data are discontinuous at the boundary of measurement. Assuming the leakage current depend only on energy deposit in Si, proton flux is estimated to be about 2×10^9 protons/sec/cm 2 . This is consistent with the value estimated from the beam intensity and its size.

The SEU test results are summarized in Table. 2. Assuming a Poisson distribution of the SEU event, we get upper limits of the cross section in 90% confidence level.

$$\sigma_{\text{SEU}} (\text{CSR}) < 5.6 \times 10^{-15} \text{ cm}^2/\text{bit}$$

$$\sigma_{\text{SEU}} (\text{buffer}) < 2.7 \times 10^{-16} \text{ cm}^2/\text{bit}$$

Calculated fluence of hadrons with an energy $>20\text{MeV}$ is $\sim 10^{10} \text{ 1/cm}^2/10\text{year}$ in MDT location [7]. Applying number of bit in total MDT system, SEU rates (R_{SEU}) will be,

$$R_{\text{SEU}} (\text{CSR}) < 0.1 \text{ upset/day}$$

$$R_{\text{SEU}} (\text{buffer}) < 0.3 \text{ upset/day.}$$

Thus less than 1 upset in the CSR for 10 days of operation in MDT system. Furthermore there was no latch up during the experiments for both chips.

Although these results are very preliminary, we feel relieved in very low SEU rate in both control registers and data buffers. This is mainly because the transistor size is relatively large in Gate-Array, so large charge is required to upset the memory.

Although the leakage current was useful to estimate the proton flux, but the large leakage current might cause damage to the chip. Therefore it is better to irradiate less fluence to a chip, and accumulate more statistics by irradiating many chips. Further experiment are being planned.

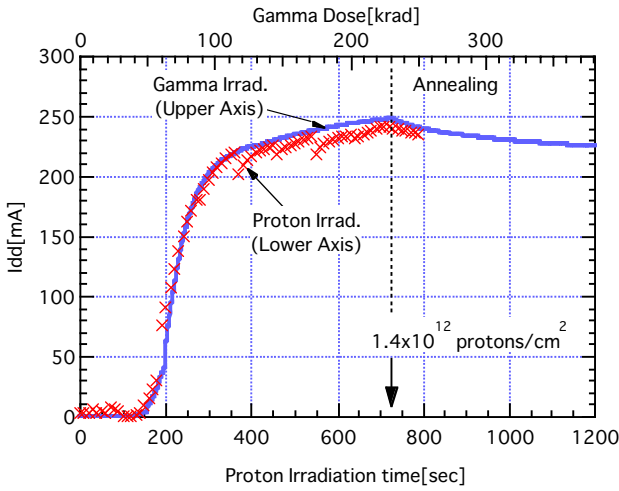


Fig. 8 Leakage current of the AMT-2 chip for gamma ray and proton irradiation. Data for proton is not continuous since the irradiation was stopped in each measurements and annealing was occur in each measurement.

Table. 2 Number of observed SEU in the proton irradiation experiment.

	Proton Fluence	No. of meas.	SEU in CSR	SEU in buffers	σ_{SEU} buffers
Chip 1	1.4×10^{12}	8	0	1	6.3×10^{-17}
Chip 2	1.0×10^{12}	10	0	2	1.8×10^{-16}
Chip 1+2	2.4×10^{12}	18	0	3	1.1×10^{-16}

V. SUMMARY

A production prototype chip (AMT-2) was successfully developed for ATLAS MDT detector. The chip fulfils required performance and being tested with MDT chambers.

A new LVDS receiver is developed and the power consumption of the AMT-2 chip is reduced to 45% of the previous chip.

Preliminary test of SEU rate by using a proton beam was performed and shows low enough rate to be safely used in the MDT. Latch up was not observed in this test.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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