STATUS OF ATLAS LAr DMILL CHIPS

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On behalf of the LArG collaboration

Abstract

This document reviews the status and performance of the ten DMILL chips developed in 2000-2001 by the ATLAS liquid argon (LAr) community in order to ensure the radiation tolerance of its front-end electronics.

1. INTRODUCTION

The LAr front-end electronics is located right on the cryostat in dedicated front-end crates [1]. These house four different species of boards :

- Front-end boards (FEB) which bear preamplifiers, shapers, analog memories, ADCs and optical outputs.
- Calibration boards to generate 0.2% accuracy calibration pulses
- Tower builder boards (TBB) which perform analog summation and re-shaping for LVL1 trigger
- Controller boards which handle TTC and serial link (SPAC) control signals

.All these boards have been produced in several exemplars in order to equip module 0 calorimeter and extensively used in the testbeam for the last three years. Their performance has met the requirements in terms of signal, noise, density at the system level on several thousands of channels [2]. However, they make use of many COTS, in particular FPGAs which are not radiation tolerant.

Since then, several developments have been realised in order to design the "final" ATLAS boards, based on the same architecture but completely radiation tolerant, by migrating most of the COTS into DMILL ASICs [3]. A milestone has been set to get the first boards by end-2001 and a full crate by the end of 2002.

The radiation levels anticipated at the LAr crate location is 50 Gy in 10 years and 1.6 10^{12} N/cm^2. Taking into account the safety factors required by the rad-tol policy [4] , they must be qualified up to 0.2-3 Gy (20-300 krad) and 1-5 10^{13} N/cm^2, depending on the process as explained in ref. [5]. For DMILL chips, the radiation tolerance criteria (RTC) are

- RTC_{TID} = 3.5*1.5*2*50 = 5 kGy
- RTC_{NIEL} = 5*1*2*1.6$10^{12}$ = 1.6 10^{13} N/cm^2
- RTC_{SEE} = 5*1*2*0.7$10^{11}$ = 7.7 10^{12} $h_{>20MeV}$/cm^2

The performance of all these DMILL chips and in particular the yield and results of irradiation and SEE tests are presented below.

2. CALIBRATION BOARDS [6]

The calibration board houses 128 pulsers which generate accurate pulses to simulate the detector signal over the full 16bit dynamic range. It is based upon 128 0.1% precision DC current sources and HF switches which transform the DC current into fast pulses with a 400 ns exponential decay. The calibration board is used to inter-calibrate the 160 000 readout channels and measure their three gains.

2.1 16bit DAC

A 16bit DAC with 10 bit accuracy is necessary to cover the full dynamic range of ATLAS and COTS did not provide adequate radiation tolerance. Therefore, a 16 bit R/2R ladder DAC has been made with 16 switched identical current mirrors. As there is only one DAC per board, external precision resistors (0.1%) can be accomodated. To reduce the sensitivity to V_{BE} mismatch and variations with temperature the emitters of the current sources are strongly degenerated. This ladder DAC has been developed and tested successfully in AMS 0.8 µm BiCMOS and submitted to DMILL in may 2000, with improved temperature stability (1 µV/K).

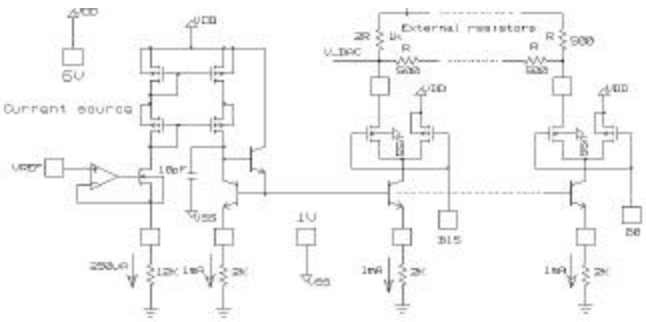


Figure 1 : *Schematic diagram of the 16bit ladder DAC*

19 chips have been received in march 2001 among 18 were fully functional, giving a yield of 94% for a chip area of 6.3mm^2.

The performance measured is 0.01% integral non linearity over the 3 gains as shown in Fig. 2. The temperature stability has been measured on 10 chips between 20 and 65C to be of +0.01%/K.

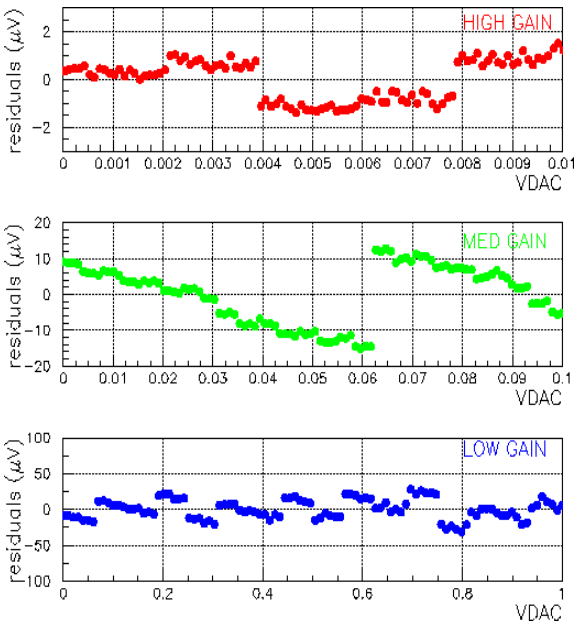


Figure 2 *: residuals of a linear fit on the DAC output over the three shaper ranges (10 mV, 100mV, 1V)*

10 chips have been irradiated up to 9. 10^{13} N/cm^2 at CERI (20 MeV) and to 2 kGy ^{60}Co at Saclay and measured on line. The result, shown in Fig. 3 and 4, indicate good tolerance to Neutrons (0.1% variation up to RTC) but also a visible drift with gammas (-0.5% after 2 kGy). As the bits ratio turned out to be very stable, the decay has been traced down to a change in the reference current : in effect a one-mV V_T shift in he current mirror is enough to cause the effect.

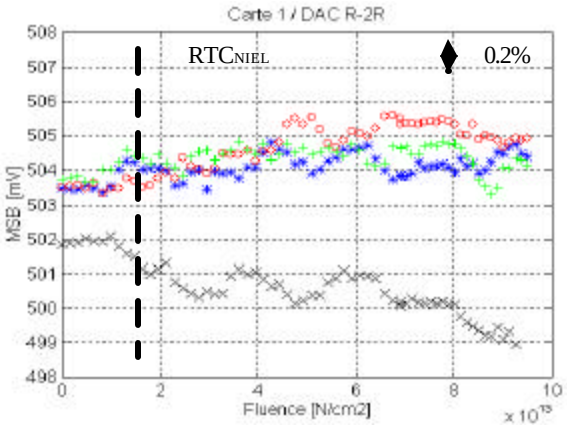


Figure 3 *DAC output voltage under Neutron irradiation*

Although acceptable as such, enough time was available for an iteration with an improved reference source : a band gap reference incorporated and the current mirror

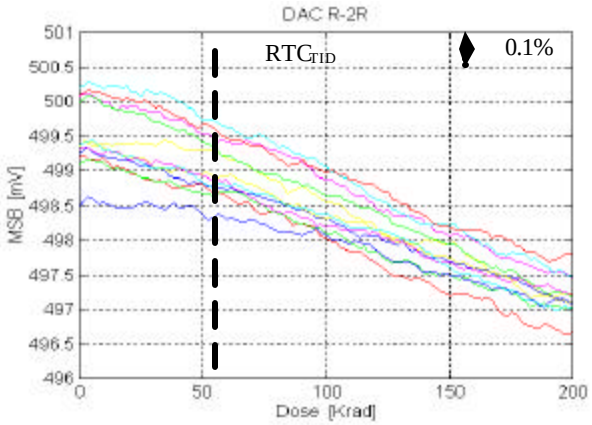


Figure 4 *: DAC output voltage under gamma irradiation*

has been replaced by a reference source built around a low-offset opamp as described below.

2.2 Low offset opamp

The DAC voltage is distributed throughout the board to 128 channels in order to produce the 2 µA – 200 mA precision current. The voltage to current conversion is based upon a low-offset opamp and a 0.1% 5Ω resistor. The opamp offset should not be larger than the DAC LSB=16µV. Again COTS did not provide adequate radiation tolerance and ASICs were developed along two paths : static and auto-zero. After prototyping in AMS, the static configuration was chosen and translated into DMILL.

As shown in Fig. 5, the circuit is built around a bipolar differential pair and external precision collector resistors (150kΩ 0.1%). The transistors are 10*1.2 NPN, mounted in centroid configuration ; a larger transistor size would in principle further reduce the offset, but would decrease the radiation hardness due to a too low current density. This input stage provides a gain of 127, enough to disregard the second stage offset. The chips are sorted to be within ± 100µV.

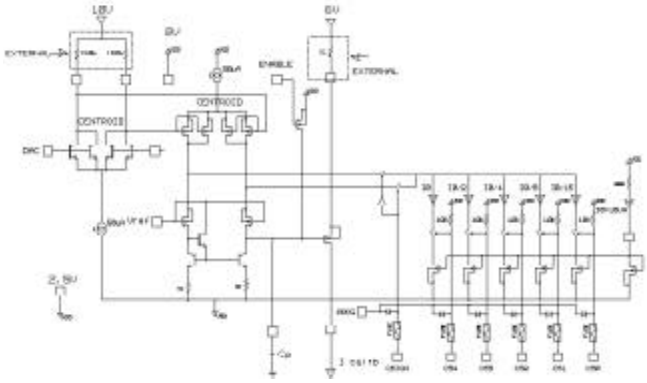


Figure 5 *: Schematic diagram of the low-offset opamp*

The second stage is built around a cascoded PMOS differential pair, again in a centroid configuration. A bank of 5 binary scaled current sources allows to add or remove up to 20% of the static current and allow further trimming down to ± 10µV. The total open loop gain is 80 000, in good agreement with measurements. The output stage is a large (20,000/0.8) PMOS in order to drive the large maximum output current (200 mA).

40 chips have been received in march 2001 among which 37 were fully functional, giving a functional yield of 94% for a chip area of 2 mm^2. The circuits have then been tested for the offset performance. As anticipated, the offset is dominated by the input pair and 27 chips were found between ± 100µV, giving a total yield of 70%, similar to what was obtained with the AMS prototype.

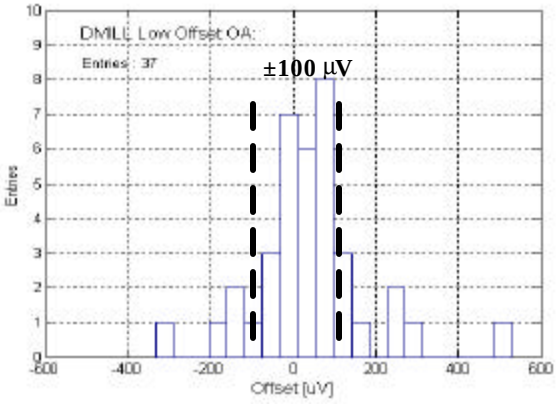
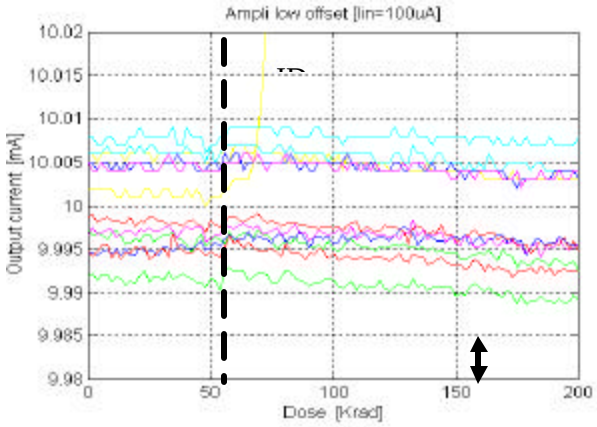


Figure 6 : *Offset distribution of the input bipolar pair.*

Concomitantly to the DAC, ten opamps have been irradiated to photons and neutrons. As can be seen in Fig.7, the offset has remained stable inside 15 µV up to 2 kGy. Incidentally, an AMS version which was left there died immediately after RTC (yellow curve).



The test to Neutrons was also performed far in excess of the requirements. After 2.5 10^{12} N/cm^2, the circuits could no longer be measured on line because of the failure of a discrete NPN transistor commanding the multiplexing relays. Notwithstanding, the circuits were measured again after the irradiation and had remained stable.

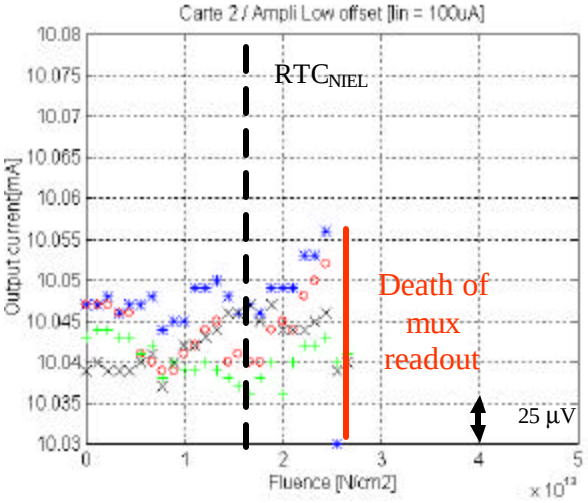


Figure 7 *: Neutron irradiation of the low offset opamp*

2.3 *Calibration logic*

The calibration boards used on module 0 were controlled by an elaborate digital circuitry which allowed to load on board a full calibration sequence (ramping the DAC, changing patterns…)[7]. Although practical and very time efficient this circuitry was based on memories and numerous FPGAs which would not operate reliably in the high radiation environment. It has thus been decided to simplify the control logic and load through the SPAC serial bus the run parameters (DAC value, delays, pulsing patterns). These parameters are decoded from I^2C local bus and stored in registers which have again been designed in DMILL. No particular SEU mitigation has been included as the calibration board is idle 99% of the time and SEU results only in a wrong calibration pulse, which can be discarded in the RODS.

The chip covers an area of 16 mm^2 and has been submitted in may 2000. 20 chips have been received in march 2001, among which 17 were functional, giving a yield of 70%.

Two chips have been subsequently tested for SEU at Louvain with 70 MeV protons. No SEE have been observed up to a fluence of 3 10^{12} p^+/cm^2. Extrapolating this cross-section to ATLAS yields one SEE/2 days, assuming the calibration is used 1% of the time.

3. FRONT-END BOARDS [8]

The Front-end board has necessitated the development of 6 chips in DMILL in order to ensure the integration of all the elaborate digital electronics necessary to operate the board. Except the preamplifier (bipolar hybrid) and the shaper (BiCMOS AMS), almost all the front-end board is built around DMILL chips. The analog pipelines (*SCA*) which follow the shapers have been designed from the start in DMILL. They make use only of the CMOS components and of full custom logic running at 40 MHz. The read and write addresses necessary to operate the SCA with no dead time are generated by a *SCA controller*. The gain selection at the SCA output are also handled by a dedicated ASIC : the *gain selecto*r. Then the data are multiplexed to 16bit 80 MHz (*MUX* chip), to be fed into the Glink serializer and output optically. Furthermore, the parameters necessary to operate the board are loaded by a serial link (SPAC). A serial link decoder (*SPAC slave*) is necessary as well as a *configuration controller*.

3.1 Switched Capacitor Arrays (SCA)

The analog pipeline is a key element of the front-end board, as it stores the analog signal until the reception of LVL1 trigger in a bank of 144 capacitors with a 13 bit dynamic range. Several prototypes have been realized in DMILL in the last 3 years, as well as in radiation soft technologies (AMS 0.8 µm, HP 0.6 µm) with similar electrical performance [9].

As more than 50 000 good chips will be necessary, corresponding to more than 200 wafers, the yield is of particular concern. Most of the various batches received so far have exhibited satisfactory yield above 65%, except a recent one as low as 10% due to a few randomly distributed leaky switches. This process defect has subsequently been understood and fixed in a later batch. Before undergoing mass-production in 2002, the final engineering run has been submitted at the end of 2000 and received in march 2001. More than 2500 circuits have been measured with the automated testing setup [10].

batch	date	# chips	yield
V 1.1	6/98	30	90%
V 1.2	8/98	30	80%
V 2 wafer 12	8/99	68	50%
V 2 wafer 4	8/99	49	84%
V 3.1	12/99	18	10%
V 3.2	7/00	35	65%
V 3.2 eng. run	3/01	2534	65%

An important parameter on the acceptance cuts is the leakage current. Although most of the cells exhibit very low leakage (2 fA in average), the requirement of having all cells on the sixteen channels (16*144) below 5 pA is enough to induce a 4% yield loss.

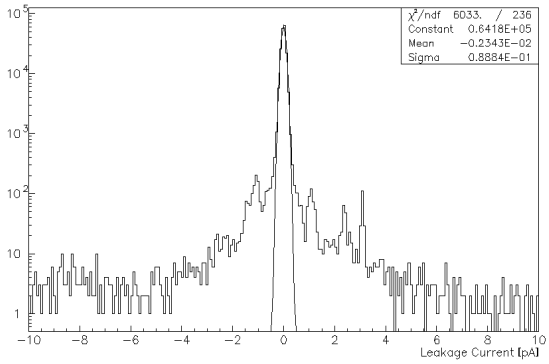


Figure 9 : *leakage current of all the SCA cells*

3.2 SCA controller (SCAC)

In module 0 FEB, the SCA controller was implemented in a XC4036 Xilinx, based on 0.35 µm technology. This component has been extensively tested for radiation tolerance and has shown a significant supply current increase after 400 Gy. Moreover, SEU tests have been carried out and have shown a cross section for SEU of $\sigma_{SEU} = 2.7\ 10^{-9}\ cm^2$, a LET for the configuration switches of 22 MeV and worse of all, one latch-up event [11].

It has then been decided to migrate this element into DMILL. However, the chip complexity and critical timings have turned out to be marginally achieved and resulted in a very large chip area ($80mm^2$) for which the yield was likely to be rather small (20%). Besides, due to the large area, it has not been possible to include any error correction mechanism, leaving the SEU problem open. For such chip, the SEU effects are rather serious as read or write pointers could get systematically wrong. A fallback in 0.25µm technology has thus also been designed, including SEU error correction logic, and submitted in march 2001.

40 DMILL SCA controllers have been received in june 01, among which 28 have passed all the digital tests, giving an unexpectedly high yield of 70%. Nine chips have been tested for maximum clock frequency and all ran up to 50 MHz. The chips also passed successfully a burn-in test.

Four chips have then been tested for SEU at Triumf with 74 MeV protons. The associated TID was around 40-70 krad. After $4.6\ 10^{10}$ p+, all chips needed a power-on cycling to reset. It has been traced to a fault in the (analog) power-on reset, which has been subsequently removed. Extrapolated to ATLAS, each SCAC would need a reset every 70 days, amounting to a reset every hour over the whole experiment.

3.3 Gain selector

The SCA is followed by a 12 bit 5 MHz ADC (AD9042) which has been qualified by CMS [12]. Two ADCs feed a gain selector chip which chooses the correct gain and formats the data for the subsequent RODs. As the chip stores two thresholds per channel for the gain selection, SEU have been mitigated with a Hamming correction code. It results in a 21 mm^2 ASIC, submitted to DMILL in september 2000. The same chip has also been submitted in 0.25 µm alongside with the SCA controller.

29 DMILL chips have been received in may 2001 and 27 were functional, giving a yield of 93%. Five chips have been tested for SEU at Harvard facility with 50, 100 and 158 MeV protons. The single event upset can be sorted in two categories : single bit errors (SBE) corresponding to one bit flip in the registers which is corrected by the error correction algorithm and single event upsets corresponding to a wrong bit in the output data which leads to a rejected event in the RODs. The measurements are shown in the table below. Coarsely extrapolated to ATLAS by multiplying the cross section by the hadron flux RTC (supposed flat) leads to 1 SBE/30mn and 1 SEU/168 mn for the full calorimeter (13 000 chips).

Energy	Fluence	#SBE	σ_{SBE}	#SEU	σ_{SEU}
MeV	$10^{13}/cm^2$		10^{-13}		10^{-13}
50	2.4	0	-	0	-
100	4.0	14	3.5	4	1.0
158	20.8	212	10.2	38	1.8

3.4 Optical output

The formatted digital data are sent out after LVL1 trigger through an optical fiber. Five samples of each 128 channels are multiplexed at 40 MHz, resulting in 2.6 Gbit/s output rate. The baseline option was using HP Glink, but extensive irradiation studies [13] have shown that although the link exhibited very good total dose tolerance up to 43 kGy and 10^{13} N, it was sensitive to SEU, 0.05 error/link/hour with ATLAS spectrum. In particular, energetic neutrons could induce synchronization errors, bringing the link down up to 10 ms [14].

A multiplexing chip (MUX) is necessary to turn the 32bit 40 MHz data into 16bit 80 MHz Glink input format. Initially, the design was done for a dual Glink option to improve redundancy [14]. This DMUX chip has been submitted in DMILL in may 2000 [15].

18 chips have been received in march 01, with a functional yield of 88% for a chip area of 16 mm^2. Four of them have been irradiated at CERI for SEE tests alongside with the Glink. Its contribution to SEU rate is negligible compared to the Glink. Furthermore, no parameters are stored in the chip, which renders SEU effects very minor.

3.5 Configuration chips (SPAC,FEBconfig)

All the parameters necessary to operate the FEB are loaded via a serial bus on the front-end crate (SPAC), inspired from I^2C [16]. This bus is decoded by an ASIC called SPAC slave, which provides regular I^2C and parallel outputs. This chips has also required the development of a special RAM and is common to all the boards.

Submitted in September 00, 18 chips have been received in march 01. The functional yield is 94 %, for a chip area of 27 mm^2. It has been iterated in sept 01 to mitigate possible SEU effects, in particular on the sub-address, with error correction logic.

Some additional functions which are specific to the FEB have been grouped in another DMILL chip called configuration controller. The design has also been submitted in September 2000 and 40 chips have been tested in july 2001. The functional yield is 93 %, for a chip area of 20 mm^2. The chip is final and has been tested successfully in relation with the other chips on a "quarter digital FEB", shown below.

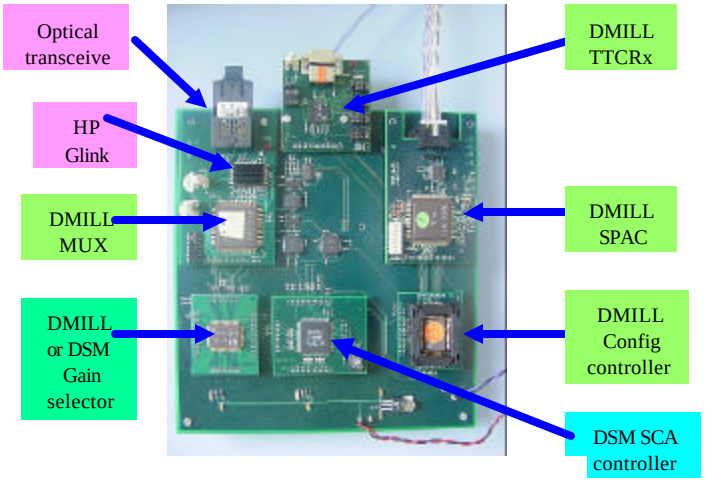


Figure 10 *: Picture of the "quarter digital FEB" used to test the FEB DMILL chips.*

4 chips have also been tested for SEE at Harvard with 158 MeV protons. The associated TID was 2-15 Mrad. After a fluence of 7 to 22 10^{13} p^+/cm^2, 69 SEU have been observed, giving a cross section of $\sigma_{SEU} = 1.5\ 10^{-13}\ cm^2$. Extrapolating this rate to ATLAS gives a rate of 1 SEU/26.8 hr.

4. PRODUCTION STRATEGY

Except the SCA, the SCA controller and the gain selector, most of the DMILL chips are needed in quantities which are too small to justify dedicated wafers. It has thus been decided to group them on shared wafers to reduce the price of the masks. Two shared wafers will thus be produced :

- An analog wafer grouping 52 low offset opamps, 1 DAC and 26 BiMUX
- A digital wafer with the 4 SPAC, 2 calogic, 3 FEB config and 3 MUX.

13 analog wafers and 20 digital wafers will be needed for a total cost of 350 k$. It should be noted that this cost is similar to the cost which was allocated for COTS.

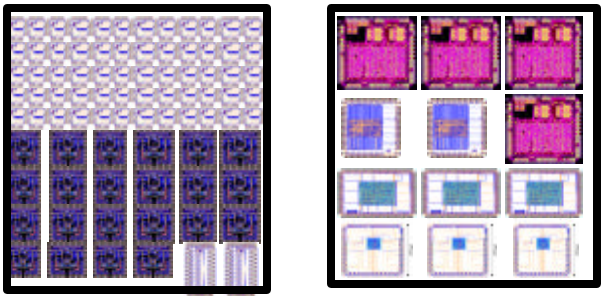


Figure 11*: layout of the analog and digital shared DMILL wafers*

5. CONCLUSION

Ten new DMILL chips have been designed and tested in 2000-2001. All of them are now final and ready for production in 2002. Shared wafers will be used to reduce the production costs.

Seven of these chips are purely digital and exhibit a yield above 70% for an area between 20 and 80 mm^2. Two of these chips have a DSM alternative (SCAC and gain selector) which are also ready and working satisfactorily. The choice will be made in October 2001.

Three chips are analog. Their yield is also larger than 70% and their electrical performance is very good, similar to what was prototyped in AMS 0.8 µm BiCMOS.

The engineering run of the analog pipeline (SCA) has been produced and tested successfully with a yield of 65%. The full production (200 wafers) will be launched at the end of 2001.

6. ACKNOWLEDGEMENTS

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Chip	Area (mm^2)	Number needed	OK/tested	Yield (%)
SCA	30	54 400	1643/2500	65
SCA contr.	80	3 300	28/40	70
Gain select	21	13 300	27/29	9 3
FEB config	20	3 300	37/40	93
MUX	18	1 650	15/17	88
SPAC slave	27	2 500	17/18	94
Opamp	3	17 000	26/37	70
DAC	6.3	130	18/19	94
Calib logic	16	700	8/10	80
BiMUX	4.6	8 320	65/80	81

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