PLENARY

P11 - LHC Physics Goals explained for Engineers
Paris Sphicas

P12 - LHC Beam Instrumentation Detectors and Acquisition Systems

Rhodri Jones
CERN, Geneva, Switzerland

Abstract

This talk will aim to give an overview of some of the detectors and acquisition systems being developed for measuring and controlling beam parameters at the LHC. The two largest systems concern the measurement of beam position, with over 1000 pick-ups, and beam loss, with over 3000 ionisation chambers. For the beam position system a novel wide band time normaliser has been developed to allow bunch-by-bunch 40MHz acquisitions with a dynamic range of ~34dB and an overall linearity of better than 1%.

Also mentioned will be the development of CdTe detectors for luminosity monitoring, beam synchronous timing, fast current transformers and some techniques for measuring the beam size and emittance.

P13 - Trends in microelectrics and nanoelectronics and their impact on HEP instrumentation

Pierre Jarron
CERN, Geneva, Switzerland

Abstract

Abstract Microelectronics is the key technology that has made possible the construction of the electronics instrumentation for the LHC experiments. For example, deep sub micron CMOS technology has enabled the challenging design requirements for the tracker systems, such as radiation tolerance, low noise figure, low power readout circuits, and very high channel density to be successfully achieved. The semiconductor industry forecasts that CMOS technology will continue its pace of miniaturization towards the nanoscale CMOS regime until 2015 and probably 2020. Beyond this timescale it is thought that nanoelectronics will play an important role. The talk will discuss trends in microelectronics and nanoelectronics and their future impact on particle physics instrumentation.

P14 - Managing for Quality in the Electronics Industry

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Abstract

The quality of electronic products is a combination of numerous attributes, including defect level, reliability, availability, appearance and ease of use. Product developers and manufacturers strive to maximize the performance level for the quality attributes that are most critical for a product's intended applications, while optimizing the overall product quality. This paper will discuss methodologies used to achieve high quality electronic products, and the measurements used to define and distinguish product quality level

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P21 - LHC DAQ Systems

Sergio Cittolin
CERN, Geneva, Switzerland

P22 - First-level trigger systems at LHC

Nick Ellis
CERN, Geneva, Switzerland

Abstract

The speaker will discuss some of the challenges of first-level trigger systems in the LHC experiments. The first part of the talk will cover analysis of the requirements from the physics and technical points of view, including the need to make decisions with a latency of a few microseconds compatible with the length of pipeline memories in the front-end electronics. This will be followed by a discussion of the techniques that are used, illustrated by some examples from the LHC experiments.

P31 - Summary of the JCOP Workshop III

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Abstract

The Joint Controls Project (JCOP) is a collaboration between the four LHC experiments and CERN support groups to provide common components for the development of the experiment Detector Control Systems (DCS). A third JCOP workshop took place in June of this year and is summarised in this paper. In particular, it will concentrate on the deliverables foreseen to be provided for JCOP (supported technologies and components), the status of these and the experience gained with them as reported at the workshop. Finally, it will conclude will an overview of the future direction of JCOP.

P32 - Radiation Assurance of LHC electronics

Martin Dentan
Saclay, France

P41 - LHC Machine and Experiment Interface Issues

Emmanuel Tsesmelis
CERN, Geneva, Switzerland

Abstract

This talk will provide an overview of issues arising at the interface between the LHC machine and the experiments, which are required for guiding the interaction between the collider and the experiments when operation of the LHC commences. In particular, an analysis of signals and parameters to be exchanged between the experiments and the accelerator will be presented. Emphasis will be placed on observables that can provide a measure of the LHC machine operating conditions for the experiments, and that can be used by the experiments to give feedback to the machine operation as well as to protect their detectors against damage from spurious operating conditions of the machine.

P42 - Grounding and Shielding Techniques for Large Scale Experiments

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Abstract

The DZero detector at Fermilab has shown excellent common mode noise performance. The common mode noise for the calorimeter in run 1 was unmeasurable and thus was more than 100 db down form the maximum signal level. The silicon detector common mode signal to noise ratio is 24 to 1 or about the equivalent of 1000 electrons. This talk will discuss design techniques to achieve good noise performance on large detectors and will use examples from Dzero. In addition, we have been studying the electrical properties of carbon fiber composite materials for the run 2b silicon detector. The talk will present some ideas for grounding and shielding detectors using carbon fiber structures and will show the results from prototype structures that we have built.

P51 - Timing Distribution at the LHC

Bruce Taylor
CERN, Geneva, Switzerland
for the RD12 Collaboration

Abstract

This paper describes a unified approach to fast timing distribution at the LHC. The timing signals for each ring of the machine will be encoded and transmitted over optical links from the RF generators to the PCR, where beam-synchronous messages will be added. High power laser transmitters will then broadcast the signals over singlemode optical fibres to the four LHC experiments, to the test beam areas, and to the beam instrumentation located around the LHC ring and on the SPS transfer lines. At the experiment areas, trigger information and local synchronous commands and data will be added. The regenerated signals will then be broadcast over multimode passive optical networks to several thousand destinations.

P52 - Distributed Processors allow revolutionary Hardware / Software partitioning

Jean-Louis. Brelet

Jean-Reynald & Jean-Louis Brelet

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Abstract

Future system designs will use, in addition to traditional embedded processors, innovative approaches based on flexible distributed processors, enabled by digital programmable logic devices like complex FPGA's.

The complexity of many of today's system architectures can be likened to that of highly integrated microelectronic chip design. Traditional system partitioning is generally done at the early stage of system architecture, by defining the tasks to be implemented on the embedded processor(s), and the tasks to be designed on the hardware.

Evolution of system-on-chip, or integration of an application in one of few devices becomes a revolution when the technology enables innovative system architectures. The key to this new approach is high-bandwidth communications between distributed processors, and a flexible hardware / software partitioning which can be adapted to the evolution of the system in real time, and during the complete product life cycle.

This study targets the Xilinx Virtex-II Pro™ platform FPGA, and is illustrated by comparative examples of hardware or software implementation. Another example shows how distributed processors can optimize interrupts management.

P53 - Technology Transfer

Roberto Amendolia
CERN, Geneva, Switzerland

P54 - Trends in High-speed Low-power Analog-to-Digital Converters

Laurent Dugoujon
STMicroelectronics
Grenoble

Abstract

After a brief summary of Data-Converters State-of-the-Art, the author will describe the different technological limitations against higher performance. The talk will focus on High Speed Data-Converters with 10 to 14-bit resolution. Implementation as stand-alone device or as System On Chip will be discussed. Special emphasis will be given to POWER consumption performances as well as DENSITY of integration in line with the HEP applications needs. Next five years improvments vision in this field will be proposed with already established Silicon Industry roadmap and advanced R&D results.

SESSION A

A 11 - Realization and test of a 0.25μm Rad-Hard chip for ALICE ITS data acquisition chain

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Abstract

CARLOS2 is a second version of a chip that is part of the data acquisition chain for the ALICE ITS experiment. The first version of the chip has been implemented on Alcatel 0.35μm CMOS digital technology and included 8 8-bit channels. Conversely this second version deals just with two 8-bit channels to increase fault-tolerance during future tests and actual data acquisition. Moreover this version has been implemented using the CERN developed digital library of enclosed gate transistors. This is a rad-hard library developed within RD49 project. The prototype works well and it is going to be applied for ALICE ITS 2002 test beams.

A 12 - Fast CMOS Transimpedance Amplifier and Comparator circuit for readout of silicon strip detectors at LHC experiments

J. Kaplon[1], W. Dabrowski[2], J. Bernabeu[3]
[1] CERN, 1211 Geneva 23, Switzerland
[2] Faculty of Physics and Nuclear Techniques, UMM, Krakow, Poland
[3] IFIC, Valencia, Spain

Abstract

We present a 64-channel front-end amplifier/comparator test chip optimized for readout of silicon strip detectors at LHC experiments. The chip has been implemented in radiation tolerant IBM 0.25 technology. Optimisation of the front-end amplifier and critical design issues are discussed. The performance of the chip has been evaluated in detail before and after X-ray irradiation and the results are presented in the paper. The basic electrical parameters of the front-end chip like shaping time, noise and comparator matching meet the requirements for fast binary readout of long silicon strips in the LHC experiments.

A 13 - OTIS - A TDC for the LHCb Outer Tracker

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Tel: 06221/544357
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http://wwwasic.kip.uni-heidelberg.de/lhcbot/about.html

Abstract

For the outer tracker of the LHCb experiment the OTIS chip is developed. A first full-scale prototype of this 32 channel TDC has been submitted in April 2002 in a standard 0.25um CMOS process.
Within the clock driven architecture of the chip a DLL provides the reference for the drift time measurement. The drift time data of every channel is stored in the pipelined memory until a trigger decission arrives. A control unit provides memory management and handles data transmission to the subsequent DAQ stage.
This talk will introduce the design of the OTIS chip and will present first test results.

A21 - The ATLAS Pixelchip FEI in Deepsubmicron Technology

Ivan Peric,
Bonn University (for the ATLAS pixel collaboration)

Abstract

The new front end chip for the ATLAS Pixel detector has been implemented in a 0.25 um technology. Special layout rules have been applied in order to achieve radiation hardness. In this talk, we present the architecture of the chip and results of laboratory and test beam measurements as well as the performance after irradiation.

A22 - DTMROC-S : Deep submicron version of the readout chip for the TRT detector in ATLAS

F. Anghinolfi**,** CERN, Geneva (Switzerland)
V. Ryjov, JINR, Moscow (Russia) and University of Lund, Lund (Sweden)
R. Szczygiel, CERN, Geneva (Switzerland) and INP, Cracow (Poland)
R. Van Berg, N. Dressnandt, P.T. Keener, F.M. Newcomer, H.H. Williams
University of Pennsylvania, Philadelphia (USA)
T. Akesson, P. Eerola, University of Lund, Lund (Sweden)

Abstract

A new version of the circuit for the readout of the ATLAS straw tube detector (TRT) has been developed in a deep-submicron process. The DTMROC-S is designed in a standard 0.25μm CMOS with a library hardened by layout techniques. Compared to the previous version of the chip done in a 0.8μm radiation-hard CMOS, the much larger number of gates available per unit area in the 0.25um technology enables the inclusion of many more elements intended to improve the robustness and testability of the design. These include: SEU- resistant triple vote logic registers with auto correction; parity bits; clock phase recovery; built-in self tests; JTAG; and internal voltage measurement. The functionality of the chip and the characteristics of newly developed analogue elements such as 8-bit linear DAC, 0.5ns resolution DLL, and ternary current receiver, will be presented.

A23 - System Performance of ATLAS SCT Detector Modules

Peter W. Phillips
CCLRC Rutherford Appleton Laboratory
Representing the ATLAS SCT collaboration

Abstract

The ATLAS Semiconductor Tracker (SCT) will be an assembly of silicon microstrip detector modules on a large scale, comprising 2112 barrel modules mounted onto four concentric barrels of length 1.6m and up to 1m diameter, and 1976 endcap modules supported by a series of 9 wheels at each end of the barrel region. To verify the system design a "system test" has been established at CERN.
This paper gives a brief overview of the SCT, highlighting the electrical performance of assemblies of modules studied at the system test. The off detector electronics and software used throughout these studies is described.

A 24 - Development of the Inner Tracker Detector Electronics for LHCb

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Abstract

For the LHCb Inner Tracker, 300 æm thick silicon strip sensors have been chosen as baseline technology. To save readout channels, strip pitch was chosen to be as large as possible while keeping a moderate spatial resolution. Additional major design criteria were fast shaping time of the readout frontend and a large radiation length of the complete detector.
This paper describes the development and testing of the Inner Tracker detector modules including the silicon sensors and the electronic readout hybrid with the BEETLE frontend chip.
Testbeam measurements on the sensor performance including signal-to-noise, signal pulseshape and efficiency are discussed. We also present performance studies on the digital optical transmission line.
The LHCb experiment is a high performance single arm spectrometer dedicated for studies of B-meson decays. Therefore, precise momentum and tracking resolution at high luminosities are essential. In order to cope with the high track densities in the region surrounding the beam pipe, the tracking detector has been divided in two technologies: straw tubes for the outer part with low particle flux and an Inner Tracker part consisting of silicon strip detectors. Silicon has been chosen because of its optimal performance under high particle fluxes. In order to save readout channels, the strip pitch should be as large as possible.
In the present design, a single silicon ladder with a maximum length of 22 cm as basic unit of one tracking station consists of the structural support made of heat conductive carbon fiber carrying the sensors. Also mounted on the ladder is an electronic readout hybrid together with a pitch adaptor. The multi-layered ceramic hybrid carries three BEETLE readout chips (developed by the ASIC laboratory of the University of Heidelberg) with a total of 384 channels.
In order to prevent pile-up from consecutive bunchcrossings, the shaping time of the BEETLE has been designed to 25ns.
For minimizing the amount of material and therefore improving the radiation length of a tracking station, the analog multiplexed data from one tracking station is transferred to a supporting module located on the Outer Tracker frame, where the on-detector digitization and multiplexing (with the CERN GOL chip) of the digital data is performed. By doing so, we extend the radiation limits as well as spatial and thermal restrictions which would be present when mounting components directly at the sensor inside the LHCb detector's acceptance.

For the long distance transmission to the electronics area, a commercial multi-fiber optical transmitter/receiver will be used together with a 12-fiber optical cable. A commercial demultiplexer plus one FPGA per fiber will then provide 8 bit data for 128 channels each. Calculated with a L1 trigger rate of 1 MHz, this corresponds to a total net data rate of just over 1 GBit/s per BEETLE chip.
This paper presents measurements on the full-size silicon ladder including signal-to-noise and signal pulseshapes. Data was taken during the last testbeam period in Summer 2002.
As this prototype sensor is equipped with multiple geometries, the influence of the width-to-pitch ratio of the strips is studied in detail.
A comparison of detection efficiencies of the 240µm pitch to a smaller pitch is also included, as part of the prototype sensor has been fabricated with a pitch of 200µm. For the optical link, transmission quality and stability has been evaluated under different conditions including additional optical attenuation.

A25 - Digital optical links for control of the CMS Tracker

K. Gill, G. Cervelli, F. Faccio, R. Grabit, A. Sandvik, J.Troska and F.Vasey.
CERN.
G. Dewhirst
Imperial College, London.

Abstract
The digital optical link system for the CMS Tracker is essentially a 2+2 way bi-directional system with two primary functions: to transmit the 40MHz LHC clock and CMS Level 1 Trigger to the Tracker and to communicate control commands that allow the setup and monitoring of the Tracker front-end ASICs.
The specifications of the system are outlined and the architecture and implementation is described from the scale of the components up to the level of the full optical links, including their intended operation in the CMS Tracker.
The performance and radiation hardness of the various individual components is examined. Results of tests of complete prototype digital optical links, based on the intended final components, including front-end digital optohybrids made at CERN, are presented.

A26 - Results of early phase of series production of ATLAS SCT barrel hybrids and modules

Y.Ikegami, KEK (representing ATLAS SCT barrel clusters)

Abstract

A status of early series production of the barrel hybrids and modules of the ATLAS Semiconductor Tracker (SCT) is reported. The manufactures of 48 hybrids and 30 modules were completed in Japan cluster by April 30 and other clusters are expected to

follow soon. Quality assurance tests were performed for all hybrids, including a 100-hours-burn-in test. Bad channel appearance was found to be less than 1%. There was very little increase in the defective channel after the 100-hours-burn-in test. Results from the quality assurance tests for hybrids and modules are described in detail.

A27 - Performance of the Beetle Readout Chip for LHCb

Niels van Bakel, Martin van Beuzekom, Jo van den Brand, Eddy Jans, Sander Klous,
Hans Verkooijen (NIKHEF / Free University Amsterdam)
Daniel Baumeister, Werner Hofmann, Karl-Tasso Knoepfle, Sven Loechner,
Michael Schmelling (Max-Planck Institute for Nuclear Physics Heidelberg)
Neville Harnew, Nigel Smale (University of Oxford)
Ulrich Trunk (Physics Institute, University of Heidelberg)
Edgar Sexauer (now at Dialog Semiconductor GmbH, Kirchheim/Teck-Nabern)
Martin Feuerstack-Raible (now at Fujitsu Mikroelektronik GmbH, Dreieich-Buchschlag)

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Abstract

The Beetle is a 128 channel pipelined front end chip developedin 0.25 um standard CMOS technology for the LHCb experiment.After intensive testing of the current version (Beetle1.1) an improved design (Beetle1.2), which is hardened against Single Event Upsets (SEU) has been submitted in April 2002. The key measurements on the Beetle1.1, which mainly drove the design changes for the Beetle1.2, are described together with the SEU robustness concept. First performance measurements with the new readout chip are shown.

A28 - Design and Performance of the CMS Pixel Readout Chip

Hans-Christian Kaestli
Paul Scherrer Institut, Switzerland

Abstract

Readout chips for pixel detectors at LHC are exposed to enormeous fluence rates that are in the range of 2*10^7 particles per second and cm^2. The architecture of a pixel readout chip must be chosen such, to have minimal data losses even at these enormous data rates.

The CMS pixel readout chips is based on a Column Drain Architecture that should have the necessary performance. We present the design and measured performance of the final CMS pixel chip in DMILL technology. The measurements in a high rate LHC-like testbeam will be shown, where the data losses of a bump-bonded pixel chip as a function of particle fluence has been studied.

A29 - Results from the first CMS Tracker System Test

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Abstract

The CMS Tracker has entered its construction phase. The first rod in its final configuration has been built. A complete series of tests has been performed either in the laboratory and in beam tests on the separate modules before assembling them in the rod. The functionality of the whole system, (readout, control, data acquisition) has been tested carefully both on the hardware and software point of view, the hardware architecture being in its final version and the software architecture very close to the final one. The most relevant tests and results are shown here.

A31 - Test and Evaluation of HAL25: the ALICE SSD Front-End Read-Out Chip

Christine HU
Christine Hu [huch@lepsi.in2p3.fr]

Abstract

The HAL25 is a mixed low noise, low power consumption and radtol ASIC intended for read-out of Silicon Strip Detectors (SSD) in the ALICE tracker. It is designed in a 0.25 micron CMOS process.
The chip contains 128 channels of preamplifier, shaper and a capacitor to store the charge collected on a detector strip. The analogue data is held by an external logic signal and can be serially read out through an analogue multiplexer. A slow control mechanism based on JTAG protocol was implemented for a programmable bias generator, an internal calibration system and selection of functional modes

A32 - Status Report of the ATLAS SCT Optical Links

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Abstract

The readout of the ATLAS SCT and Pixel detectors will use optical links, assembled into harnesses. The final design for the on-detector components in the barrel SCT opto-harness is reviewed. The assembly procedures and test results of the pre-series opto-harnesses are summarised. The mechanical and electrical QA that will be used in production are explained. First results are given for the new 12 way VCSEL and PIN arrays to be used for the off-detector opto-electronics. The design of the off-detector ASICs is described and test results from the production wafers are given.

A33 - Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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Abstract

We have developed two prototype radiation-hard ASICs for optical data transmission in the ATLAS pixel detector at the LHC: a driver chip for a Vertical Cavity Surface Emitting Laser (VCSEL) diode for 80 Mb/s data transmission from the detector, and a Bi-Phase Mark decoder chip to recover the control data and 40 MHz clock received optically by a PIN diode. We have successfully implemented both ASICs in 0.25 micron CMOS technology using enclosed layout transistors and guard rings for increased radiation hardness. We present results from recent prototype circuits and from irradiation studies with 24 GeV protons up to 50 Mrad.

A41 - Aluminium microcable technology for fhe ALICE silicon strip detector: a status report

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M.J. Oinonen, Z. Radivojevic
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Abstract

All interconnections in the ALICE Inner Tracker Silicon Strip Layers are realised using kapton/aluminium microcables. The major advantages are the reduction in material budget and the increased mechanical flexibility as compared to traditional wirebonding. Since the last reports (Snowmass LHC workshop '99) considerable progress has been made and designs have been refined and adapted to facilitate production, which will start end of this year.
This paper describes the design of the 3 major interconnection parts:
-the TAB-frame chipcables, which connect the front-end chips to the detector and to the flex.
These cables are mounted in carrier frames for testing and have unique coding to identify cable type as well as coding to check correct alignment in the test connector.
-the flex, which is essentially a multi-layer interconnecting bus supplying power and control to the front-end chips, with integrated LVDS terminating resistors. The flex is the constructive basis of the hybrid, SMD components can be mounted by soldering or gluing as well as by means of TAB bonding. Ultrasonic bonding and pulsed-bar reflow soldering techniques are used to interconnect the flex to the other parts.
-the laddercable, a 60 cm. long cable connecting the front-end modules to the endcaps. This flatcable is designed as a differential stripline for analog and LVDS signals using ultra-low density polyimide foam as spacer material.
Optical and electrical testing of microcables and scanning techniques to inspect TAB-bonding connections are also discussed.

A42 - High Rate Photon Irradiation Test of an 8-Plane TRT Endcap Sector Prototype

Juan Valls
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ATLAS TRT detector

Abstract

In this document we report the results from a high rate photon irradiation test of an 8-plane TRT endcap sector prototype with 192 straws instrumented with near to final front-end electronics. Data was taken at the CERN X5 Gamma Irradiation Facility with a ^{137}Cs photon source and at the Weizmann Institute irradiation facility in Israel with a Gammabeam 150 ^{60}Co source. Results on the performance of the straws are presented in terms of occupancies and noise rates at high counting rates, cross-talk studies between straws, and test pulse hit efficiencies under irradiation.

A43 - The Effect of Highly Ionising Events on the APV25 Readout Chip

R. Bainbridge
Imperial College, London
on behalf of the CMS Tracker collaboration.

Abstract

Highly ionising particles, produced in inelastic hadronic interactions in silicon detectors, can result in large energy depositions and measurable deadtime in all 128 channels of the CMS Tracker APV25 readout chip. The mechanism by which all channels experience deadtime has been understood to be linked to the powering scheme of an inverter stage. An analysis of beam test data has provided measurements of the probability of observing deadtime following a highly ionising event. Laboratory studies have shown that through a suitable choice of an external resistor on the front-end hybrid, the deadtime can be significantly reduced and the effect, in terms of signal loss, is negligible.

A44 - Readout Control Unit of the Front End Electronics of the Time Projection Chamber in ALICE

Presented by Jørgen Lien, Høgskolen i Bergen / Universitetet i Bergen / CERN

Authors: Håvard Helstrup - Høgskolen i Bergen; Dieter Röhrich, Kjetil Ullaland, Anders S. Vestbø - Universitetet i Bergen; Bernhard Skaali, David Wormald - Universitetet i Oslo; Luciano Musa - CERN
for the ALICE Collaboration.

Abstract

The unit is designed to control and monitor the front-end electronics of the ALICE Time Projection Chamber, and to collect the data and ship them onto the Detector Data Link (optical fiber).
Handling and distribution of the central trigger are also performed, using the on board mounted TTCrx chip. Interfacing with the Detector Control System is done via a separate Slow Control bus.
For the prototype of the RCU the Altera EP20K400 FPGA has been used for application specific system integration.

A45 - The Alice Silicon Pixel Detector Readout System – Moving Towards System Integration

Roberto Dinapoli, for the Alice Collaboration

Abstract

A number of key components have been designed, produced and tested for the readout system of the Alice Silicon Pixel Detector (SPD). The SPD consists of 240 detector ladders each of which is bump-bonded to 5 Alice1LHCb pixel readout chips. Two ladders form a half-stave and sixty staves, each consisting of two half-staves, are mounted in two concentric barrels around the interaction region. Each half stave is equipped with a Multi Chip Module (MCM), which hosts three different ASIC chips: one for the biasing of the Alice1LHCb chip and for temperature monitoring, one for digital read-out and one for data transmission. The chips were designed at CERN in a commercial 0.25μm CMOS process using radiation tolerant layout techniques. This presentation gives an overview of the system, describes the results obtained from the individual components as well as the software and hardware of the Data Acquisition System.

A46 - Front-End Hybrid for the CMS Silicon Tracker
(Preparation of Industrial Production)

J.D. Berst, U.Goerlach, C. Maazouzi, F. Didierjean, Ph. Grähling

Abstract

A Front-End Hybrid for the readout electronics of the CMS silicon tracker has been developed in two different technologies with the aim of a complete industrial production of the ca. 16000 modules needed for the experiment. We will present the development of the electrical design of the multi-layer board and its implementation in three different technologies: thick-film on ceramic, advanced FR4-PCB and a combined Mixed-Flex Rigid multi-layer structure. We will describe the impact on the design, test results of the

various hybrids fabricated and discuss in particular the possibilities of a cost-effective production in industry.

A47 - Reliability prediction for TFBGA assemblies

Z. Radivojevic, A.Q.Yasir, J. Rantala

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Abstract

One of the key hot topics in dense LSI packaging technologies is to reduce the thermo-mechanical stress caused by a mismatch of coefficients of thermal expansion (CTE) among material employed. Nearly all developers of portable electronics products typically perform several kinds of physical test in development cycle to evaluate reliability/quality of the products. In this work a common thermal ageing tests were replaced by novel so-called power-cycling tests, which are closer to the real electro-thermo-mechanical life of electronics product. More precisely, special thermal test chips of TFBGA168 was designed and made for investigation of die packaging quality/reliability as well as reliability of the functional interconnections. The assembly consisted of an array of polysilicon resistors (active area 36 mm^2) surrounding a sensing diode for precise temperature measurements. The whole assembly was designed to reproduces thermo-mechanical behavior of TFBGA package massively produced by STMicroelectronic [1], the second microelectronics manufacturer in Europe. Both, physical experiments and simulations were carried-out to locate position of critical parts. Complexity of structural package characteristics was simulated by using ANSYS and FLOTHERM software. A strain energy based model was employed to locate the most vulnerable areas in the package and predict mean-time-to-failure (MTF).

A48 - The CCU25: a network oriented Communication and Control Unit integrated circuit in a 0.25 um CMOS technology.

C. Ljuslin, C. Paillard, A. Marchioro
CERN, EP Division 1211 Geneve 23, Switzerland

Abstract

The CCU25 is the core component of a newly developed field bus intended for the slow control, monitoring and timing distribution for the CMS silicon tracker.
As no commercial component could satisfy all requirements of radiation hardness, functionality and electrical properties, a new component has been developed.

Its architecture has been inspired by commercial token-ring type topologies. Each CCU25 contains various types of peripheral controllers and has dual network input and output ports allowing the cabling of a redundant network.
Inside the chip, critical circuitry is tripled and a majority voting scheme is used to cope with errors caused by radiations.
The design was fabricated with a library in rad-tolerant 0.25µm CMOS developed at the CERN it contains 50.000 cells and has 196 I/O pads for a die-size of 6x6mm.
The detailed functionality is described and first prototype usage is reported.

A51 - Embedding deserialisation of LHC experimental data inside Field Programmable Gates Arrays.

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Laboratoire Leprince-Ringuet

Presentation: Thierry ROMANTEAU, Laboratoire Leprince-Ringuet, Ecole Polytechnique, F-91128 Palaiseau cedex, France

Abstract

LHC experiments will make use of thousands of serial links in order to transfer digital data from the electronics sitting in the detectors to the off detector electronics located more than 100 meters away. Due to the high level of radiation present in the detectors CERN designed and developed the Giga Opto Link (GOL) chip, a radiation hard serialiser.
On the contrary the off-detector electronics currently designed for the processing of the digital data as received from the detectors will heavily rely on commercial programmable components like Field Programmable Gate Arrays.
Deserialising the serial data before their processing by the FPGAs will also be done using commercial components. Xilinx company is now offering a new type of FPGAs which embed deserialisers (Virtex2Pro). Using such components will allow more powerfull and compact design of the processing boards of the off-detector electronics. This presentation will describe the results of tests performed for measuring the performance of a complete link made of a GOL chip and a Virtex2Pro circuit.

A52 - High Voltage Power Supply Module Operating in Magnetic Field

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Abstract

The article describes a high voltage power supply module which can work efficiently under a magnetic field of 1.5 tesla. The module incorporates a piezoelectric ceramic transformer. The module includes feedback to stabilize the output voltage, supplying from 2000V to 4000V to a load of more than 10 megohm at an efficiency of higher than 60 percent. The module provides interface so that a micro-controller chip can control the module. The chip can set the output high voltage, detects the short circuit of the output high voltage and control its recovery. The chip can also monitor the output current. Most functions of the module are brought under the control of the chip. The module will be soon commercially available from a Japanese manufacturer.

A53 - Electromagnetic Compatibility Test for CMS experiment.

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Abstract

Electromagnetic compatibility (EMC) is concerned with the generation, transmission and reception of electromagnetic energy. These three aspects form the basic framework of any EMC design.

CMS experiment is a very complex system. Millions of low-cost acquisition channels using very low-level signals have to work inside magnets and under radiation. This front-end electronics constitutes the sensitive receptor in the EMC model.
Noise can be coupled to the sensitive electronics through conductive or radiation paths. The former constitutes the most important coupling mechanism and some EMC tests are necessary to qualify the immunity of the different parts of the front-end electronics. Sets

of tests to measure the common mode noise and differential mode noise sensitivities of the front-end electronics are described. Also test to measure the immunity to transient perturbations are included. These tests are of major importance to define a map of electromagnetic (EM) emission and susceptibilities to integrate the detector in a safe way.

A61 - Progress in Radiation and Magnetic Field tests of CAEN HV and LV boards

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Abstract

A new HV and LV sub-assembled device for design evaluations has been tested in radiation and magnetic field. Results of the proton beam tests performed in Louvain-la-Neuve and magnetic field tests performed at CERN are presented. Comparisons with older tests confirm the same behavior in a harsh environment. The HV and LV boards have succesfully passed the scheduled tests and can be a good candidate for several LHC experiments.

A62 - Noise immunity analysis of the Forward Hadron Calorimeter Front-end electronics.

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Abstract

The Very Forward Hadron Calorimeter (HF) in CMS is composed by about 3000 photo-multipliers (PMT) arranged in boxes housing 30 PMTs each one. Read-out amplifiers are arranged in 6 channel daughter cards located about 4 meters from the PMTs. Shielded cables are used to connect the PMT anode signal to the amplifiers.
This paper addresses the study of the immunity to common mode spurious signal and external fields of the electronic system described above. It allows predicting grounding and shielding problems and estimating the effect of interference noise at early stages of the design.

A63 - A Common 400Hz AC power supply distribution system for CMS front-end electronics

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Abstract

A 400Hz AC system is proposed to distribute power to all CMS sub-detectors. It distributes high voltage from the counting room to the periphery of the detector using a 208V three-phase system. On the detector, three phase step-down transformers, in conjunction with rectifiers and inductive-capacitive filters in the secondary, transform the high AC voltage to appropriated DC low voltages. These units have to operate in a harsh environment with magnetic field and neutron radiation.

This paper describes the proposed power distribution system, its topology and components and the characteristics that should present each element to be compatible with standards, radiation and magnetic tolerance. Special attention is paid in the analysis and design of the transformer operating in magnetic field.

A64 - A flexible stand-alone testbench for characterizing the front-end electronics for the CMS Preshower detector under LHC-like timing conditions

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Abstract

A flexible test system for simulating LHC-like timing conditions for evaluating the CMS Preshower front-end electronics (PACE-II, designed in DMILL 0.8micron BiCMOS) has been built using off-the-shelf components. The system incorporates a microcontroller and an FPGA, and is controlled via a standard RS232 link by a PC running LabView. The system has been used to measure the digital functionality and analogue performance, including timing, noise and dynamic range, on about 100 PACE-II samples. The system has also been used in a beam test of Preshower silicon sensors, and may be viewed as a prototype for the final evaluation system of ~5000 PACE.

A65 - Production Testing of ATLAS Muon ASDs

John Oliver, Matthew Nudell : Harvard University
Eric Hazen, Christoph Posch : Boston University

Abstract

A production test facility for testing up to sixty thousand octal Amp/Shaper/Discriminator chips (MDT-ASDs) for the ATLAS Muon Precision Chambers will be presented. These devices, packaged in 64 pin TQFPs, are to be mounted onto 24 channel front end cards residing directly on the chambers. High expected yield and low packaging cost indicates that wafer level testing is unnecessary. Packaged devices will be tested on a compact, FPGA based Chip Tester built specifically for this chip. The Chip Tester will perform DC measurements, digital i/o functional test, and dynamic tests on each MDT-ASD in just a few seconds per device. Functionality and architecture of this Chip Tester will be described.

A66 - MASS PRODUCTION TESTING OF THE ANODE FRONT-END ELECTRONICS FOR THE CMS ENDCAP MUON CATHODE STRIP CHAMBERS

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Abstract

Results are reported on the mass production testing of the anode front-end preamplifiers and boards (AFEB), and their associated delay-control ASICs for the CMS Endcap Muon Cathode Strip Chambers. A special set of test equipment, techniques and corresponding software were developed and used to provide the following steps in the test procedure: (a) selection of the preamplifier/shaper/discriminator ASICs for the AFEBs, (b) test of the functionality of the assembled AFEBs at the factory. (c) an AFEB burn-in test, (d) final certification tests of the AFEBs, and (e) the certification test of the delay-control ASICs.

A67 - APV25 production testing and quality assurance

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Abstract

The APV25 is the 128 channel chip for silicon tracker readout in CMS. The production phase is now underway, and sufficient wafers produced to allow significant conclusions to be reached on yield and performance based on data acquired during the wafer probing phase. The wafer probe tests are described and results used to make comparisons between chips, wafers and wafer lots. Chips sampled from wafers after dicing are mounted in a custom setup enabling more detailed QA performance measurements, and some of these are also irradiated to confirm radiation hardness. Details of measurements and results are presented.

SESSION B

B11 - The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI)

N. Ellis, P. Farthouat, K. Nagano, G. Schuler, C. Schwick, R. Spiwoks, T. Wengler

Abstract

The Level-1 Muon to Central Trigger Processor Interface (MUCTPI) receives trigger information synchronously with the 40 MHz LHC clock from all trigger sectors of the muon trigger. The MUCTPI combines the information and calculates total multiplicity values for each of six programmable pT thresholds. It avoids double counting of single muons by taking into account the fact that some muons cross more than one sector.
The MUCTPI sends the multiplicity values to the Central Trigger Processor which takes the final Level-1 decision. For every Level-1 Accept the MUCTPI also sends region-of-interest information to the Level-2 trigger and event data to the data acquisition system. Results will be presented on the functionality and performance of a demonstrator of the MUCTPI in full-system stand-alone tests and in several integration tests with other elements of the trigger and data acquisition system. Lessons learned from the demonstrator will be discussed along with plans for the final system.

B12 - Tests of CMS regional calorimeter Trigger prototypes

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Abstract

The CMS regional calorimeter trigger system detects signatures of electrons/photons, taus, jets, and missing and total transverse energy in a deadtimeless pipelined architecture. It uses a Receiver Card, with four gigabit copper cable receiver/deserializers on mezzanine cards, that deskews, linearizes, sums and transmits data on a 160 MHz backplane to an electron isolation card which identifies electrons and a jet/summary card that sums energies. Most of the processing is done on five high-speed custom ASICs. Results from testing the prototypes of this system, including serial link bit error rates, data synchronization and throughput measurements, and ASIC evaluation will be presented.

B13 - An Implementation of the Sector Logic for the Endcap Level-1 Muon Trigger of the ATLAS Experiment

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Abstract

We present development of the Sector Logic for endcap Level-1 (LVL1) muon trigger of the ATLAS experiment. The Sector Logic reconstructs tracks by combining R-Phi information from the TGC detectors and chooses two highest transverse momentum (pT) tracks in each trigger sector. The module is designed in single pipelined structure to achieve operation with no dead time and shorter latency. LUTs (Look-Up Table) method is used so that pT threshold levels can be variable. To meet these requirements, we adopt FPGA devices for implementation of the prototype. The design and results of performance tests of the prototype are given in this presentation

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B21 - Results of a Sliced System Test for the ATLAS End-cap Muon Level-1 Trigger

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Abstract

The sliced system of the ATLAS end-cap muon level 1 trigger consists of 256 inputs. It completes almost entire functionalities required for the final system. The six prototype custom chips (ASICs) with the full specification are implemented in the system. The structure and partitioning are also conformed to the final design. With this sliced system, we have made validity check of the design, performance test and long run tests for both the trigger and readout parts in detail. We report the outline of the sliced system along with the final design concept, and present results of the system test and discuss possible improvements in the final system.

B22 - Level 0 trigger decision unit for the LHCb experiment

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Abstract

This note describes a proposal for the Level 0 Decision Unit (L0DU)
of LHCb. The purpose of this unit is to compute the L0 trigger decision by using information of L0 sub-triggers. For that, the L0 Decision Unit (L0DU) receives information from L0 calorimeter, L0 muon and L0 pile-up sub-triggers, with a fixed latency, at 40 MHz. Then, a physical algorithm is applied to give the trigger decision and a L1 block data is constructed. The L0DU is built to be flexible : downscaling of L0 trigger condition, change conditions of decision (algorithm, parameters, ...) and monitoring are possible due to the 40 MHz fully synchronous \fpga based design.

B23 - Pile-Up Veto L0 Trigger System for LHCb using large FPGA's

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Abstract

A zero-level trigger system for detecting multiple events in a bunch crossing is in development. The fraction of multiple events is high and a veto on them frees bandwidth for lowering cuts of zero-level hadronic triggers. The detection is performed by histogramming hit combinations of 2 dedicated Silicon-detector planes and selecting vertex peaks using Mgate Xilinx FPGA's. Details of the logic and further implementation are given in the presentation.

B25 - Prototype Cluster Processor Module for the ATLAS Level-1 Calorimeter Trigger

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Abstract

The Level-1 Calorimeter Trigger consists of a Preprocessor, a Cluster Processor (CP), and a Jet/Energy-sum Processor (JEP). The CP and JEP receive digitised trigger-tower data from the Preprocessor and produce trigger multiplicity and region-of-interest (RoI) information. The CP Modules (CPM) are designed to find isolated electron/photon and hadron/tau clusters in overlapping windows of trigger towers. Each pipelined CPM processes a total of 280 trigger towers of 8-bit length at a clock speed of 40 MHz. This huge I/O rate is achieved by serialising and multiplexing the input data. Large FPGA devices have been used to retrieve data and perform the cluster-finding algorithm. A full-specification prototype module has been built and tested, and first results will be presented.

B26 - The Design of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger

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Abstract

The ATLAS level-1 muon trigger in the barrel region identifies candidate muon tracks within a programmable transverse momentum range. A system of seven Resistive Plate Chamber detector concentric layers provides the hit information in the bending and non-bending projection. A coincidence of hit in the detector layers within a programmable road is required to generate a trigger signal. The width of the track road in the detector is used to select the transverse momentum cut to be applied.
The Coincidence Matrix ASIC provides the core logic of the trigger on-detector electronics. Both the trigger algorithm and the detector readout logic are implemented in

this chip. Each CMA is able to process 192 RPC signals coming from up to four different detector layers. Most of the CMA logic works at an internal frequency of 320 MHz.
The design and the tested performance of the ASIC are presented.

B27 - The ATLAS readout system of the Liquid Argon Calorimeter

Daniel La Marra, Annie Leger, Guy Perrot, Luc Poggioli, Julie Prast, Imma Riu, Stefan Simion

Abstract

The Readout Driver (ROD) system is a key element of the ATLAS Liquid Argon Calorimeter readout system. It processes a predetermined number of samples of the bipolar output waveform from the calorimeter front-end electronics and precisely determines the energy deposited in each calorimeter cell and the timing of these signals at the Level one trigger output rate of 100 kHz. It applies an optimal filtering algorithm while minimizing the pileup and electronic noise and uses coefficient constants determined from the calibration.
Approximately 200000 channel outputs are processed through the Liquid Argon ROD system. Only their energy, timing and a quality flag are sent to the data acquisition. The impossibility to recover the original data imposes severe reliability requirements to the ROD system.
The system consists of around 200 ROD modules, 200 transition modules and 16 custom-made backplanes. A ROD module receives data from 1024 calorimeter cells through eight 1.6 Gbit/s optical fibers and consists of one mother board with four mezzanine boards (called processing units) which contain two DSPs each. This modular design offers the possibility to use the latest development on DSP technology in the future. Two different DSPs have been tested and the results compared. These results together with the description of the Liquid Argon Calorimeter readout system are presented.

B31 - ATLAS Tile Calorimeter Digitizer-to-Slink Interface

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Abstract

This paper describes the ATLAS Tile Calorimeter Digitizer-to- Slink interface card design, performance and radiation hardness tests and production processes.

A total of about 10,000 channels of a readout system are required for Tile Calorimeter, which are housed in 256 electronics drawers. Each electronics drawer in Tile Calorimeter

has one interface card. It receives optical TTC information and distributes command and clock signals to 8 digitizer boards via LVDS bus lines. In addition, it collects data from 8 digitizer boards in a format of 32-bit word at a rate of 40Mbps. The data of each drawer is aligned, repacked with headers and CRC control fields. It is then subsequently serialized with G-link protocol to be sent out to ROD module via a dual optical G-link at a rate of 640Mbps. The interface card can order the sequence of output channels according to drawer geometry or tower geometry. A master clock can be selected for timing adjustment, either from an on-board clock or from one of the eight DMU clocks to eliminate effects of propagation time delays along the data bus from each digitizer boards.

Since each interface card transports data from an entire electronics drawer, any failure could cause all data loss of an entire drawer. To overcome this hazard, we have incorporated a 2-fold redundant circuit design including optical components. An on-board failure detection circuits automatically selects one of the two TTC receivers. Other redundant functional circuits work in parallel. The destination ROD module makes a decision to take the data from one of two channels based on data qualities and failure conditions.

B32 - FED-kit design for CMS DAQ system

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Abstract

We developed series of modules, collectively referred to as FED-kit, to help design and test the data link between the Front-End Drivers (FED) and the FED readout Link (FRL) modules which act as Event Builder network input module for the CMS experiment.
FED-kit is composed of three modules:
-The Generic III: module is a PCI board which emulates FRL and/or FED. It has 2 connectors to receive the PMC receiver. It has one FPGA which is connected to four busses (SDRAM, Flash, 64-bit 66MHz PCI, IO connectors).
-A PMC transmitter transfers the S-Link 64 IO's coming for FED to a LVDS link via a FPGA.
-A PMC receiver receives up to 2 LVDS links to merge data coming from FED.
The Generic III has a flexible architecture, that it can be used for multiple others applications;Random data generator, FED emulator, Readout Unit Input (RUI), WEB server, etc..

B33 - A Gigabit Ethernet Link Source Card

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Abstract

A Link Source Card (LSC) has been developed which employs Gigabit Ethernet as the physical medium. The LSC is implemented as a mezzanine card compliant with the S-Link specifications, and is intended for use in development of the Region of Interest Builder (RoIB) in the Level 2 Trigger of Atlas. The LSC will be used to bring Region of Interest Fragments from Level 1 Trigger elements to the RoIB, and to transfer compiled Region of Interest Records to Supervisor Processors. The card uses the LSI 8101/8104 Media Access Controller (MAC) and the Agilent HDMP-1636 Transceiver. An Altera 10K50A FPGA is configured to provide several state machines which perform all the tasks on the card, such as formulating the Ethernet header, read/write registers in the MAC, etc. An on-card static RAM provides storage for 512K S-Link words, and a FIFO provides 4K buffering of input S-Link words. The LSC has been tested in a setup where it transfers data to a NIC in the PCI bus of a PC.

B41 - PCI-based Readout Receiver Card in the ALICE DAQ System

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Abstract

The PCI-based readout receiver card (PRORC) is the primary interface between the detector data link (an optical device called DDL) and the front-end computers of the ALICE data-acquisition system. This document describes the architecture of the PRORC hardware and firmware and of the PC software. The board contains a PCI interface circuit and an FPGA. The firmware in the FPGA is responsible for all the concurrent activities of the board, such as reading the DDL and controlling the DMA. The co-operation

between the firmware and the PC software allows autonomous data transfer into the PC memory with little CPU assistance. The system achieves a sustained transfer rate of 100 MB/s, meeting the design specification and the ALICE requirements.

B42 - CMS Data to surface transportation architecture

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Abstract

The front-end electronics of the CMS experiment will be read out in parallel into approximetaly 700 modules which will be located in the underground control room. The data read out will then be transported over a distance of ~200m to the surface control room where they will be received into deep buffers, the "Readout Units". The latter also provide the first step in the CMS event building process, by combining the data from multiple detector data sources into larger-size (~16 kB) data fragments, in anticipation of the second and final event-building step where 64 such sources are merged into a full event. The first stage of the Event Builder, referred to as the Data to Surface (D2S) system is structured in a way to allow for a a modular and scalable DAQ system whose performance can grow with the increasing instantaneous luminosity of the LHC.

B43 - TAGnet, a high rate eventbuilder protocol

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Abstract

TAGnet is a custom, high-rate event scheduling protocol designed for event-coherent data transfers in trigger farms. Its first implementation is in the level-1 VELO trigger system of LHCb where all data sources (Readout Units) need to receive destination addresses for their DMA engines at the
incoming trigger rate (1 MHz). TAGnet organises event-coherency for the source-destination routing and provides the proper timing for best utilization of the network bandwidth. The serial TAGnet LVDS link interconnect all Readout Units in a ring, which is controlled by a TAGnet scheduler. The destination CPU's are situated at the crossings of a 2- dimensional network and memory-mapped through the PCI bus on the Readout Units. Free CPU addresses are queued, sorted and transmitted by TAGnet scheduler, implemented as programmable PCI card with serial LVDS links.
The serial TAGnet LVDS links interconnect all Readout Units (RU) in the LHCb L1 VELO trigger network within a ring configuration, which is controlled by a TAGnet scheduler. The latter provides the proper timing of the transmission and organises event-

coherent transfers from all RU buffers at a destination selection rate of 1 MHz per CPU. In the RU buffers, hit-cluster data are received and queued in increasing event-order. TAGnet allocates the event-number of the oldest event in the RU buffers with a free CPU address and starts the transfer.
Each new TAG is sent in a data packet that includes a transfer command and an identifier of a free CPU in the trigger farm where to transmit the next buffer. The TAG transmission rate is considerably higher than the incoming trigger rate, leaving enough bandwidth for other packets, which may transport purely control or message information. The CPU identifiers are converted within each RU into physical PCI addresses, which map via the shared memory network directly to the destination memory. The DMA engines perform the transfer of hit-clusters from the RU's input buffers to the destination memory. The shared-memory paradigm is established between all destination CPUs and local MCU's (PMC processor card) on the Readout Units. The CPUs and MCU's are interconnected via 667 Mbyte/s SCI ringlets, so that average payloads of 128 bytes can be transferred like writing to memory at frequencies beyond 1 MHz and at transfer latencies on the order of 2-3 us.
The TAGnet format is conceived for scalability and highest reliability for a TAG transmission rate of initially 5 MHz, including also Tags for control and messages. Tags may either be directed to a single slave (RU, or Scheduler) or be accepted by all TAGnet slaves in the ring. A TAG packet consists physically of 3 successive 16-bit words, followed by a 16 bit idle word. A 17^{th} bit is used to flag the 3-words of data from the idle frame. The scheduler generates a permanent sequence of 3 words and 1 idle, therefore this envelope is called the TAGnet "heartbeat" which remains unaltered throughout the ring. Whilst the integrity of the 3 words within a heartbeat is protected by Hamming codes, the integrity of the 17^{th} frame bit is guaranteed by the fixed heartbeat pattern which is in a fixed phase relation between the output and input of the TAGnet scheduler. The TAGnet clock re-transmission at each slave is used as a ring-alive status check for physical TAGnet ring connection layer.
The above described TAGnet event building operates with small payloads (128 byte typically) at 1 MHz and beyond, hence it requires a very low overhead Transport Format. A variant of STF as defined for Readout Units is used which adds only 12 bytes to the full payload transmitted by each RU to a CPU. Included in STF are event numbers and a transfer complete bit which serves as "logical AND" at the destination CPU to start processing when all RU buffers have arrived.

B44 - MROD, the MDT Read Out Driver.

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Abstract

The MROD is the Read Out Driver (ROD) for the ATLAS muon MDT precision chambers. Here is presented the first full scale MROD prototype called MROD-1. The MROD is an intelligent data concentrator/event builder which receives data from six MDT chambers through optical front end links. Event blocks are assembled and subsequently transmitted to the Read Out Buffer (ROB). The maximum throughput is about 1 Gbit/s. The MROD processing includes data integrity checks and the collection of statistics to facilitate immediate data quality assessment. In addition the MROD allows to "spy" on the events. The MROD-1 prototype has been built around Altera APEX FPGAs and ADSP-21160 "SHARC-II" DSPs as major components. Test results will be presented.

B45 - The implementation of the production version of the Front-End Driver card for the CMS silicon tracker readout.

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Abstract

The first boards of the production version of the Front-End Driver (FED) card for the CMS silicon tracker are now being manufactured. The primary function of the FEDs in the tracker readout system are to digitise and zero-suppress the multiplexed data sent on each first level trigger via analogue optical links from on-detector pipeline chips (APV25). This paper outlines the design and describes in detail the implementation of the 96 ADC channel, 9U VME form factor, FED. In total, 450 FEDs will be housed in the counting room to readout the 10 million readout channels of the CMS tracker.

B46 - ROD General Requirements and Present Hardware Solution for the ATLAS TileCalorimeter.

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Abstract

This works describes the general requirements and present hardware solution of the Read Out Driver for the ATLAS Tile Calorimeter. The developments currently under execution include the adaptation and test of the LiAr ROD to TileCal needs and the design and implementation of the PMC board for algorithm testing at ATLAS rates.The adaptation includes a new transition module with 4 SLINK inputs and one output which match the initial TileCal segmentation for RODs. We also describe the work going on in the design of a DSP-based PMC with SLINK input for real time data processing to be used as a test environment for optimal filtering

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B47 - Evolution of S-LINK to PCI interfaces

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(Henryk Niewodniczanski Institute of Nuclear Physics)
Markus Joos, Robert McLaren, Jorgen Petersen, Erik van der Bij
(CERN)

Abstract

S-LINK is an interface specification for a link that can move data at a speed of up to 160 MB/s. In most applications and test systems the data has to be moved to a PCI based computer. An overview of the evolution of S-LINK to PCI interfaces is given. The performance that can be reached with those interfaces in several types of PCs is presented and a description of the FILAR, a future PCI interface with four integrated inputs, is given.

B48 - The Read Out Driver for the ATLAS Muon Endcap trigger and its architectural and design language techniques

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Abstract

The ATLAS Muon Endcap trigger has a hierarchical readout system for 320,000 binary channels. The "Read Out Driver (ROD)", module for each octant collects data via 13 optical links and (1) sends an assembled event via an output S-link to the ATLAS central DAQ, and (2) sends a small sample of the event data via the VMEbus to a commercial VME processor.
A ROD prototype has been implemented based on a single large Xilinx Virtex FPGA. Its design features, implementation details, DAQ software, and current status are described. A procedural language was used as one of the hardware description languages.

B51 - A Configurable Radiation Tolerant Dual-Ported Static RAM macro, designed in a 0.25 µm CMOS technology for applications in the LHC environment.

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Abstract

A configurable dual-port SRAM macro-cell has been developed based on a commercial 0.25 µm CMOS technology. Well-established radiation tolerant layout techniques have been employed in order to achieve the total dose hardness levels required by the LHC experiments. The presented SRAM macro-cell can be used as building block for on-chip readout pipelines, data buffers and FIFOs. The design features synchronous operation with separate address and data busses for the read and write ports, thus allowing the execution of simultaneous read and write operations. The macro-cell is configurable in terms of word counts and bit organization. This means that tiling memory blocks into an array and surrounding it with the relevant peripheral blocks can construct a memory of arbitrary size. Circuit techniques used for achieving macro-cell scalability and low power consumption are presented. To prove the concept of the macro-cell scalability two demonstrator memory chips of different sizes were fabricated and tested. The experimental test results are being reported.

B52 - Overview of the new CMS electromagnetic calorimeter electronics

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Abstract

Since the publication of the CMS ECAL Technical Design Report end of 1997 the ECAL electronics has experienced a major revision in 2002. Extensive use of rad hard technology digital electronics in the front-end allows simplifying the off-detector electronics. The new ECAL electronics system will be described with emphasis on the off-detector sub-system.

B53 - Front-end Electronics for the LHCb preshower

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Abstract

The LHCb preshower detector (PS) is both used to reject the high background of charged pions (part of L0 trigger) and to measure particle energy (part of the electromagnetic calorimeter).
The digital part of the 40 MHz fully synchronous solution developped for the LHCb preshower detector front-end electronics is descibed including digitization. The general design and the main features of the front-end board are recalled. Emphasis is put on the trigger and data processing functionnalities. The PS front-end board handles 64 channels. The raw data dynamic range corresponds to 10 bits, coding energy from 0.1 MIP (1 ADC count) to 100 MIPs while the trigger threshold is set around 5 MIPs.

B61 - A BiCMOS synchronous pulse discriminator for the LHCb calorimeter system.

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Abstract

A monolithic prototype for the analogue readout of the Scintillator Pad Detector (SPD) of the LHCb Calorimeter is presented.. A low power version that works at 3.3 V has been designed using the 0.8 um-BiCMOS technology of AMS. It consists on a charge iscriminator with a dual path structure formed by an integrator, a track and hold, a substractor and a comparator. Each circuit has 8 full channels. The resolution of the system is about 5fC and the bandwidth is 200MHz. The chip also includes a DAC and serial digital control interface to program the threshold of the discriminator. Design, simulation and test results for different version of the circuit will be described.

B62 - Channel Control ASIC for the CMS Hadron Calorimetry Front End Readout Module

Ahmed Boubekeur, Alan Baumbaugh, John Elias, Theresa Shaw, Ray Yarema

Abstract

The Channel Control ASIC (CCA) is used along with a custom Charge Integrator and Encoder (QIE) ASIC to digitize signals from the HPDs and photo multiplier tubes in the CMS hadron calorimeter. The CCA sits between the QIE and the data acquisition system. All signals to and from the QIE pass through the CCA chip. One CCA chip interfaces with two QIE channels. The CCA provides individually delayed clocks to each of the QIE chips in addition to various control signals. The QIE sends digitized PMT or HPD signals and time slice information to the CCA which sends the data to the data acquisition system through an optical link.

B63 - QIE8 for HCAL/CMS v a Non-linear 4 Range Design.

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Presented by Sergey Los

Abstract

Signal readout for the CMS HCAL photo detectors is based on a mixed-signal ASIC, the QIE8. This chip operates at the LHC machine frequency and provides multirange integration and digitization. Implementation of an integrated non-linear FADC with other improvements allowed for significant design optimization. As a result, 4 ranges of integration and a 5-bit ADC have provided the required 13 bits of energy resolution with quantization error matched to the detector resolution. An additional mode boosts sensitivity by a factor of 3 on the most sensitive range, and, when combined with low FADC DNL, allows for ionization source calibration. Operation of the chip is described with emphasis on optimization of the parameters, and results of the first measurements are presented.

B64 - A low-power high dynamic range front-end ASIC for imaging calorimeters

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Abstract

High granularity Sci-Fi calorimeters with shower imaging capabilities require dedicated front-end electronics. The ICON-4CH is a 4 channel input, 12 channel output ASIC designed for use in a multi-anode photomultiplier system with very large dynamic range and low-noise requirements. Each of the four input signals to the ASIC is split equally into three branches by a current conveyor. Each of the three branches is scaled differently: 1:1, 1:8 and 1:80. The integrated signal is read out by a 12 channel low-noise/low power high dynamic range charge sensitive preamplifier-shaper circuit (VA4-PMT chip), with simultaneous sample and hold, multiplexed analog readout, calibration facilities. Tests performed in our lab with a MAPMT are reported in terms of linearity, dynamic range and cross-talk of the system.

B65 - ATLAS/LAR Calibration system

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Abstract

In order to calibrate the ATLAS LAr calorimeters to an accuracy better than 1%, over 16 bits dynamic range, 10 boards with 128 pulse generators have been designed with COTS components and used in test beams for the last 2 years.
The final version requires radiation hard components (low offset amplifiers, DAC, control logic), which have been realized in DMILL technology.
The performance of these chips as well as the measurements of uniformity, linearity, radiation tolerance on a first prototype smaller board are presented.

B66 - Chamber Service Module (CSM1) for MDT.

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Abstract

CSM-1 is the second and latest version of the high speed electronic unit whose primary task is to multiplex serial data from up to 18 ASD/TDC cards located at the ends of the Monitored Drift Tubes. Each CSM will capture data from all 24 channel TDC (AMT-2 units) of a given chamber and transfer it along a single optic fiber to the MROD, the event builder and readout driver. The core of the board is a Xilinx VirtexII FPGA which will use JTAG protocol (IEEE Std. 1149.1) for logic configuration parameter loading.

B67 - Frontend Electronics for the CMS Barrel Muon Chambers

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LHC Experiment: CMS

Abstract

Frontend electronics of CMS barrel muon chambers is organized in compact boards housed in the detector gas volume. The heart of the system is a custom ASIC that provides the primary processing of drift tubes signals and some ancillary functions reducing the necessity of external components. A flexible test pulses system for trigger calibration and I2C slow control features for channels enable/disable and detector temperature monitoring are also implemented. Attained results confirm the good performances of the whole system regarding efficiency, noise and low power consumption; particularly, radiation and ageing reliability were successfully tested in order to check

POSTER

The Clock and Control Board for the Cathode Strip Chamber Trigger and DAQ Electronics at the CMS Experiment

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Abstract

The design and functionality of the Clock and Control Board (CCB) for the Cathode Strip Chamber (CSC) peripheral electronics and Track Finder crate at the CMS experiment are described. The CCB performs interface functions between the Timing, Trigger and Control (TTC) system of the experiment and the CSC electronics.

Design and performance testing of the Read Out Boards for CMS-DT chambers

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Abstract

Readout boards (ROB) are one of the key elements of readout system for CMS barrel muon drift chambers. To insure proper and reliable operation under all detector environmental conditions an exhaustive set of tests have been developed and performed on the 30 pre-series ROB's before production starts.
These tests include operation under CMS radiation conditions to detect and estimate SEU rates, validation with real chamber signals and trigger rates, studies of time resolution and linearity, crosstalk analysis, track pattern generation for calibration and on-line tests, and temperature cycling to uncover marginal conditions. We present the status of the readout boards (ROB) and tests results.

The instrument for measuring dark current characteristics of straw chambers modules

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Large scale production of straw drift chambers requires efficient and fast methods of testing the quality of produced modules.
This paper describes the instrument which is capable to measure characteristics of dark currents of straw chambers modules in automated manner. It is intended for testing the LHCb Outer Tracker detector straw chambers modules during their production. It measures the dark current characteristics at any of the voltage in range from 0V to 3kV and stores them. These data will be then used at CERN for detector calibration.

The large scale production of the straw drift chambers in the LHCb experiment requires efficient and fast methods of testing the quality of produced modules. About 800 modules with 128 straws each will be produced resulting in total production of more than 100000 straws.
A common and powerful test of the quality of the produced straws is the measurement of the dark currents in a function of applied high voltage. The described below instrument will rise the high voltage applied to the wires in 128 straws in defined steps for a given range and will automatically measure dark currents consecutively in each straw. In this way all the problems related to improper wire mounting can be localized and corrected in the early stage of production process. In particular, it is possible to detect quickly the shorts on the wires.
The measurement cycle setup and control is done by a computer. The instrument is equipped with RS-232 data transmission protocol. Thus it can be connected to almost any computer because usually they are provided with it as a standard. This gives a kind of portability, for example when used with a laptop. If there is a computer with a CAN driver card available then optionally CAN Bus connection can be used.
After performing the measurements it is possible to store the data on a hard disk and use them later for any purpose. This feature allows to take the characteristics of built straw chambers modules and use them for calibrating LHCb Outer Tracker detector at CERN.
The typical measured current for a straw chamber is about few nA. Using this instrument we can measure the current with 128 pA resolution in the range up to 250 uA.

Compensation for the settling time and slew rate limitations of the CMS-ECAL Floating Point Preamplifier

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Abstract

The Floating Point Preamplifier of the Very Front End Electronics for the CMS Electromagnetic Calorimeter has been investigated on a 5x6 crystal prototype matrix. Discontinuities at the signal peak were observed in the pulse shape reconstruction from the 40MHz sampled and digitized data. The propositions linked to those observations are described, together with a focalized overview of the detector readout chain. A settling time problem is identified and it is shown that a 5ns delay applied to the ADC clock provides a secure solution. Finally, the implementation in the FPPA design of this delay is presented.

Improvements of the LHCb Readout Supervisor and Other TFC Modules

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Abstract

The LHCb Timing and Fast Control (TFC) system is entering the final phase of prototyping. This paper proposes improvements of the main TFC modules, two of which the most important are switching fully to the new Altera APEX family of PLDs and eliminating the PLX chip in the implementation of the local bus between the Credit Card PC and the board logic.
Since the Readout Supervisor is a very complex module, the prototyping was staged by starting out with a minimal version including the most critical logic and then adding the remaining logic in subsequent prototypes. The paper also covers all the additions in order to implement the final full version.

Low Voltage Control for the Liquid Argon Hadronic End-Cap Calorimeter of ATLAS

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Abstract

At the ATLAS detector a SCADA system surveys and controls the sub-detectors. The link is realized by PVSS2 software and a CanBus hardware system.
The low voltages for the Hadronic Endcaps of the Liquid Argon Calorimeter are produced by DC/DC-converters in the power boxes and split into 320 channels corresponding to the pre-amplifier and summing boards in the cryostat. Six units of a prototype distribution board are currently under test. Each of it contains 2 ELMBs as CanBus interface, a FPGA of type QL3012 for digital control and 30 low voltage regulators for the individual fine adjustments of the outputs.

Application specific analog semicustom array with complementary bipolar structures, intended to implement front-end electronic units

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Abstract

The structure of an analog semicustom array (SA), intended to implement front-end electronics ICs on its basis, is considered. The features of this SA are: implementation with bipolar technology at containing an equal number of NPN and PNP structures with like characteristics, supply voltages from 1.5V to 15V, transistor gain factors B_{st}~100 and unity gain frequencies F_t~(1.5…3)Ghz, high- and low-ohmic resistors, MOS capacitors, two variable plating levels.
Specific circuit diagrams and parameters of the front-end electronics ICs, created on the basis of the considered SA, are presented. The results of their tests are given.

Scintillation fiber detector of relativistic particles

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Abstract

At present the development of a silicon photomultiplier (SiPM), being a microcell photodiode with Geiger amplification, is going on. Such devices are capable of registering faint light bursts, what, in aggregate with their small dimensions, makes them highly promising for application as photoreceivers in scintillation fiber detectors. A bread-board model of a tracking detector of relativistic particles, containing 16 channels, has been designed and created. The characteristics of SiPM have been studied with a beta-source.
A read-out electronic unit, containing preamps, shapers, discriminators, has been designed to collect the signals of SiPM. The characteristics of this unit are presented and the prospects of its application in experimental physics are discussed.

Software framework developed for the slice test of the ATLAS end cap muon trigger system

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Abstract

A sliced system of the ATLAS end cap muon level 1 trigger has been constructed and tested. We have developed a software framework for property and run controls of the

system. As we have built a similar structure to both the property database described in XML for the system components and their configuration control program, we could obtain a simple and consistent software system. The system is described in C++ throughout. The multi-PC control system is accomplished using the CORBA system. In this report we discuss the present system in detail and future extension to be done for integration with the ATLAS online framework.

Data Acquisition and Power Electronic for Cryogenic Instrumentation in LHC under neutron radiation

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Abstract

This paper concern the tests performed at ITN (Portugal) for developing the radiation tolerant electronic instrumentation for the LHC cryogenic system. The radiation dose is equivalent to ten years of operation in the LHC machine. The results of commercial CMOS switches built in different technologies by several manufacturers and of power operational amplifiers are presented. Moreover, the degradation of the ADS7807 16 bit CMOS analog-to-digital converter is also described. Finally the increase of the series resistance of power bridge rectifiers is reported. The main parameters of the devices were measured on-line during the irradiation period and all of them were analyzed before and after the sample deactivation.

FPGA test benches used for Atlas TileCal Digitizer functional irradiation tests.

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Abstract

Before launching the full production of the Atlas Tile calorimeter digitizer board, system level tests were performed with ionizing, neutron and proton irradiation. For these functional tests FPGA based test benches were developed, providing a realistic run time

environment for the tests and checking system performance. Since the configuration of the digitizer is done via ttc-commands, received by a ttc-rx chip,the ttc-protocol was emulated inside the FPGA.

Design and use of a networked PPMC processor as shared-memory SCI node

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Abstract

The MCU mezzanine was designed as a networked, 486 processor-PMC for monitoring and control with remote boot capability for the LHCb Readout Unit (RU). As PCI monarch on the RU, it configures all PCI devices (FPGA's Linux operating system. A new application is within the LHCb L1-Velo trigger where a 2-dimensional CPU-farm is interconnected by SCI nodes, with data input from one RU at each row of the network. The SCI interface on the RU is hosted by the MCU, exporting and importing shareable memory in order to become part of the global shared memory of the trigger farm. Thereafter, trigger data are transferred by FPGA DMA engines, which can directly write via SCI to exported, remote memory.
Designed around a 100 MHz "PC-on-a-chip", the MCU mezzanine card is a fully compatible PC system. Conceived as a diskless monitoring and control unit (MCU) of the PCI bus subsystems on the LHCb Readout Unit (RU), it boots LINUX operating system from a remote server. It's implementation as a general purpose PMC card has allowed to use it in other target applications than slow control and monitoring. The successful integration of a RU into a shared memory trigger farm is one example.
The MCU's processor core is based on a Cyrix 486 core architecture which integrates a peripheral subsystem which is divided in two large blocks: embedded interfaces and I/O extensions. The embedded interfaces are serial and parallel ports, watchdog timers, EIDE, USB and floppy controllers, access bus (I2C compatible) interface, keyboard and PS/2 mouse systems. The extensions on the MCU are 10/100 Mbit ethernet and user programmable I/O. The latter are available via the VITA-32 user connector (P14) and provide the following programmable functions: 1.) I2C master 2.) JTAG master. Due to their programmed nature they operate at a 100 KHz level.
For the diskless boot operation, the BOOTP and DHCP protocol are used in succession. After receiving an IP address, the MCU requests from the server an operating system image which gets transmitted via a packet-based basic protocol (TFTP). When the operating system is completely loaded, it executes locally in the SDRAM of the MCU, and is capable of mounting a file system over the network. Normal user login is then available via remote login.
The MCU being a monarch, it scans and initializes the PCI bus of the RU during the boot operation and finds 1.) all four FPGAs and their resources 2.) an SCI network interface 3.) all data buffers and registers which are mapped via the FPGA's. In the LHCb L1-Velo trigger, a 2-dimensional CPU-farm network is implemented in 667 Mbyte/s SCI

technology with hundreds of CPUs at the x-y intersections and with data input from a RU at each row of the network. The SCI node interface on the RU is a PCI card, hosted by the MCU. Using the IRM driver for SCI, it exports and imports shareable memory with the other CPU nodes in the farm, thus becoming part of the global shared memory of the trigger farm. The SCI node adapter shares its 64 bit@66 MHz PCI bus segment with an FPGA-resident DMA engine. The latter requires a physical PCI address to copy, via SCI, trigger data to remote, exported memory in a destination CPU node. The corresponding physical address can be extracted after the
integration of the MCU into the shared memory cluster has been completed. The copy process from the local PCI bus to a remote PCI bus of a CPU is similar to a hardware copy to local memory, requiring only a few microseconds.

The APVE emulator to prevent front-end buffer overflows within the CMS Silicon Strip Tracker

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Abstract

A digital circuit board, using FPGA logic, is under construction to emulate the logic of the pipeline memory of the APV25 readout circuit for the CMS silicon strip Tracker. The primary function of the APVE design is to prevent buffer overflows. It will also provide information to the Front End Drivers (FEDs) to ensure synchronisation throughout the Silicon Strip Tracker. The purpose and the functionality of the APVE will be presented along with results from simulation and operation.

The electronic stability of silicon front-end hybrids

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Abstract

This paper analyzes the electronic stability of current silicon front-end hybrids. Ground foil AC power summation delivers the additional amplification of the front-end chips analog input signals, in order to start oscillation when the number of operating front-end chips is greater then an critical number. General solutions are givens to start a discussion.

Experience with easy to use and difficult to use front-end chips is given. A requirement for the design specification of front-end chips is made.

SiC Pressure Sensors Radiation Hardness Investigations

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Abstract

Radiation investigations of SiC-based pressure sensors were carried out. It was experimentally shown that these devices are more thermal stable and radiation hard as compared to the Si-based pressure sensors. It is connected with the basic physical properties of SiC such as wide bandgap, high thermal conductivity etc. The theoretical investigations were performed to explain the experimentally measured radiation hardness of SiC pressure bridge under dose rate, total dose and neutron flux irradiation. The good agreement between theoretical and experimental data confirms the high potential of SiC devices for harsh applications.

A very low offset voltage auto-zero stabilized CMOS operational amplifier

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Abstract

A high precision operational amplifier has been developed in a standard .8u CMOS process. A continuous time auto-zero stabilized architecture is used, that leads to a typical input offset voltage less than 2uV +100nV/degre. The amplifier with its output buffer consumes 5mW at a supply voltage of +/- 2.5V. The gain bandwidth product is 2Mhz while the slew rate is respectively -6V/uS and +8.8V/uS on 10pF with 10Kohm load. This amplifier is suitable to control a large dynamic (>10E5) calibration signal, and for very low signal instrumentation.

Design, Prototyping and Testing of the Detector Control System for the ATLAS Endcap Muon Trigger

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Abstract

The TGC detector will be inaccessible during operation due to high radiation levels in the ATLAS cavern. The detector requires a Detector Control System (DCS) to monitor important detector and environmental parameters, calibrate, set and maintain the configuration of FE electronics, and take appropriate corrective action to maintain detector stability and reliable performance.
The TGC DCS system makes full utilization of the intelligence offered by the ATLAS ELMB CAN nodes in order to distribute the control of complex tasks on the front end nodes. This talk will describe our hardware and software design, integration and radiation test results.

Radiation Tolerance Tests of CMOS Active Pixel Sensors used for the CMS Muon Barrel Alignment

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Abstract

Neutron and proton irradiation tests were performed to study the radiation induced alterations of COTS (Commercially available Off The Shelf) CMOS active pixel sensors at two facilities. The sensors will be used for the CMS Barrel Muon Alignment system. Results of the tests are presented in this paper.

Neutron induced radioactivity of components of integrated circuits operating in intense radiation environments

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Abstract

Neutron induced activation of a monolithic ASIC and some packagings were studied. It was found that the gamma dose from the activated components of the device could be, on the average, some 10 % of the dose from the external radiation environment at the position of operation of the circuit in LHC detectors. At the same time, the auto-radiogram of the neutron activated monolithic ASIC had shown that "hot spots" of induced radioactivity can develop in the structure where the radiation damage hazard can be significantly higher.
This work was supported in part by the Hungarian Scientific Research Fund (OTKA-T026184).

A Measurement of the Radiation Field in the CDF Tracking Volume"

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Abstract

We present direct measurements of the spatial distribution of both ionizing radiation and low energy neutrons (E_n < 200keV) inside the tracking volume of the Collider Detector Facility (CDF) at Fermilab. Using data from multiple exposures we are able to separate the contributions from beam losses and proton-antiproton collisions. Initial measurements of leakage currents in the CDF silicon detectors show patterns consistent with predictions based on our measurements.

The trigger for K^0 ® p^0 p^0 decays of the NA48 experiment at CERN

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NA48 Collaboration

Abstract

The trigger used for the collection of the samples of $K^0 \rightarrow \pi^0 \pi^0$ decays in the NA48 experiment at CERN has successfully operated over several years. The novelty of this system is largely its architecture, where the entire trigger computation is performed in a single, fully synchronous and dead-time-free pipeline, running at the common experiment clock frequency of 40 MHz. This approach allowed to cope with the demanding specifications of a high rate kaon beam. The feature of having no dead time is most important in the ε'/ε analysis. The system was also sufficiently flexible to allow rare decay triggers to be added. The trigger efficiency was carefully studied and is well understood. The overall measured efficiency for $K^0 \rightarrow \pi^0 \pi^0$ events is (99.920 ± 0.009)\%; it is the same for K_S and K_L events, thus bearing no correction on the double ratio measurement.

SynUTC – High Precision Time Synchronization over Ethernet Networks

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Abstract

This article describes our SynUTC (Synchronized Universal Time Coordinated) technology, which enables high-accuracy distribution of GPS time and time synchronization of network nodes connected via standard Ethernet LANs. By means of exchanging data packets in conjunction with moderate hardware support at nodes and switches, an overall worst-case accuracy in the range of some 100 ns can be achieved, with negligible communication overhead. Our technology thus improves the 1 ms-range accuracy achievable by conventional, software-based approaches like NTP by 4 orders of magnitude. Applications can use the high-accuracy global time provided by SynUTC for event timestamping and event generation both at hardware and software level.

SynUTC is based upon inserting highly accurate time information into dedicated data packets at the media-independent interface (MII) between the physical layer transceiver and the network controller upon packet transmission and reception, respectively. As a consequence, every node has access to the local time information of any communication peer and can therefore re-adjust it's local clock accordingly. This enables both simple solutions based upon synchronizing with a (GPS-equipped) master node as well as elaborate fault-tolerant clock synchronization algorithms.

Each node must be equipped with a special network interface card (NIC) for this purpose, which extends standard NIC chipsets by a custom hardware encapsulated in a single IC plugged into the MII. This chip contains primarily a high-precision adjustable adder-based clock and timestamping registers as well as a uC core executing the synchronization algorithm. Our technology is generic, in the sense that our hardware support can be used with any NIC chipset based upon the MII. Moreover, since clock synchronization, except a simple service that broadcasts messages on a regular basis, is performed by the on-chip uC, standard NIC device drivers and protocol stacks can be used without changing. Last but not least, the principle underlying SynUTC is not limited to Ethernet-based networks but is applicable for any packet-oriented data network as well.

To verify the feasibility of our approach, a research prototype has already been developed and evaluated successfully. Currently, a multi-node demonstration system is being built to facilitate the transfer of our SynUTC technology in commercial applications.

ASubracks (Crates) and Power supplies for LHC Experiments

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Abstract

Powered and cooled Subracks for the LHC experiments have been described as well as special Power Supplies, either for supplying remotely, over long distance, or in front of the detector electronics as a radiation and magnetic field tolerant system. For low magnetic environment fan cooled, and for higher magnetic fields water cooled power supplies are reviewed. Common to all are the low noise DC outputs, even at higher currents. The installation of a sufficient remote monitoring system basing on CANbus, Ethernet and WorldFip is possible.